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SAMOS

SUBSYSTEM F - FERRET 2 SYSTEM
ENGINEERING ANALYSIS REPORT

VOLUME I

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Prepared by

SATELLITE SYSTEMS SUBSYSTEM F DEVELOPMENT

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SATELLITE SYSTEMS SAMOS PROGRAM

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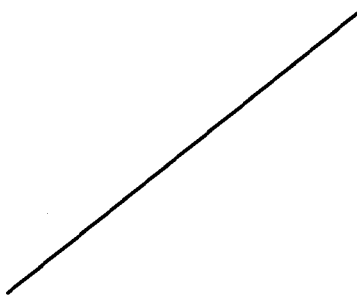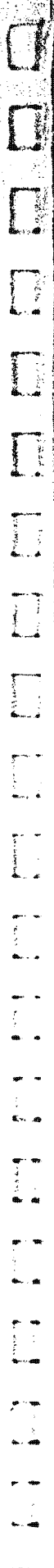
FOREWORD

The two volumes of this report analyze the Ferret 2 (F2)
system of Subsystem F for Samos satellites. The report
was prepared by Lockheed Missiles and Space Division in
accordance with Contract AF 04(647)-563. Volume I (Sec-
tions 1 - 4) gives a general description of Subsystem F
and analyzes payload and checkout equipment. Volume II
(Sections 5 - 9) analyzes the ground data-handling
system, on-orbit calibration equipment, field-support
program, system engineering, and reliability.

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Volume I

SUMMARY

The purpose of the Ferret 2 system is to ferret emitter radiations from an orbiting satellite. As the Samos satellite speeds along its orbital path, ferret antennas in the payload scan the earth's surface and intercept radar signals. Receivers in the payload pass these signals to a data handler which measures their characteristics and accordingly either rejects or accepts the intercept data. Accepted signals are converted into coded form and are stored for future reconversion into signals suitable for transmission to the ground.

This report explains the function of the major equipment, both spaceborne and ground-based, which is used in the operation of the Ferret 2 system. Here is a brief survey of the analysis of the system.

Two different antenna arrays intercept emitter radiations -- one is used in the payloads of Flights 1 and 2, the other is used in those of Flights 3 and 4. Each payload uses a similar receiving system to pass the intercepted radar signals, namely a frequency-scanning superheterodyne.

Intercept signals from the ferret receivers in the payload are examined by a data handler which is a transistorized digital device. This device verifies whether a received signal is a valid intercept and then either stores the intercept signal or rejects it. Acceptable data are recorded for future telemetry transmission to ground.

Valid intercept data collected by the payload are transmitted to ground via a telemetry link (Subsystem H). The ground system which receives these data comprise conversion equipment, display equipment, and payload-command equipment located at two tracking and acquisition stations and the Satellite Test Center. After receiving these data, the ground-handling equipment processes them for transmission to the user (Subsystem I). Also, the

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equipment controls the engineering functions of monitoring, calibration, and on-orbit adjustment of the payload.

Before the ferret payload lifts from the launch pad atop the Samos vehicle, the payload equipment is subjected to an extensive checkout on the ground. Components and subsystems within the payload are checked and tested to assure that the ferret system will work properly during orbital flight.

Also, before the ferret payload is ready for launching, personnel who will operate, maintain, and check out Subsystem F equipment are trained in their respective tasks. Adequate training guarantees capable operation and maintenance of equipment.

The F-2 System design program is augmented by several studies which provide mathematical and technical analyses in critical areas affecting system development and operation. These areas include readout, calibration frequency, effects of satellite tilt, orbital structure for F-2 satellites, off-frequency detection, spurious emissions, inhibit clogging, terrain reflections, strong signals, minimum detectable signals, and location accuracy of the F-2 system.

The reliability of the F-2 payload is discussed in the last section of the report. Equipment reliability, which emulates calculated predictions of reliability whenever possible, is ensured through a thorough program of evaluation. This program calls for a review of all designs, testing components, establishing standards and application criteria, and analyzing malfunctions. Parts and materials are also tested to determine whether they will withstand their operational environment for extended periods of time.

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SECTION 1
GENERAL DESCRIPTION OF SUBSYSTEM F

1.1 GENERAL CHARACTERISTICS

Subsystem F is an electronic reconnaissance subsystem of spaceborne equipment that collects intelligence information from radiations in the 30 to 300, 000 Mc range. The equipment processes and stores the intercept information in coded form and, at the proper time, reconverts the stored information into a form suitable for transmission to the ground. Subsystem F ground data handling equipment receives the ferret data from the satellite, via the Communications and Control (C&C) Subsystem, processes it for transmission to the user (Subsystem I), and handles the engineering functions (such as monitoring, calibration, and on-orbit adjustment) required for proper operation of the payload equipment. Subsystem F calibration vans transmit known signals from locations at specified times to the ferret equipment for on-orbit calibration of the reconnaissance system. Subsystem F ground support equipment provides the preflight checkouts of the spaceborne equipment. Subsystem F consists of the following equipment: (a) spaceborne ferret, (b) ground-based data handling, (c) ground-based calibration, and (d) ground-based checkout.

Figure 1-1 is an overall block diagram of Subsystem F. A frequency-scanning superheterodyne intercept receiving system is used because of its superior sensitivity, frequency selectivity, adaptability to advanced systems, and relatively low power requirements. The frequency range is divided into 19 receiver bands (Table 1-1). Each model of Subsystem F contains receivers that cover selected frequency bands. The Ferret 2 (F-2) System contains receivers for bands 1, 2, 3b, and 3c. For each band, a two-channel receiver is used. One channel is connected to a "signal" antenna, and the other channel is connected to an "inhibit" antenna. The antenna patterns of the two channels are such that within a cone having an apex angle of

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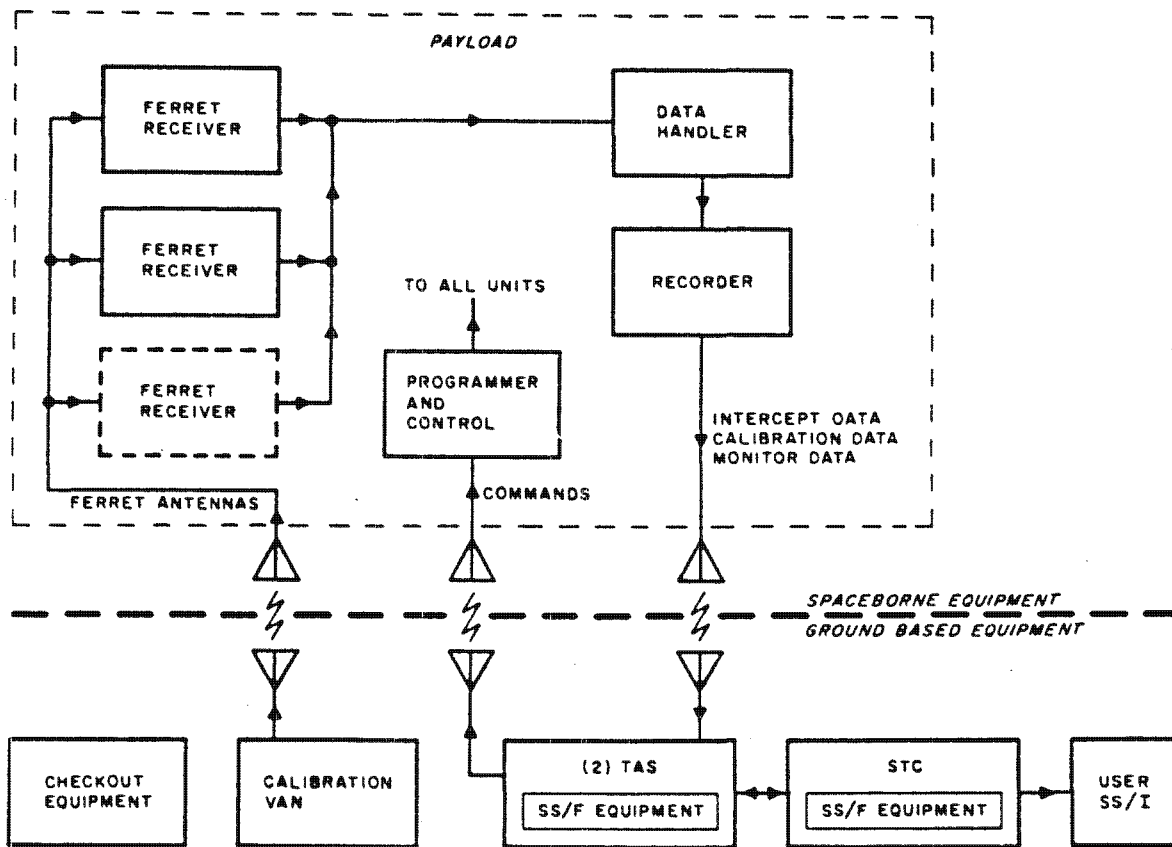
Figure 1-1 Block Diagram of Subsystem F

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Table 1-1

FREQUENCY BANDS

Frequency Band (Mc)	Priority Number	Frequency Band (kmc)	Priority Number
30 to 59	10	8.2 to 12.4	8
59 to 130	3a	9 to 10	2
130 to 290	3b	12.4 to 18	9
290 to 650	3c	18 to 27	11
650 to 1300	4	27 to 40	12
1300 to 2500	6	40 to 60	13
2500 to 3200	1	60 to 90	14
3200 to 5130	5	90 to 135	15
5130 to 8200	7	135 to 200	16
		200 to 300	17

about 32 degrees centered at the nadir of the satellite, the gain of the signal channel is higher than that of the inhibit channel. For all directions outside this cone, the inhibit-channel gain is greater than the signal-channel gain. By directing these two received signals into an amplitude comparator, it is possible to reject all signals that come from a direction outside the 32-degree coverage cone, and to pass to the data handling circuits only the signals from emitters lying within the coverage cone.

The data handling circuits in the payload measure parameters of the received signals, store desired information, reject some redundant information, and at the proper time reconvert the stored signals into a form suitable for transmission by the communications and control system.

Digital techniques provide sufficient flexibility to minimize the redesign that might be needed to handle different types of information in later missions. They lend themselves to extremely reliable design, since moderate changes in component characteristics need not affect the validity of the data system

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output. They are well suited for selecting desired information, and for temporary storage and transmission of extracted data.

It is necessary to program the intercept receivers and data handling circuits so that (a) the desired intelligence information is intercepted and processed, (b) the payload equipment is monitored and calibrated to keep apprised of the reliability of the intercepted data as processed, (c) defective components are detected, and adjusted or replaced, and (d) the intercept equipment reads out information to and accepts commands from an authorized interrogation station only. These four functions are performed by the payload control system in conjunction with the C&C decoder and sequence programmer; the control system relays the decoded and processed instructions to the designated units.

Coded ferret information received at the ground station will be decoded and technically processed by the ground data handling equipment. This equipment, which is part of the ground-based satellite control equipment, has two general functions: a technical processing function and a technical supervision function. It processes, corrects, and assembles data quickly, accurately, and in a form suitable for the user (Subsystem I). It processes test data, calibration data, and other data from the payload and from various Subsystem F ground installations to ensure proper technical operation of the ferret equipment. It permits the establishing of data-correction factors, and it permits complete and adequate monitoring of all aspects of equipment performance. On-orbit payload equipment adjustments for technical or operational reasons are also part of its function.

The ground-based satellite control equipment also includes the on-orbit calibration equipment. For on-orbit calibration it is necessary to transmit radar signals whose frequencies, PRF, and PW are accurately known. Knowledge of the operational status of the satellite-borne equipment is obtained by comparing the intercepted calibration data as retransmitted from the satellite to the control center with the data originally transmitted. The ferret equipment will intercept calibration transmissions only when the calibration station is being illuminated by the Subsystem F signal antennas.

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Generally, the satellite will pass directly over a station within the United States only once or twice a week. A calibration van will be located at each tracking and acquisition station (TAS).

The ground support program provides equipment needed for preflight checkout of the ferret equipment. The checkout equipment provides an overall system test by injecting accurately calibrated simulated radar signals to test all components of the ferret system.

1.2 PARAMETER-MEASUREMENT DATA

When a signal is accepted as a valid intercept by the ferret receivers, data handling circuits extract the desired information from the received pulses and store the information in digital form for future transmission to the ground. The signal parameters that are measured and stored in all F-2 models are frequency, PRF (measured as pulse intervals), PW, and time-of-intercept. In one of the F-2 models, nonuniform PRF, pulse amplitude, amplitude difference, single pulses, long pulses, and sequential pulses are measured (or detected) also.

The scan rates of the ferret receivers are slow enough to provide sufficient time in each channel for interception of at least three pulses at the lowest expected PRF. Therefore, two PRF measurements can be obtained for each signal. If only one radar signal is intercepted per frequency channel, then the PRF measurement is usually constant from pulse to pulse. If two or more signals are intercepted in one channel, however, the measured PRF will almost always have two different values for two consecutive intervals. In this case, additional correlation is needed to identify the radars, but the possibility that two or more may be present will be known. The PRF measurements are a better indication of the number of emitters than the PW measurements; the same PW could be used by a number of radars at a given frequency, but it is unlikely that more than one radar would have the same PRF. The bands are scanned serially from the lowest to the highest frequency. Each receiver is operational only during its scan period.

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During the off period of each receiver, the scan mechanism returns to the initial setting.

1.3 SIGNAL LOCATION

The apparent location of an emitter depends upon the location and attitude of the satellite at the time-of-intercept and on the radiation patterns of the intercept antennas. The position of the satellite is measured by another sub-system. The altitude information is received, converted into digital form, and formed into a digital word once each scan cycle.

In the cone whose apex is 32 degrees centered at the satellite's nadir, the gain of the signal antenna is, ideally, greater than that of the inhibit antenna; in the remainder of the area beneath the satellite, the gain of the inhibit antenna is greater. Thus, the signal antenna intercepts an on-the-ground circle with a diameter of about 172 nautical miles if the satellite is at an altitude of 300 nm. By comparing the amplitudes of the same signal from the two antennas, the location of the signal's emitter is determined to be either inside or outside the signal channel's cone of coverage. The emitter is located more accurately by choice of the frequency-scan time. The method of this accurate location is described in the following paragraph.

Assume a hypothetical airborne reconnaissance satellite that has a ground speed of 3.80 miles per second, that intercepts emitters within a circle having a diameter of 172 miles, and that scans all frequency bands at least once every 22.6 seconds. During one 22.6-second frequency scan the satellite travels about 86 miles. If on two successive scans the same sig-nal is intercepted, the apparent location of its emitter is known more accu-rately (Figure 1-2). In the direction of motion the emitter is located with an error not greater than 43 miles; its location in a transverse direction may have an error of 74 miles. (If the signal is intercepted only once, its locational error ranges up to 86 miles.) With a faster scan time--15 seconds, for example--the number of times that a single emitter will be intercepted during one orbit will be increased. If a radar is intercepted on three successive scans, its location in the direction of motion will be

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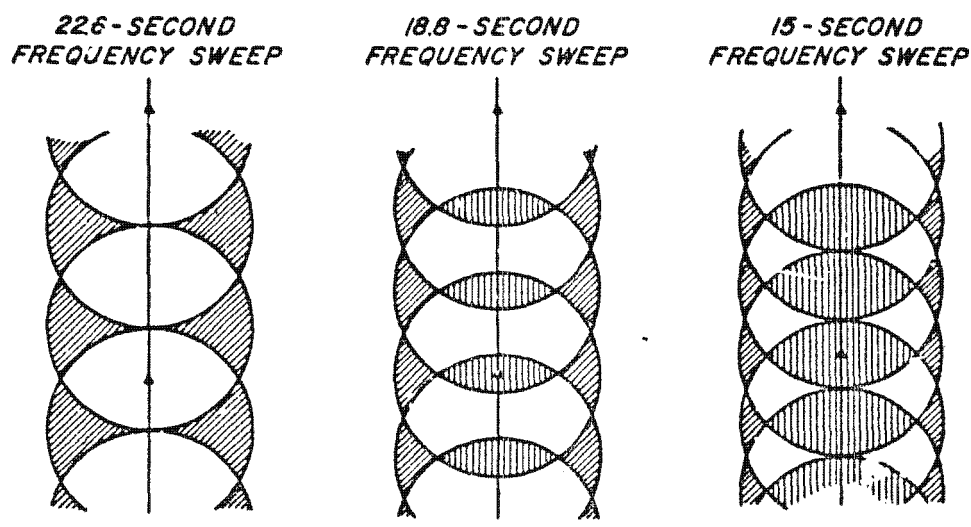
REGION OF I INTERCEPT PER ORBIT
REGION OF 2 INTERCEPTS PER ORBIT
REGION OF 3 INTERCEPTS PER ORBIT

ASSUMPTIONS:
    DIAMETER OF CIRCLE = 172 NAUTICAL MILES
    GROUND VELOCITY = 13,700 NAUTICAL MILES PER
                        HOUR (3.80 NM/SEC)

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Figure 1-2 Location of Emitters

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determined within 29 miles and its location in the transverse directions will be determined within 64 miles.

Another method of increasing the accuracy of emitter location requires the measurement of pulse amplitude to help determine that portion of the antenna coverage pattern in which the signal was intercepted.

It is clear that the accuracy of emitter location is affected by the ferret antenna radiation patterns, by the height, velocity, and orbital stability of the satellite, and by the scan time of the ferret receivers. Only when all of these parameters are known can the accuracy of probable location on a single pass be determined. More accurate location depends on use of overlap areas in adjacent swaths. As intercept data accumulate, the locational accuracy of each emitter will increase.

1.4 F-2 MODELS

The F-2 satellite-borne equipment has two submodels: F-2 (flights 1 and 2) and F-2 (flights 3 and 4). The F-2 (flts 1, 2) equipment contains receivers for bands 1 and 2. The band 3a antenna is included in the antenna array. This antenna, however, is not presently used by Subsystem F. The F-2 (flts 3, 4) payload contains receivers for bands 1, 3b, and 3c. The checkout and ground data handling equipment are primarily for the F-2 (flts 1, 2) model. Modifications or additions will be made so that the equipment can serve both F-2 models when the F-2 (flts 3, 4) payloads are ready for use.

1.5 PERFORMANCE CHARACTERISTICS OF F-2 (FLIGHTS 1 AND 2) PAYLOAD

Frequency Coverage	Band 1: 2500 to 3200 Mc
	Band 2: 9000 to 10,000 Mc
Scan Time	Band 1: 6.6 seconds
	Band 2: 4.8 seconds
Cycle Time (2 bands)	13.5 seconds
PRF Measurement	125 to 25,000 pps

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PW Measurement	1.0 to 30.0 μsec
Data Handler Resolution	±0.5 μsec
Payload System Accuracy	+1.5, -0.5 μsec

Signal-Antenna Gain	13 db minimum at beam center
Receiver Threshold Sensitivity	-80 dbm
Receiver Noise Figure	15 db maximum
Local-Oscillator Accuracy	1 percent minimum

IF Bandwidth:	Signal Channel	Inhibit Channel
Band 1	2.5 ± 0.2 Mc	4.0 ± 0.3 Mc
Band 2	5.0 ± 0.2 Mc	8.0 ± 1.0 Mc

Dynamic Range of Receiver	
Input	60 db
Output	20 db

Ground Area Coverage (for 90 percent triggering)	172 nm diameter circle
Locational Accuracy	±50 nm
Maximum intercept Recording Rate	40 per second
Start-Record-Stop Intervals	5 millisec for each (nominal)
Bit Length	100 ± 20 μsec
Intercept Word Length	50 bits
Time Interval, Tape Readout	5 ± 1.0 millisec
Time Interval, Direct Readout	5 ± 0.1 millisec

Intercept Capacity	10,000 words minimum
Intercept Data Output	PRF (2), PW, time, frequency, band, attitude
Maximum Readout Time	100 ± 20 seconds

1.6 PERFORMANCE CHARACTERISTICS OF F-2 (FLIGHTS 3 AND 4) PAYLOAD

Frequency Coverage	Band 1:	2500 to 3200 Mc
	Band 3b:	130 to 290 Mc
	Band 3c:	290 to 650 Mc

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Scan Time	Band 1: 4. 2 seconds Band 3b: 2. 4 seconds Band 3c: 5. 4 seconds
Cycle Time (3 bands)	13. 8 seconds
PRF Measurement	Band 1: 200 to 20, 000 pps Bands 3b and 3c: 80 to 20, 000 pps
PW Measurement	1. 0 μsec to 2 millisec
Data Handler Resolution	$\pm$0. 5 μsec below 32 μsec +32 μsec above 50 μsec $\pm$16 μsec between 32 and 50 μsec

Signal-Antenna Gain	Band 1: 10 to 15 db within coverage
	              circle
	Bands 3b and 3c: 0 db within cover-
	                              age circle

Receiver Sensitivity	-80 dbm
Receiver Noise Figure	Band 1: 14 db (measured) Bands 3b and 3c: 12 db* (calculated)
I-F Bandwidth	

All Bands	Signal channel: 2. 5 $\pm$ 0. 2 Mc
	Inhibit channel: approximately 8 Mc
	                          (bandwidth of log
	                          IF channel)

Dynamic Range of Receiver	
Input	60 db
Output	20 db
Ground Area Coverage (for 90 percent triggering)	
Band 1	Circle coverage, 172 nm diameter (nominal)
Band 3b	Swath coverage size to be determined
Band 3c	Circle coverage, 300 nm diameter
Maximum Intercept Recording Rate	66 per second (maximum capability of data handler)
Start-Stop Intervals	5 millisec for each (nominal)

---

* To be determined.

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Record Intervals	6.8 millisec
Bit Length	
Tape Readout	100 ± 20 µsec
Direct Readout	100 ± 2 µsec
Intercept Word Length	68 bits
Time Interval, Tape Readout	6.8 ± 1.0 millisec
Time Interval, Direct Readout	6.8 ± 0.14 millisec
Spare Bits	7
Maximum Number of Intercepts Before Tape Readout	7500 words or more
Intercept Data	Same as for F-2 (flts 1, 2) plus pulse amplitude, pulse amplitude difference, alarm bit for nonuniform PRF, single-frequency sequential, and long pulse
Maximum Readout Time	100 ± 20 seconds

SECTION 2
FERRET 2 (FLIGHTS 1 and 2) PAYLOAD EQUIPMENT

2.1 ANTENNAS

The F-2 (flts 1, 2) antennas are distinctly different from the F-1 antennas. The F-2 antenna systems provide three advantages: (a) extended frequency range with improved SWR over the range, (b) improved circular-polarization performance, and (c) considerably less bulk and weight for the band 1 cigar antenna, compared with the large F-1 band 1 horn.

The antenna array for the F-2 (flts 1, 2) payload equipment is shown in Figure 2-1. The band 1 inhibit antenna is a crossed dipole (turnstile), as shown in Figure 2-2. The antenna is fed in phase quadrature by a coupler (Figure 2-3), to obtain circular polarization. The band 1 signal antenna consists of the same type of turnstile antenna, and has a cigar element added to increase the directivity and gain (Figure 2-4). Radiation patterns of the band 1 antennas are shown in Figure 2-5.

The band 2 signal antenna is an octagonal horn (Figure 2-6). Circular polarization is achieved by using a metal-probe phase shifter, and by running a twisted waveguide from the standard X-band waveguide to the square waveguide of the phase-shifting section. The octagonal horn provides lower sidelobe levels than does a square horn. The band 2 inhibit antenna (Figure 2-7) is an open-end waveguide with a square cross section and a circular ground plane about 0.75 inch from the end. Its circular polarization is achieved by the use of a phase shifter similar to that used in the signal antenna and a twisted waveguide section identical with that used in the signal antenna. A resistance card (cross-mode absorber) is included between the phase shifter and the twist section to maintain low ellipticity (good circular polarization) — over the band. Radiation patterns of the band 2 antennas are shown in Figure 2-8.

2-1
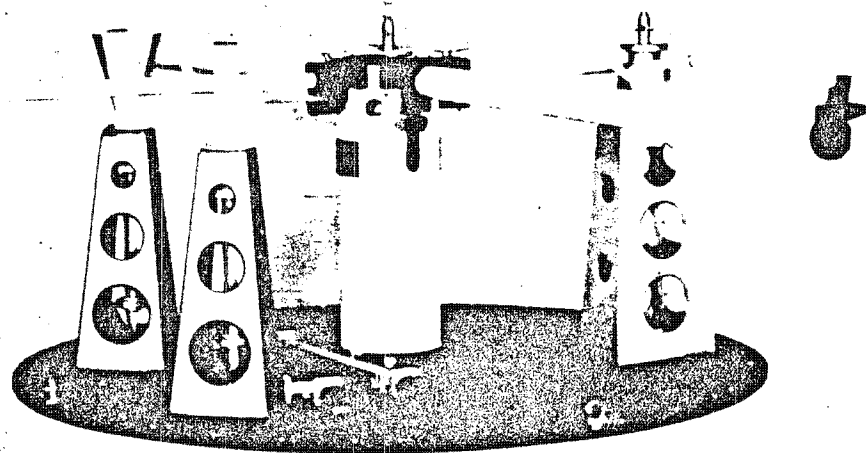
Figure 2-1 Antenna Array for F-2 (Flts 1, 2) Payload
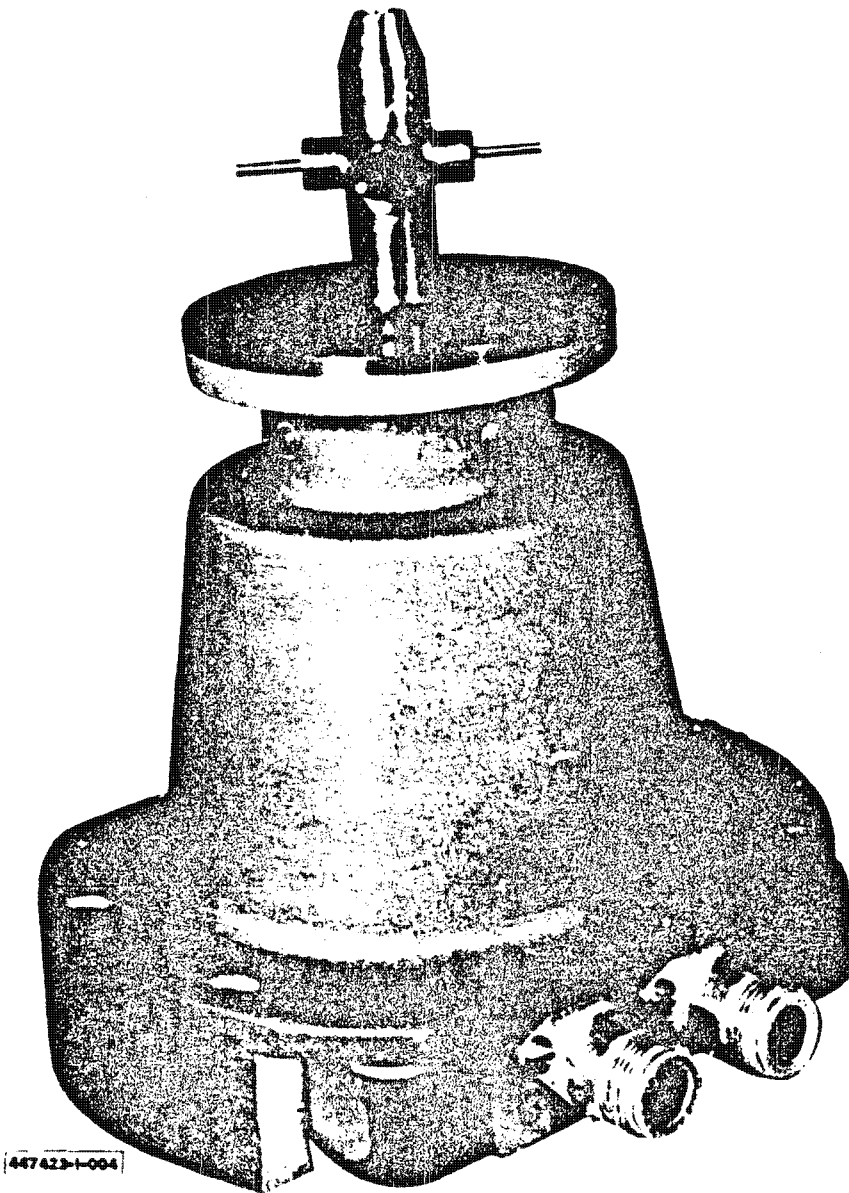
Figure 2-2 Band 1 Inhibit Antenna

2-3
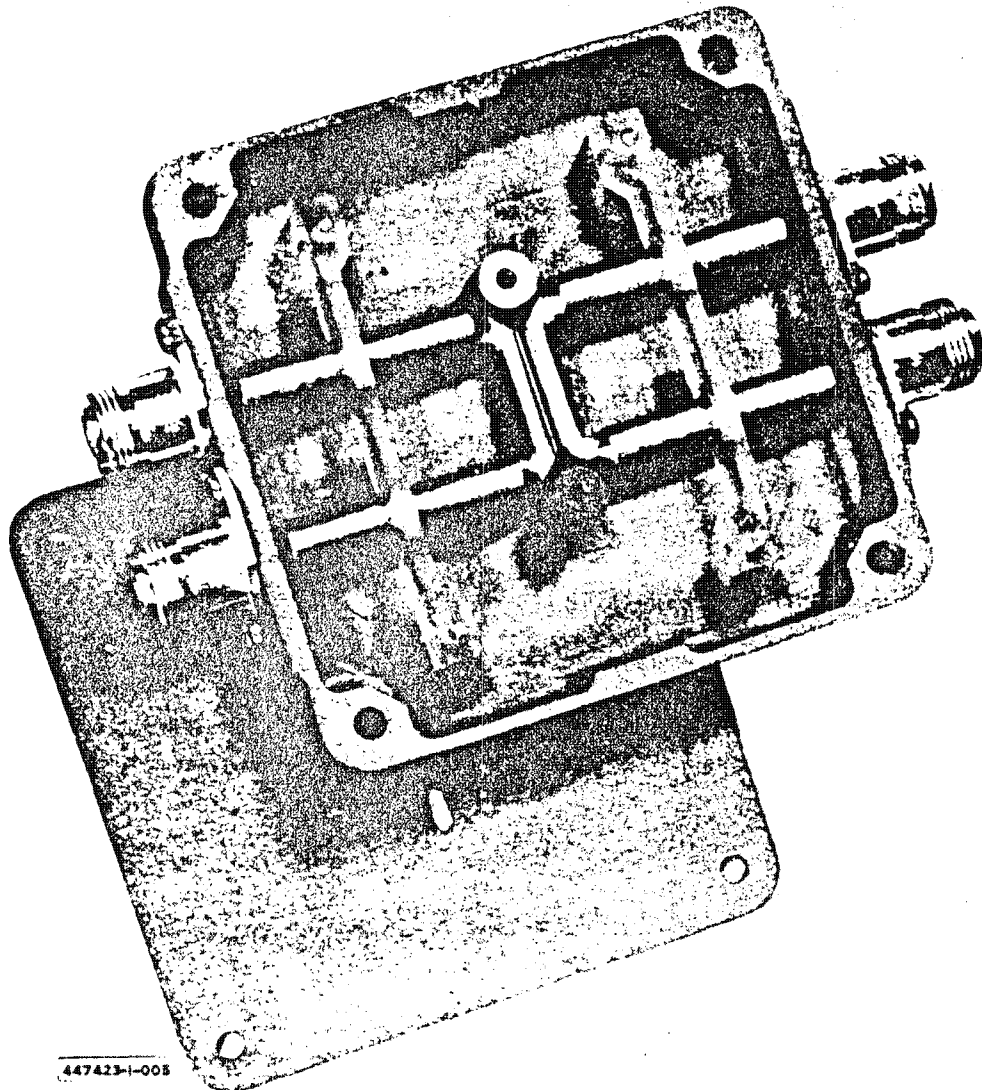
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Figure 2-3 Band 1 Antenna Coupler

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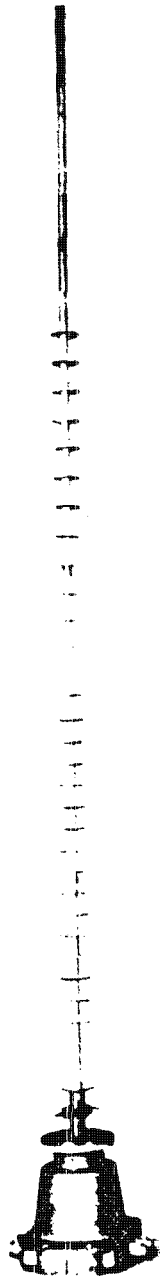
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Figure 2-4 Band 1 Signal Antenna

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INHIBIT ANTENNA
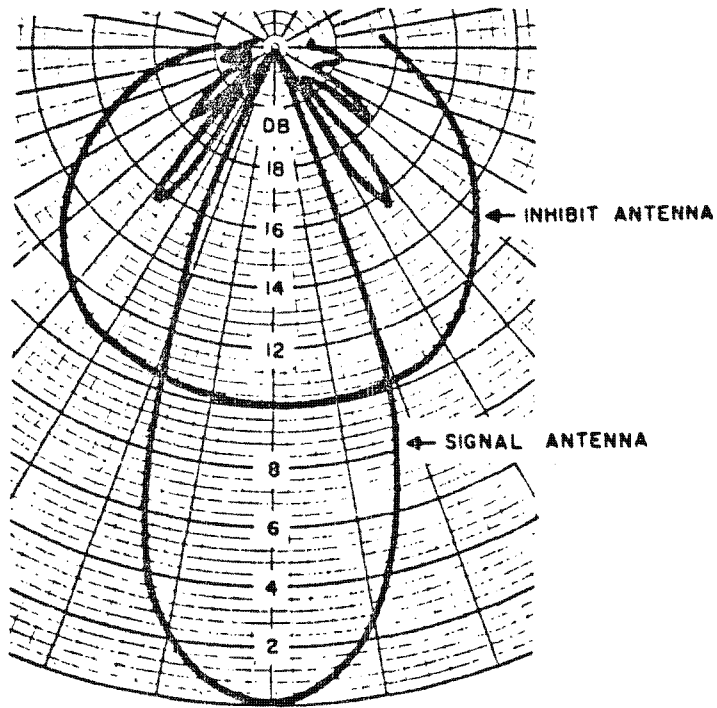
SIGNAL ANTENNA

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Figure 2-5 Radiation Patterns of Band 1 Antennas

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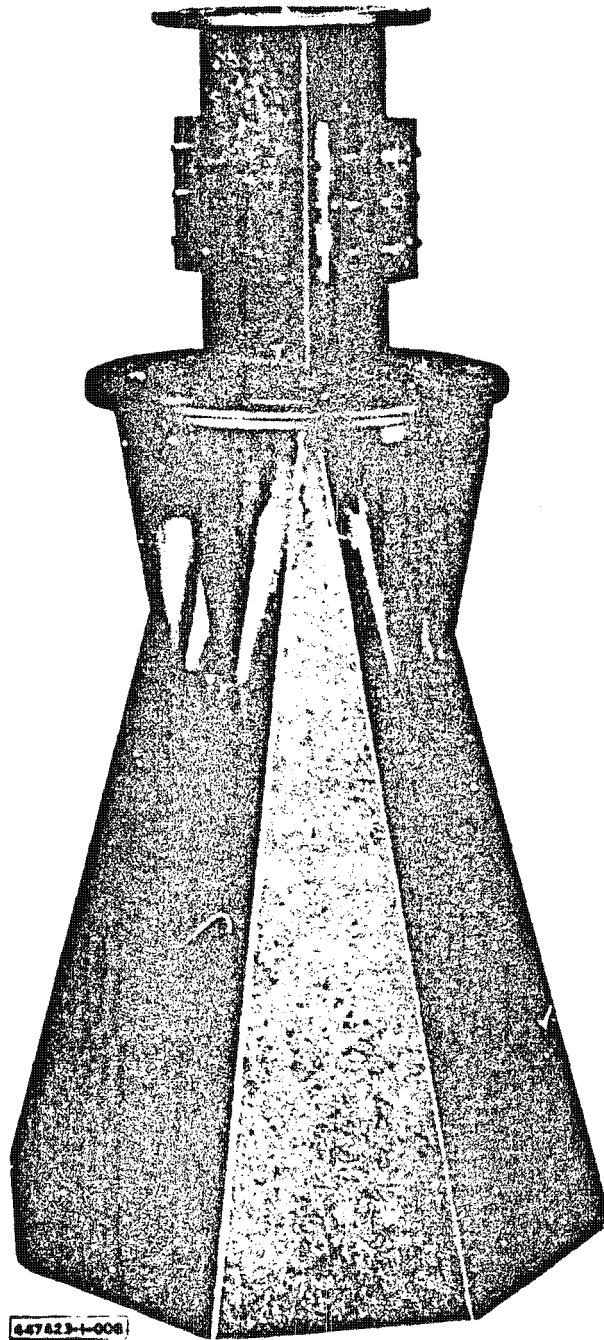
Figure 2-6 Band 2 Signal Antenna

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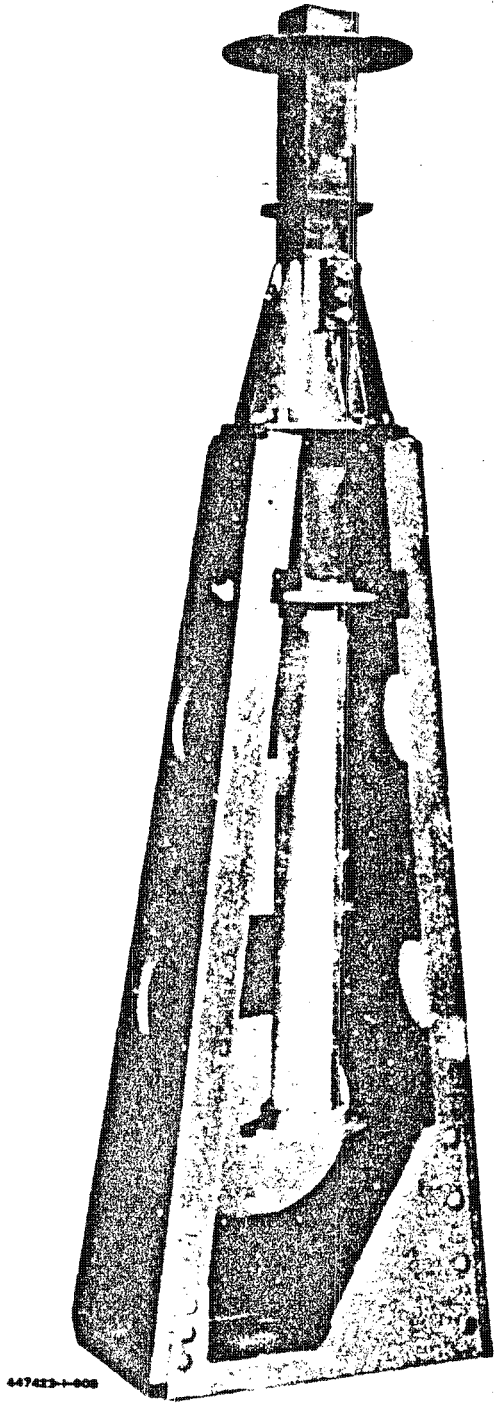
Figure 2-7 Band 2 Inhibit Antenna

2-8
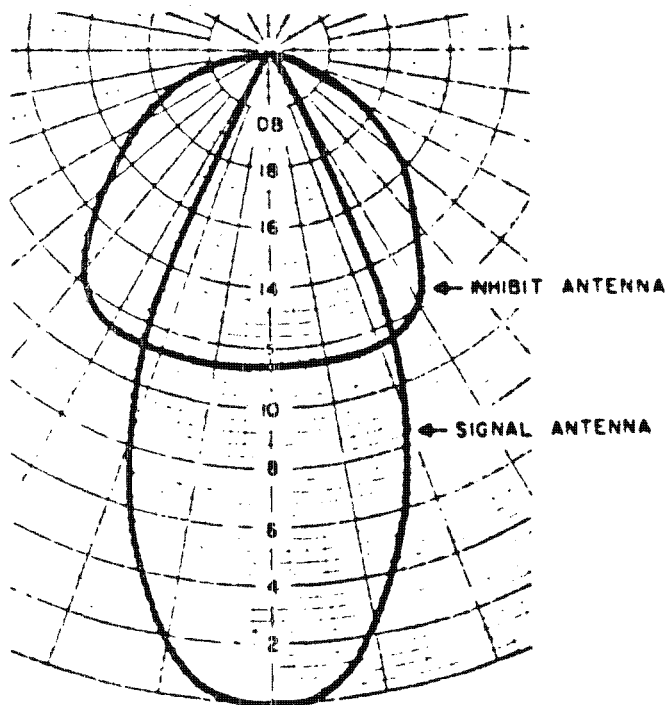
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Figure 2-8 Radiation Patterns of Band 2 Antennas

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The band 3a dipole antenna is designed to operate in two modes to provide both signal and inhibit functions. The normal dipole mode (signal mode) is the sum mode, in which current flows in the same direction in both halves of the dipole. This mode provides the familiar figure eight radiation pattern. In the difference mode (inhibit mode) the current flows in opposite directions in the two halves and provides a null in the radiation pattern in a plane normal to the dipole at its midpoint. With a hybrid feed, the dipole can be operated in both modes at the same time. In such operation a bandwidth ratio somewhat greater than 2:1 is achieved. The dipole's length is such that the electrical length varies from about 0.5 to about 1 wavelength over the frequency band.

The band 1 signal antenna serves as a return path for the current in the low end of band 3a. For this reason the cigar is made about 0.25 wavelength long at the low frequency. The dipole antenna is insulated from the equipment, and fed with coaxial feed lines cut in high-impedance lengths. To limit undesirable radiation from the ground structure (the payload), a pair of resonant (at mid-band) spokes are added in space quadrature. This antenna configuration provides only partial inhibit action.

Figure 2-9 shows the band 3a antenna in the operating position, with the band 1 cigar antenna mounted in the center. Space limitations dictate that the antenna will be folded for packaging as shown in Figure 2-10. The antenna will be erected after the payload is in orbit. In the F-2 (flts 1, 2) payload, the band 3a antenna is inoperable since there is no band 3a receiver. There will be no RF connections to this antenna; it will serve as a structural support (during flight) for the band 1 antenna.

2.2 RECEIVERS

Figure 2-11 is a block diagram of the superheterodyne receivers used in the F-2 (flts 1, 2) payloads. Each receiver has a signal channel and an inhibit channel. In general, the two channels differ in that the signal channel contains a preselector for image and spurious-response rejection, and the IF bandwidth of the signal channel is less than that of the inhibit channel, thus
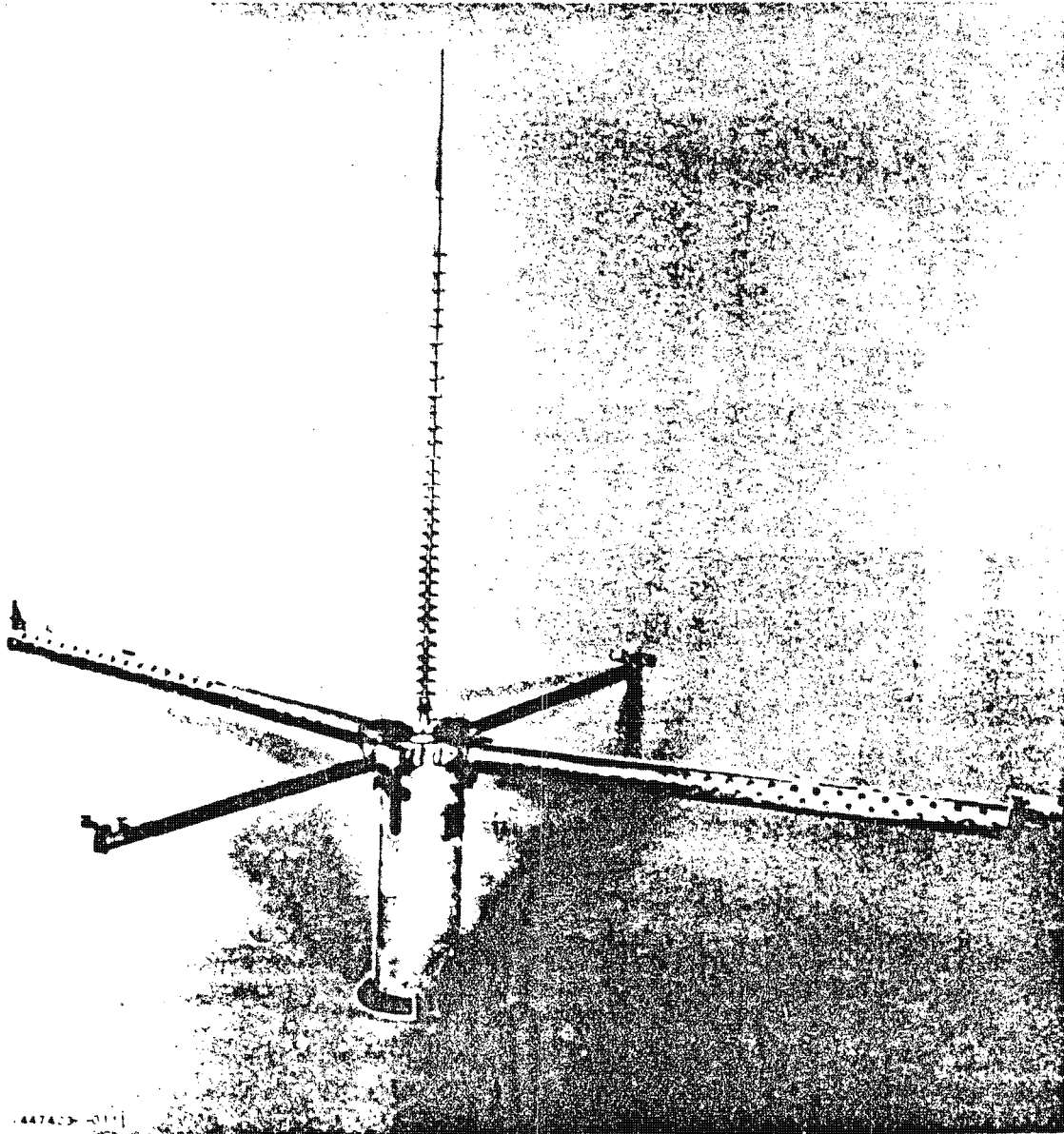
Figure 2-9 Band 3a and Band 1 Antennas in Operating Position

2-11
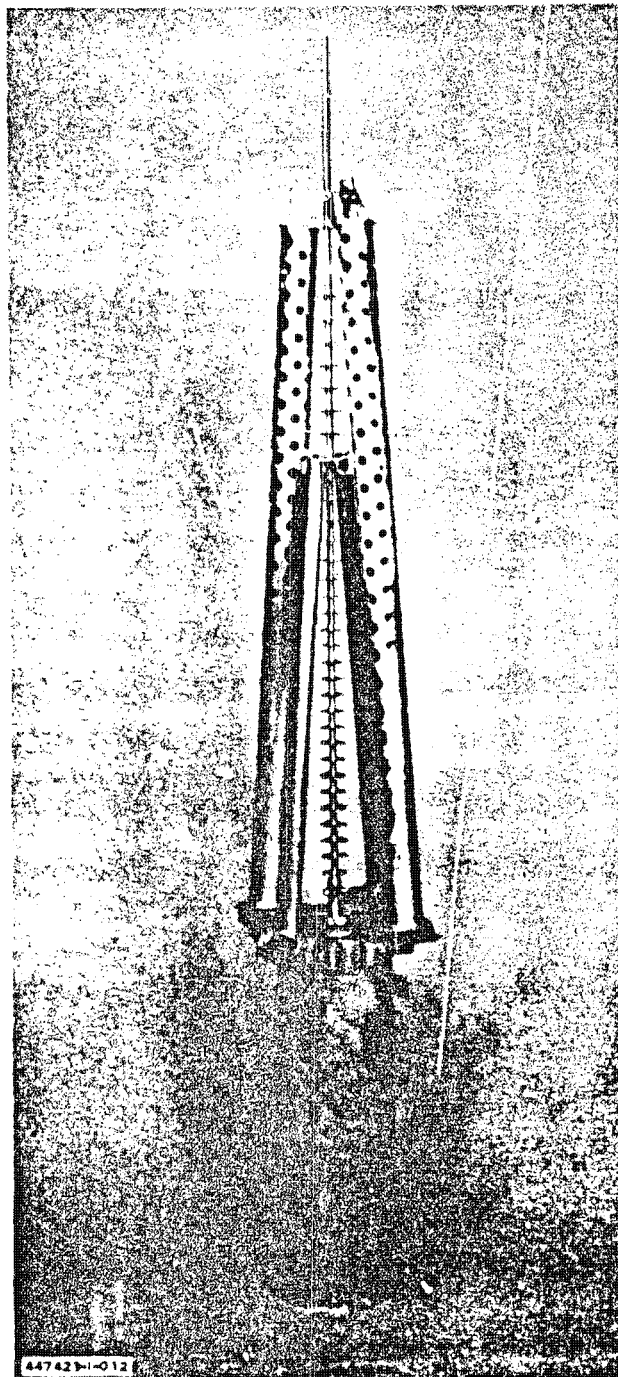
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Figure 2-10 Band 3a and Band 1 Antennas in Packaged Position

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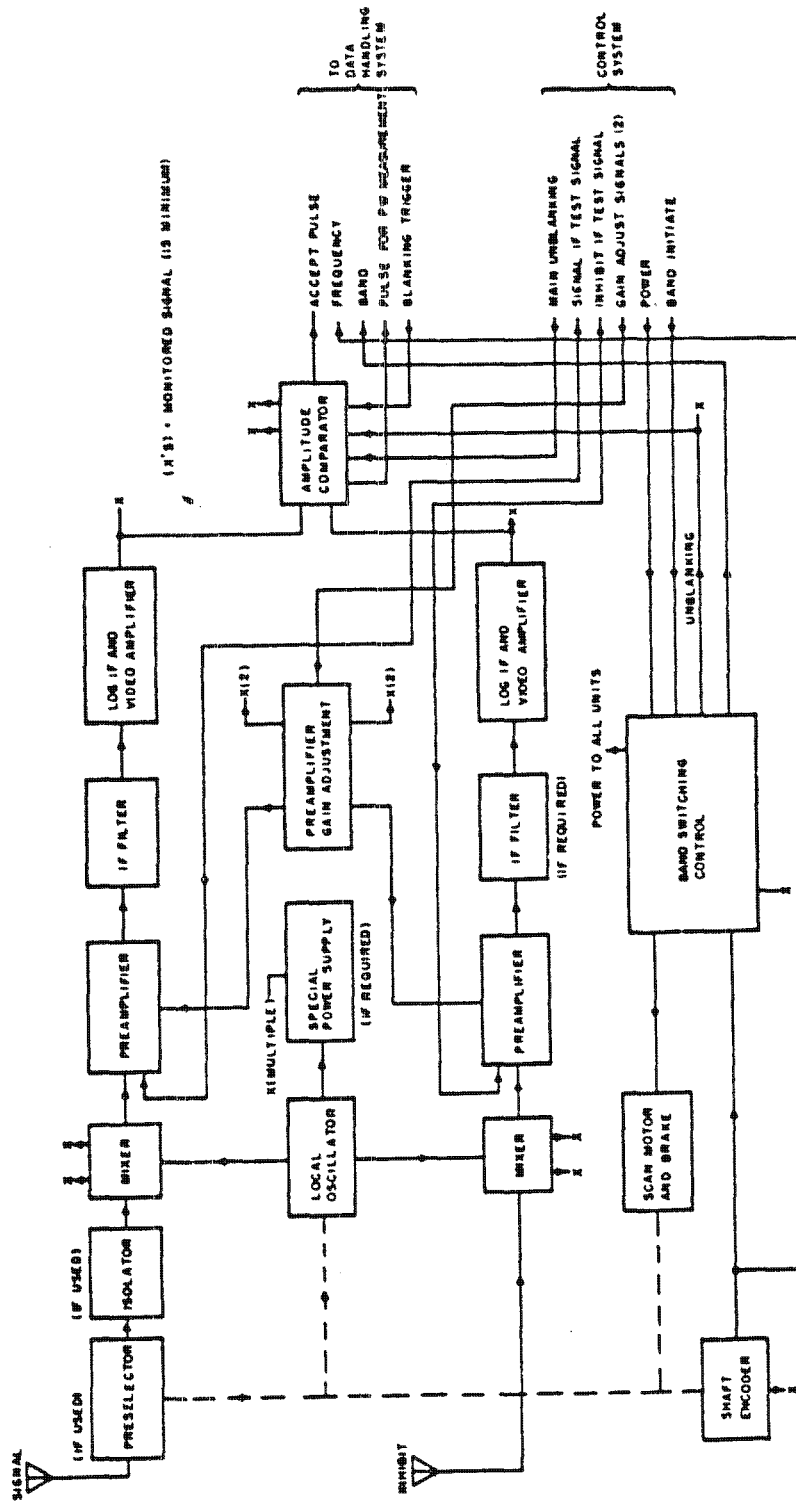
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Figure 2-11 Block Diagram of F-2 (Flts 1, 2) Receivers

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limiting acceptance to signals within the band of interest. A common local oscillator is used for both channels. Each band has a completely independent receiver, with its own front end, IF amplifier, and amplitude comparator. This straightforward receiver design makes the F-2 equipment adaptable to engineering changes and to a wide variety of tactical situations and substantially decreases the probability of total failure of all receivers.

As shown in Figure 2-11, the receiver unit for each band contains all the necessary equipment for passing a standard "accept" pulse and a PW pulse to the data handling circuits. Each payload will be capable of multiband operation. Because frequency bands are scanned serially rather than simultaneously, one limitation on the number of receivers that can be carried is the available scan time. Total scan time cannot exceed 23 seconds without seriously increasing the probability of overlooking an emitter. The scan time of any band is variable within limits that depend upon the minimum PRF that it is desired to intercept and the frequency resolution required. When the minimum PRF and the channel width have been established for a particular frequency band, the minimum scan time for that band is automatically established. All the receivers carried in one payload must have a total scan time of less than 23 seconds if the system is to be effective.

The receiver-introduced limitations on parameter measurements are dependent on the signal channel's IF bandwidth, and the receiver scanning rate. The IF bandwidth must be adequate to pass the minimum PW expected, but it must be kept within the limits set by receiver noise and signal resolution requirements. The scanning rate of the receiver is set so that during one scan at least three pulses can be received at minimum PRF. However, the scanning rate must be fast enough that the entire frequency band is covered during the time that the payload's ground coverage circle moves one coverage radius. Increasing the number of times the same intercept is received (that is, increasing the scan rate) improves the locational accuracy.

The band 1 receiver is shown in Figure 2-12 and the band 2 receiver in Figure 2-13. The receivers operate as follows. Signals from the signal and inhibit antennas are fed to their respective channels; there they are mixed,

2-14
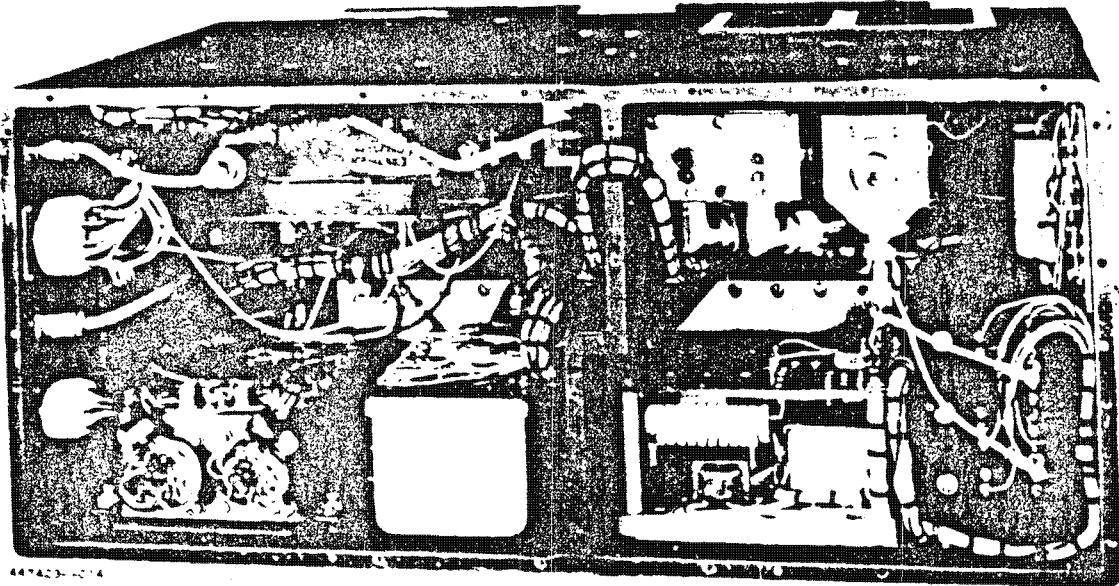
Figure 2-12 Band 1 Receiver
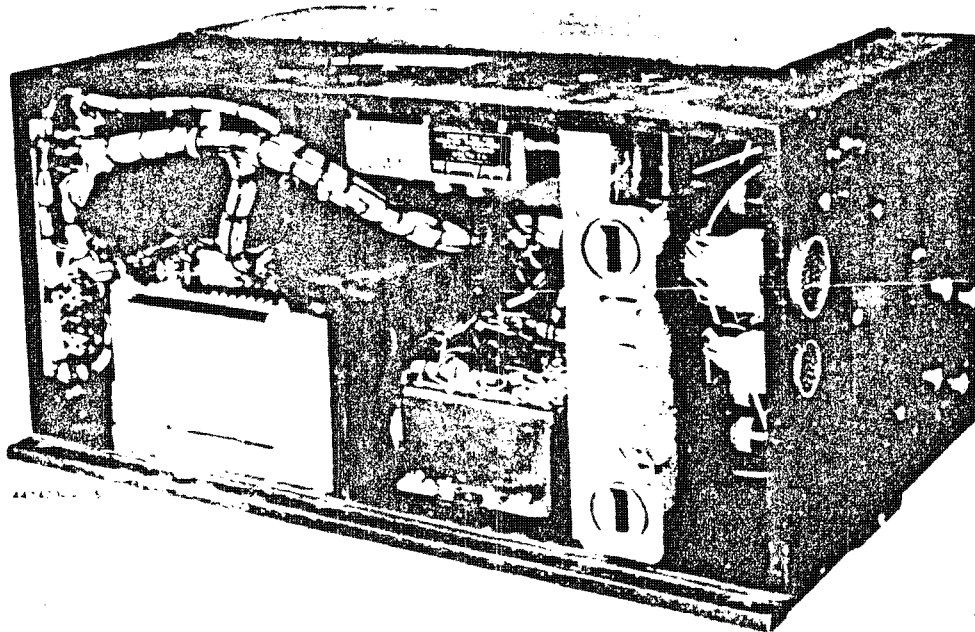
Figure 2-13 Band 2 Receiver

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amplified, detected, amplified further in a video amplifier, then fed to an amplitude comparator. The comparator determines from the relative amplitudes of the two signals whether or not the intercepted signal came from an emitter within the circle of coverage. If the emitter lies within the coverage circle, the amplitude comparator sends two pulses to the data handling circuits - the accept pulse and an amplitude-limited sample of the intercepted pulse. This sample is used for PW measurements.

The receiver threshold sensitivity is -80 dbm; that is, a -80 dbm signal at the input terminals of the receiver will trigger the amplitude comparator 90 percent of the time if the false-alarm rate (noise signal) is less than one per second. The receiver dynamic range is nominally 60 db. Since pre-amplifier linearity is reduced for input power levels above -25 dbm, the actual dynamic range is limited to 55 db to ensure good amplitude tracking.

2.2.1 Preselector

The two principal design objectives for the preselector are: (a) an image attenuation of at least 20 db, and (b) an insertion loss of less than 1.5 db. Since the preselector must track the local oscillator, the bandwidth of the preselector is made as wide as possible. Since there is no preselector in the inhibit channel, spurious signals from that channel are larger than those from the signal channel. The amplitude comparator recognizes this difference and inhibits the output of the receiver when such signals occur. Thus the combined actions of the inhibit channel and the comparator serve as a filter and discriminator against signals that lie outside the pass band of the receiver.

A two-cavity coaxial filter is used in band 1. The preselector bandwidth is 30 Mc. When used with a 60-Mc IF strip, this preselector provides image attenuation greater than 20 db. No preselector is used in band 2. The band 2 receiver will therefore have two responses, one 60 Mc above and the other 60 Mc below the local-oscillator frequency. Twice as many intercepts for each emitter will be obtained as would be recorded if a preselector were used. However, the expected signal density in band 2 is sufficiently low

that doubling the intercept rate will not tax the receiver or data handling capacity. Advantages of omitting the preselector are improved receiver sensitivity and improved reliability.

2.2.2 Local Oscillators

The originally proposed 6299 triode oscillator for use in band 1 has been re- placed with the F-1 klystron oscillator.* Reliable power output distribution and frequency coverage were not obtained with the 6299 units. On this basis a new band 1 oscillator program was initiated. The first step of this pro- gram was to effect an immediate solution to the problem by the substitution of the proven F-1 local oscillator into the F-2 (flts 1, 2) equipment. Several voltage-tunable devices were considered, and the development of a new tri- de oscillator using either a GE 6771 or a GE 6442 tube type was subcon- tracted to ACF Industries. Since the klystron oscillator is proving to be satisfactory, the development program for other oscillators has been discontinued.

In band 2 a VA161 BWO is used, which requires 15 watts of input power at relatively low voltages. This BWO is a rugged unit of ceramic in integral magnetic construction. It is electronically tunable over the required fre- quency range, and its operating frequency setting is sufficiently insensitive to load changes.

2.2.3 Mixers

Because of crystal nonlinearity, any crystal mixer will have a number of spurious responses. The following equation describes the spurious fre- quencies as a function of harmonic order:

$$F_s = \frac{nF_{LO} \pm F_{I-F}}{m}$$

where $n = 1, 2, 3 \ldots$

$m = 1, 2, 3 \ldots$

F_s = Signal frequency

F_{LO} = Local oscillator frequency

F_{I-F} = I-F frequency

*ZV1009

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It can be seen that when m = n spurious responses will occur between the local-oscillator frequency and the signal frequency. Experimental results show that, for either a single-ended or a balanced mixer, the sensitivity for the m = n = 2 case is about 50 db below the sensitivity at the signal frequency (Figure 2-14). To utilize the inhibit action of the receiver, it is necessary to reduce these responses in the signal channel by about 6 db. This can be accomplished easily by preselector attenuation.

To minimize the noise figure and the driving power required for the local oscillator, balanced mixers are used in each band. Balanced mixers reduce the noise figure by canceling local-oscillator noise; this is particularly important at low intermediate frequencies and where a BWO is used as the local oscillator. 1N23EMR crystals will be used for band 2, and 1N21EMR crystals will be used for other bands. The conversion loss (L_c) specification for the 1N21EMR crystals is 3.5 (5 db) and the noise temperature (T) is 1.4 (1.4 db).

If we assume an I-F noise figure of about 3.2 (5 db), the overall noise figure of the receiver (neglecting preselector loss) will be 10.6 db.

$$F = L_c(T + F_{I-F} - 1) = 10.6 \text{ db}$$

The insertion loss of preselector and isolators must be added to this noise figure in the bands and channels in which these components are used. Figure 2-15 shows the receiver sensitivity as a function of overall receiver noise figure and I-F bandwidth.

STRIPLINE* circuits are used as mixers in band 1. Figure 2-16 is a photograph of the STRIPLINE ring junction band 1 mixer. Waveguide circuits are used as mixers in band 2 (Figure 2-17).

2.2.4 I-F Amplifiers

The I-F circuits are divided into three different units: (a) a linear preamplifier, including a gain control and band-limiting filters (Figure 2-18 and 2-19), (b) a logarithmic amplifier (Figures 2-20 and 2-21), and (c) a video

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* Trademark Registered, U.S. Patent Office.

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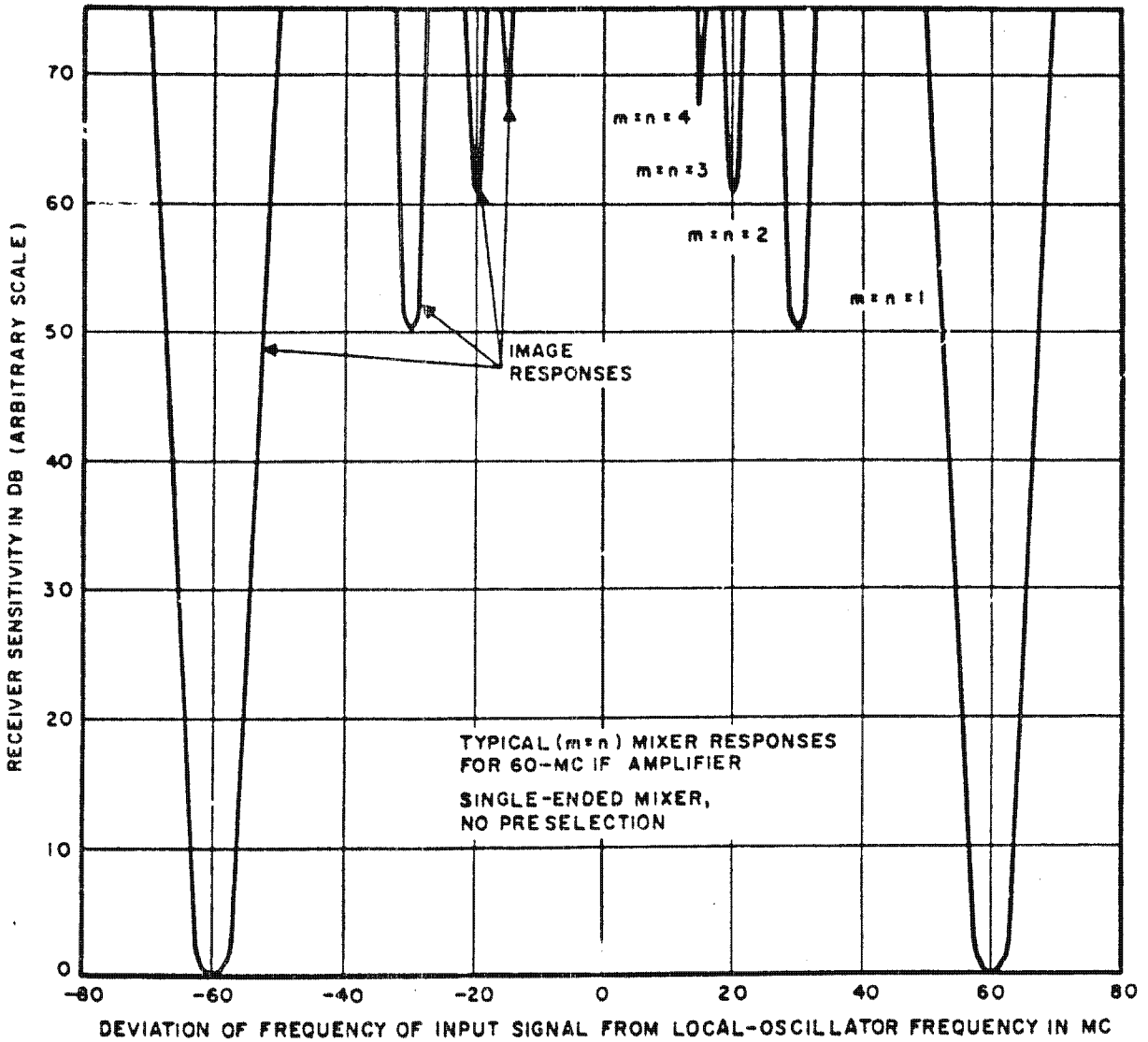
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Figure 2-14 Spurious-Response Characteristics of a Mixer

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SENSITIVITY IS THE INPUT SIGNAL STRENGTH REQUIRED
TO PRODUCE AN IF SIGNAL-TO-NOISE RATIO OF ONE

RECEIVER NOISE FIGURE IN DB

BANDWIDTH IN MC
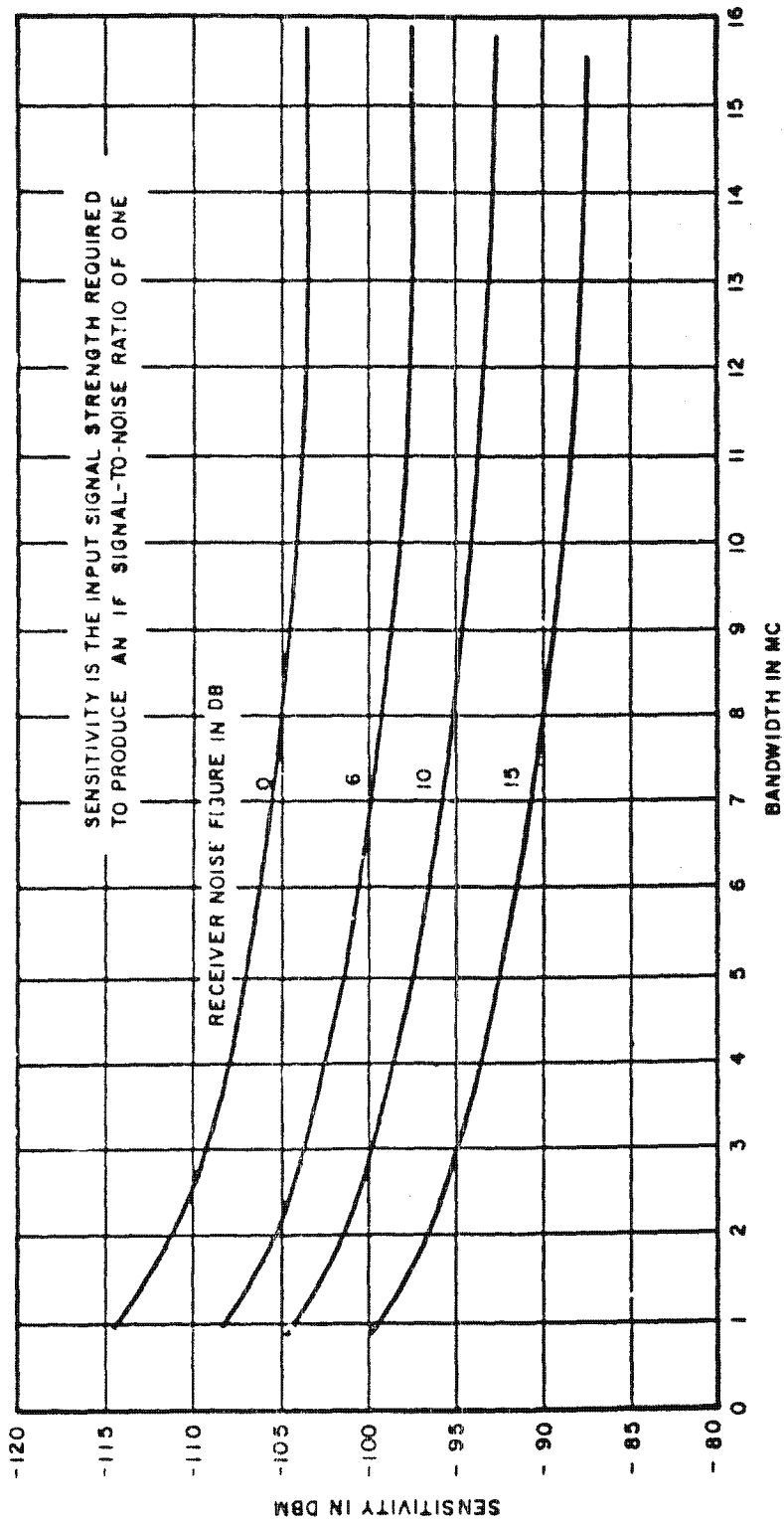
SENSITIVITY IN DBM

Figure 2-15 Receiver Sensitivity

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Figure 2-16 Band 1 Mixer

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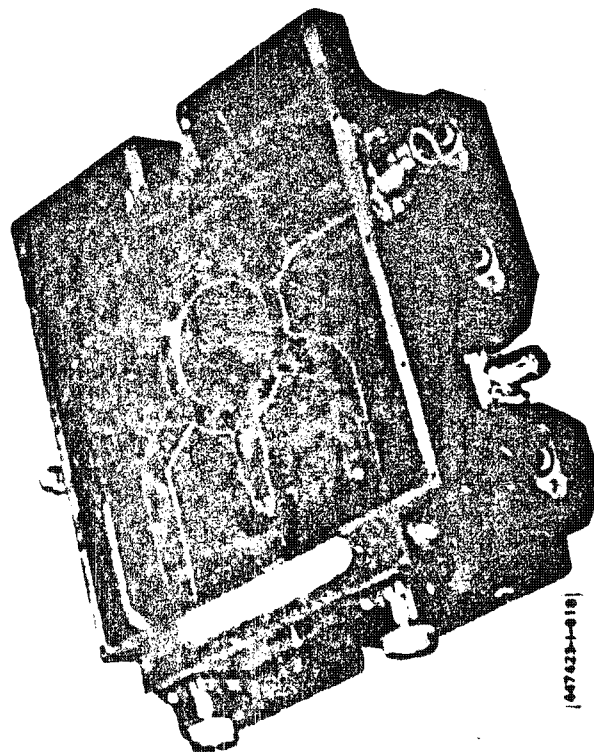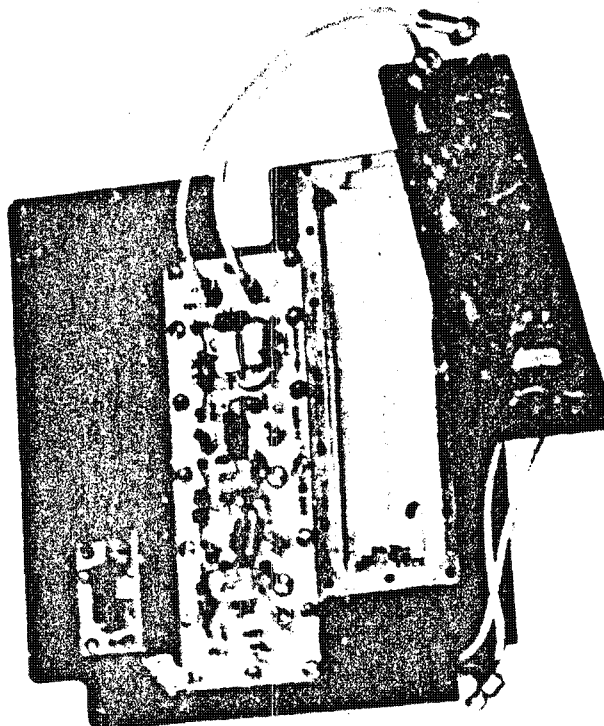
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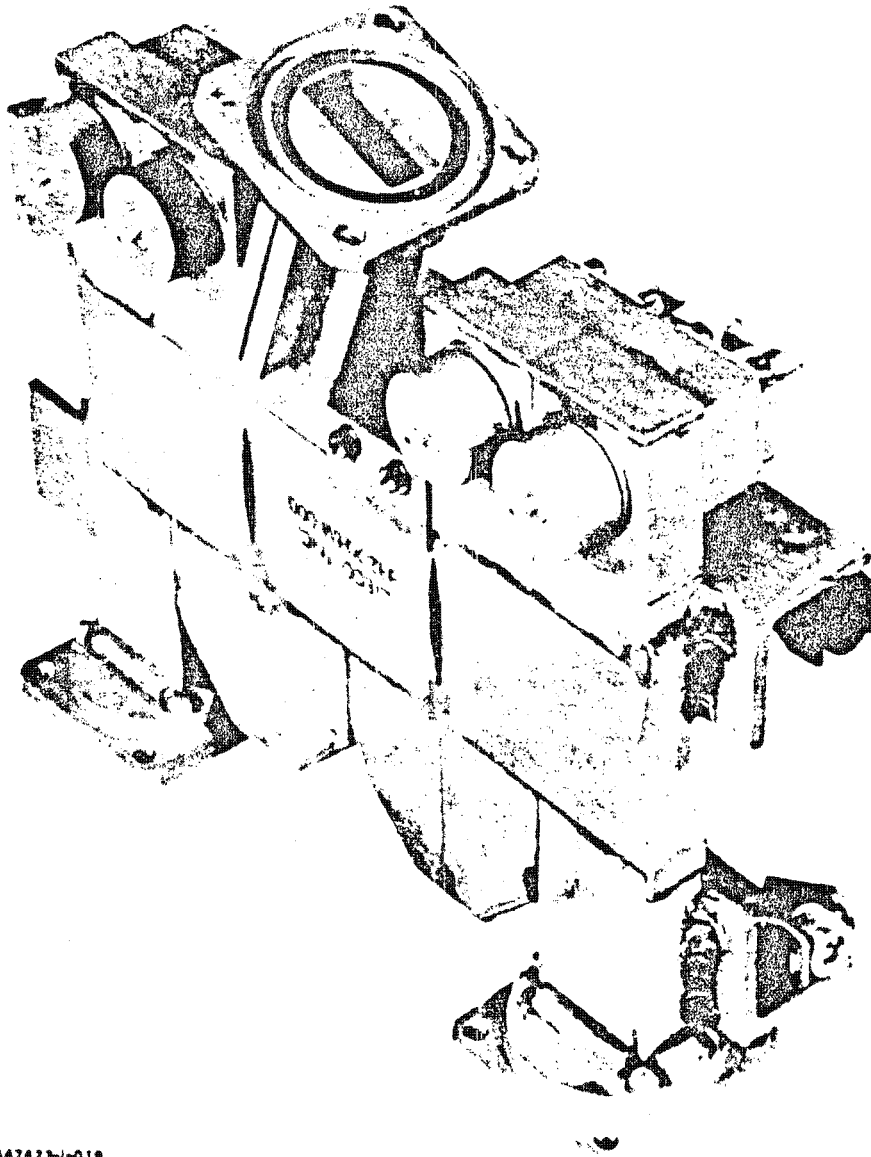
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Figure 2-17 Band 2 Mixer

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Figure 2-18 I-F Preamplifier

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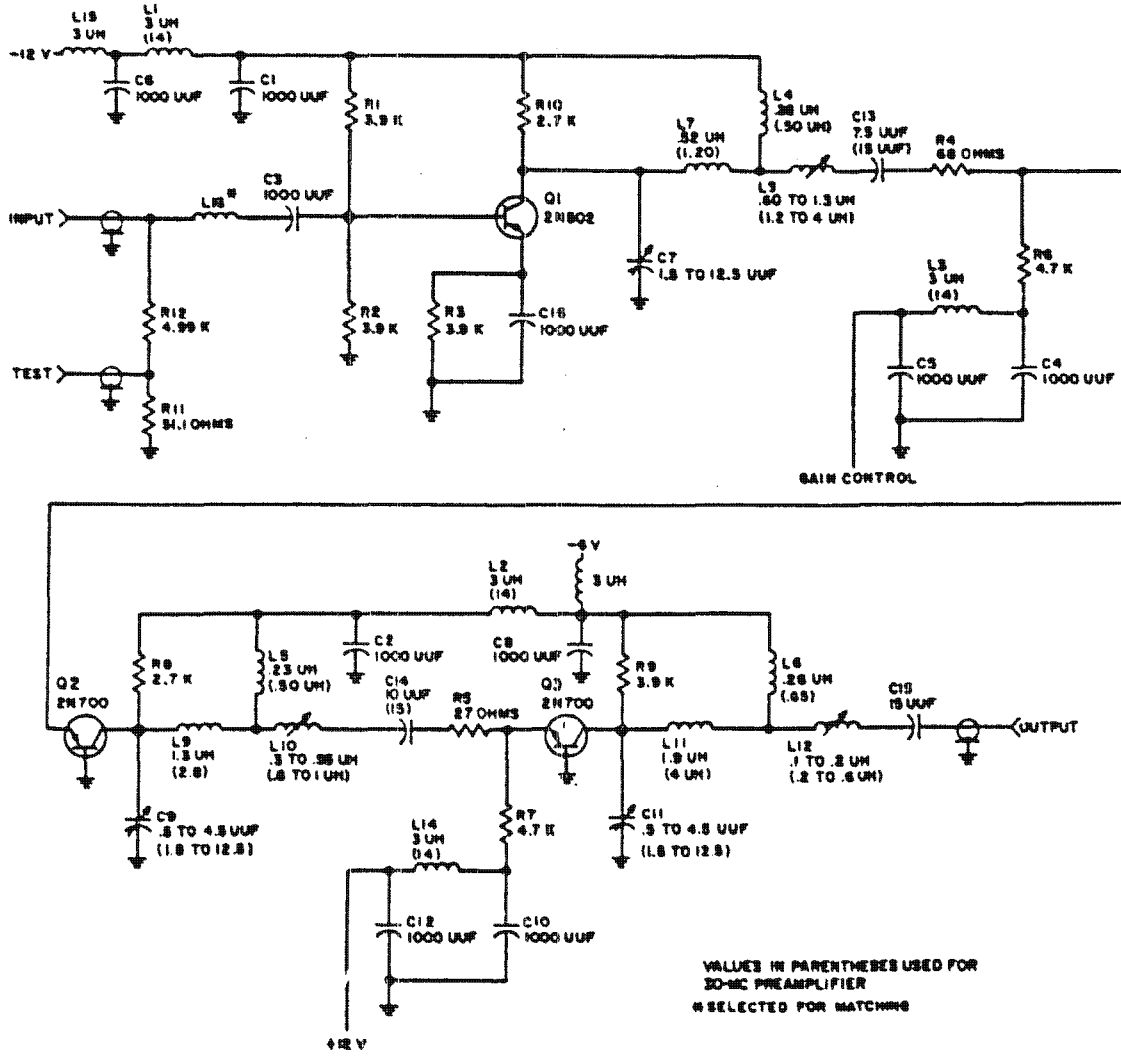
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Figure 2-19 Schematic Diagram of I-F Preamplifier
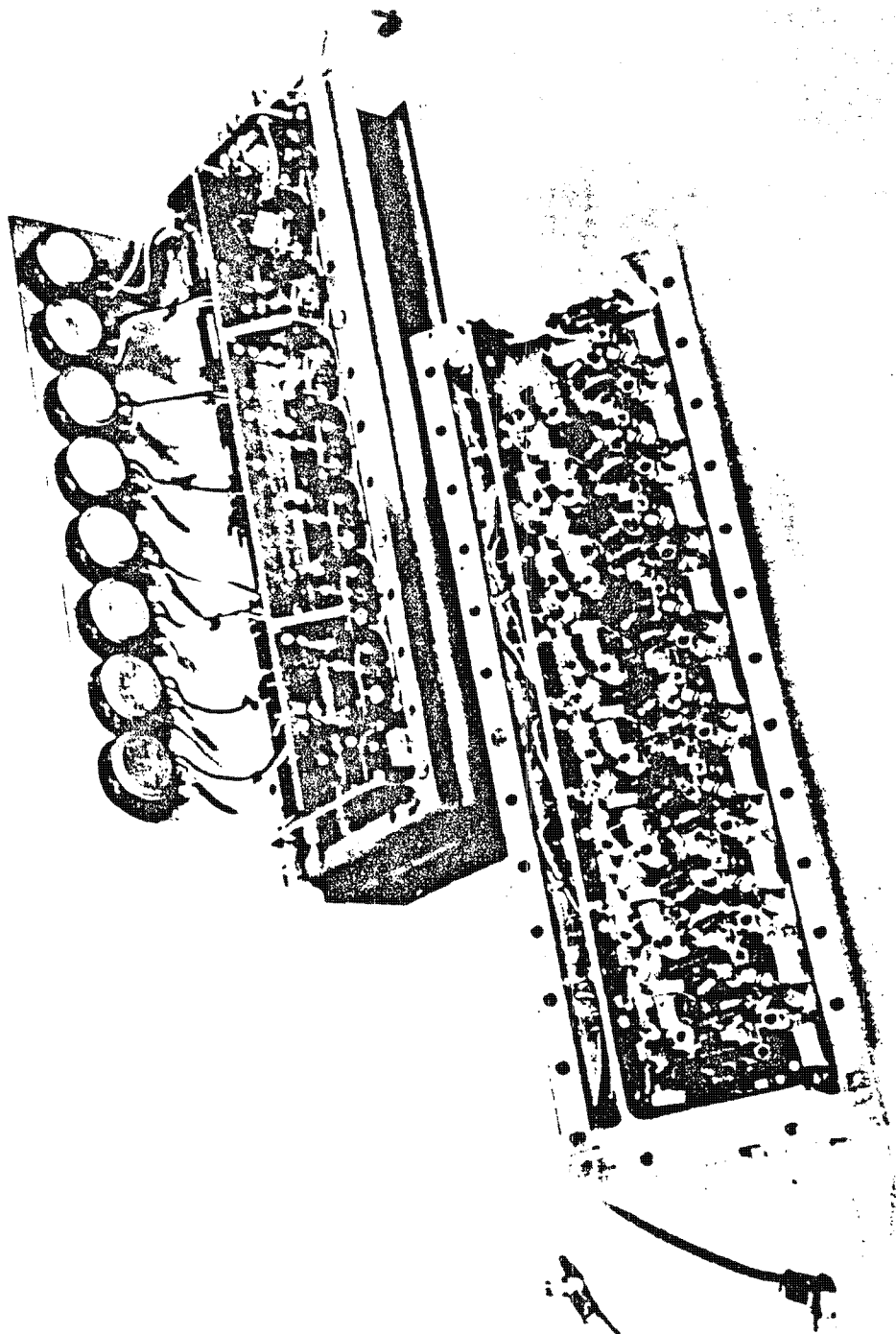
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Figure 2-20 Log I-F Amplifier

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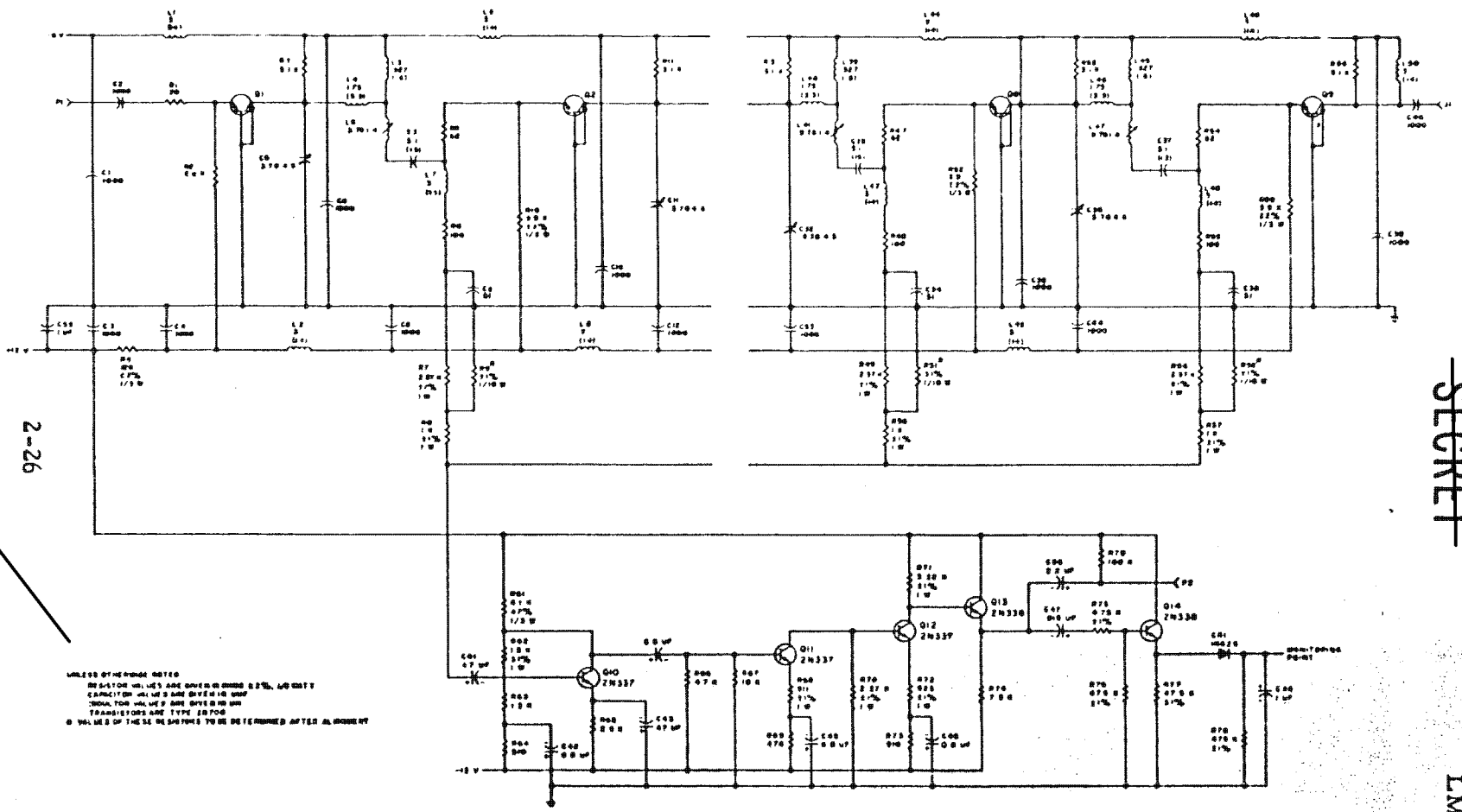
Figure 2-21 Schematic Diagram of Log I-F Amplifier

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amplifier. The logarithmic amplifier and the video amplifier are both included in the log I-F strip.

The dynamic range of the input I-F signal from the mixer may vary in amplitude from about -95 to -35 dbm. The I-F amplifier must have logarithmic characteristics to meet this large dynamic range requirement and to thus ensure that variations in signal levels do not introduce errors on the diameter of the ground coverage circle. Since the amplitude comparator requires an input signal amplitude between 1 and 10 volts, the 60-db dynamic range of the receiver input signal must be compressed to a 20-db dynamic range at the input to the amplitude comparator.

The I-F strips are transistorized to provide maximum reliability and minimum power drain, size, and weight. Consequently the intermediate frequency must be low enough so that transistors can be used successfully. On the other hand, it is desirable to use a high intermediate frequency so that the image response can be separated as far as possible from the signal band (to ease preselector tracking problems). A 60-Mc intermediate frequency is used.

In the logarithmic I-F amplifier, the technique of successive detection is used to obtain a large dynamic range. A small detected signal is extracted from each interstage, and all of the signals thus detected are added in a resistive network. The output of the summing network is fed to a video amplifier, whose output is a video signal with an amplitude that is proportional to the logarithm of the input signal.

An eight-stage 8-Mc-wide, double-tuned, common-base circuit is used for the successive detection. The nonlinear input impednace of a transistor in the common-base circuit performs the actual detection function. The output of the I-F portion of the circuit ranges from 2 to 20 mv for input signals from -70 to -10 dbm; within this range, the output is logarithmic to within 0.2 mv. The video amplifier provides linear amplification, and its output amplitude will range up to 10 v.

The 2N700A transistor was selected for this application because of its ability to operate at high frequency, its uniform characteristics, and its rugged construction.

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Channel bandwidths are controlled by passive filters following the preamplifiers; thus the 60-Mc log I-F strips, which have an 8-Mc bandwidth, can be used interchangeably in all bands. The preamplifier gain control has a range of 10 db. In all but two channels, the I-F bandwidths are fixed by means of filters. The I-F band-pass characteristics are tabulated in Table 2-1.

2.2.5 Amplitude Comparator

The amplitude comparator (Figures 2-22 and 2-23) determines whether an intercepted signal originates within the desired region of coverage of the antenna system. It accomplishes this by comparing the amplitudes of the video pulses from the signal and inhibit channels. A difference bias determines the amount by which the amplitude of the signal-input pulse must exceed that of the inhibit-input pulse to produce a signal accept condition.

The positive signal channel-input pulse and inhibit channel-input pulse are received at the bases of Q1 and Q9, respectively, where they are superimposed upon present quiescent DC levels. These DC levels determine the normal back bias on the base-emitter junction of Q2, the comparator stage. When the signal pulse exceeds the inhibit pulse by the difference bias (difference between present DC levels plus Q2 base-emitter voltage drop) Q2 conducts. The output of Q2 is amplified and triggers the blocking oscillator, Q5 via Q4. The blocking oscillator fires, establishing an accept pulse. To establish the existence of a valid intercept, two accept pulses are required by the verifier circuit in the data handler.

Transistors Q6 and Q7 form a monostable multivibrator, and Q8 is a blanking switch. They blank the blocking oscillator after each valid intercept, thus allowing the receiver data to be processed. Provision has also been included to blank the amplitude comparator on command directly through Q8.

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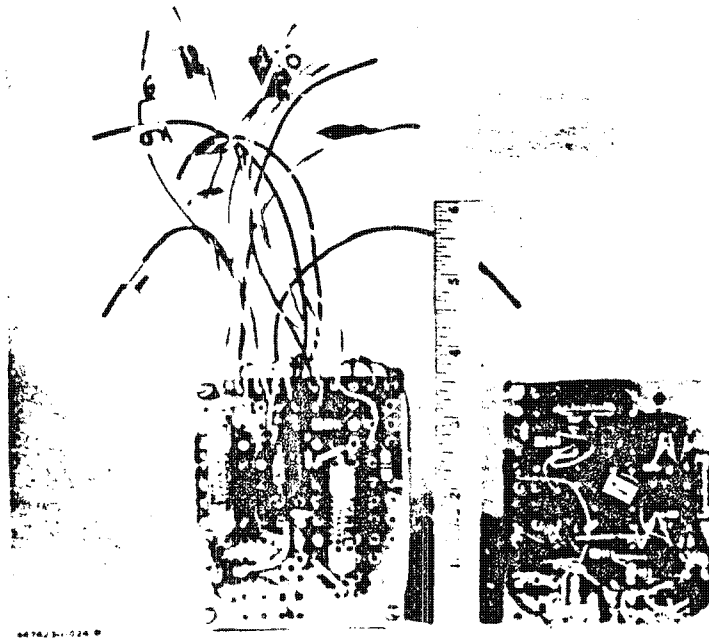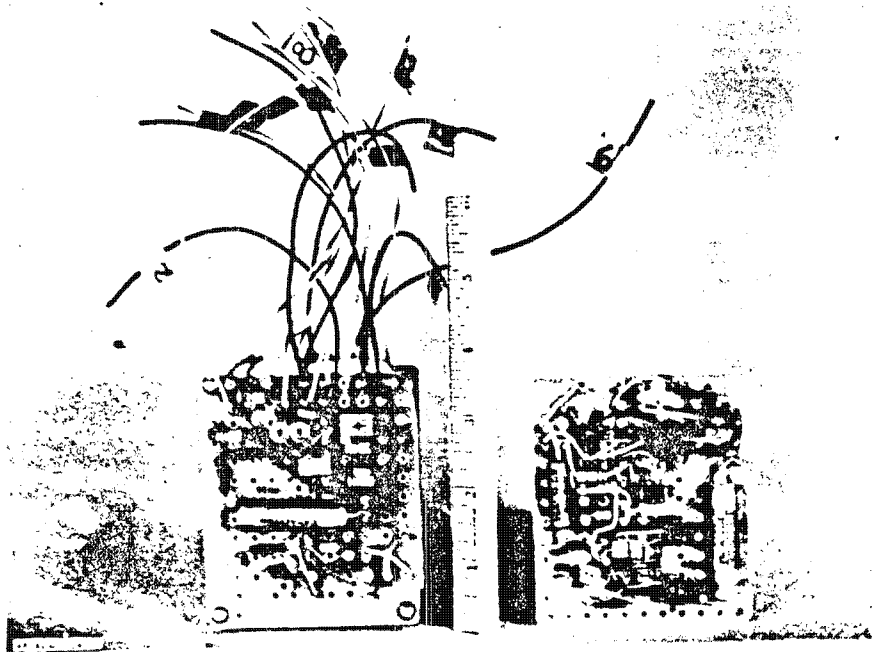
Figure 2-22 Amplitude Comparator

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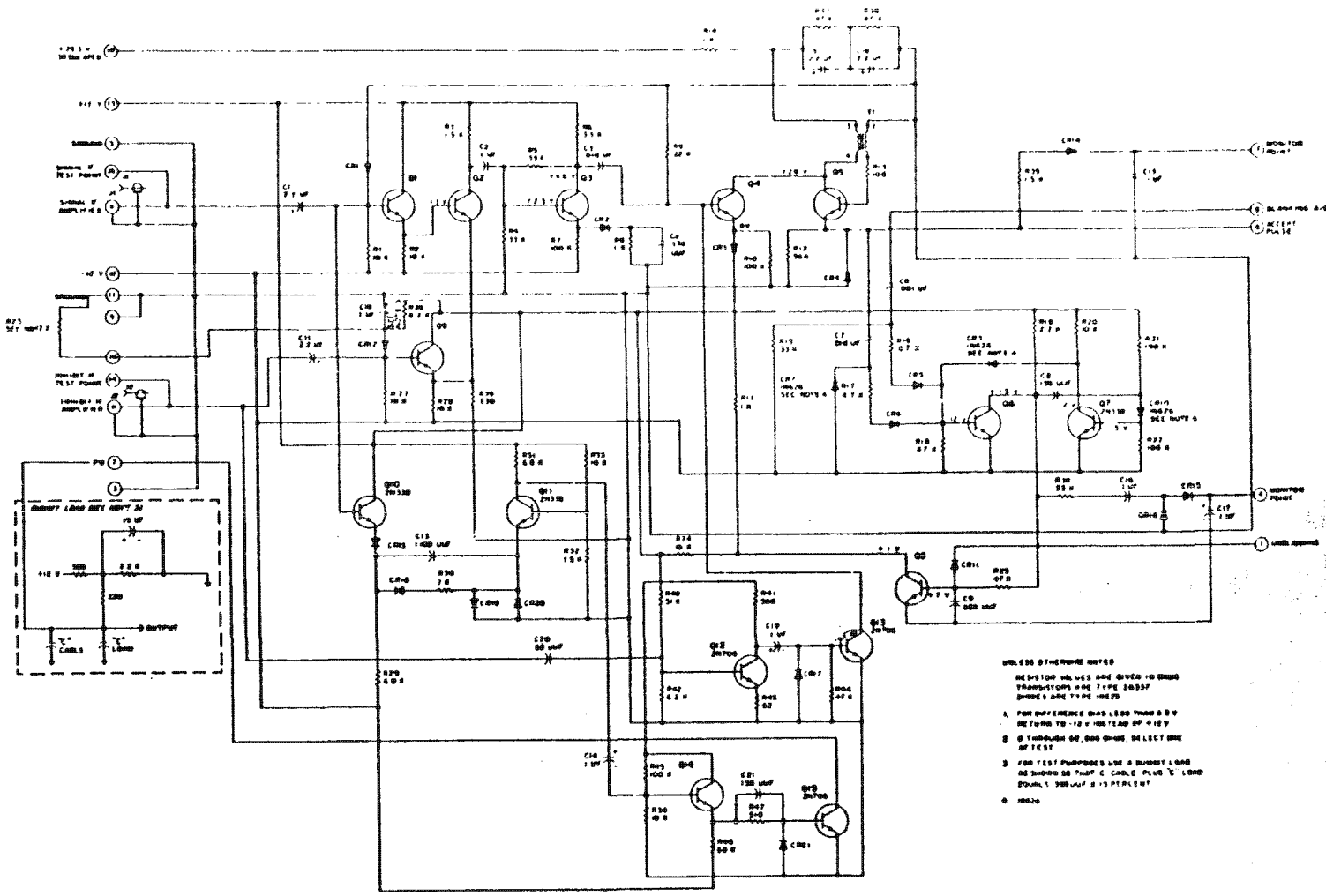
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Figure 2-23 Schematic Diagram of Amplitude Comparator

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Table 2-1

I-F AMPLIFIER BAND-PASS CHARACTERITSTICS FOR F-2 (FLTS 1, 2)

	Center Frequency (Mc)	3-db Bandwidth (Mc)	60-db Bandwidth (Mc)
Band 1 Signal	60 ± 0.4	2.5 ± 0.2	$6.5 + 1.5 - 1.0$
Band 1 Inhibit	60 ± 0.4	4.0 ± 0.3	$14.0 + 2.0 - 1.0$
Band 2 Signal	60 ± 0.4	5.0 ± 0.2	$12.5 + 3.0 - 2.0$
Band 2 Inhibit	60 ± 0.5	7 minimum*	

* No filters used in this channel. Values shown are for input signal of -40 dbm.

Since the I-F bandwidths of the signal channel and inhibit channel are not the same, incorrect comparisons would result at the trailing edges of the video pulses. To prevent this, Q12 and Q13 generate a disabling pulse at the end of the shorter inhibit video pulse. This prevents the blocking oscillator signal from appearing at the time when the delayed signal video is present. Q10, Q11, and Q15 reshape the signal video pulse to drive the data handler PW oscillator with a constant voltage from a low impedance source. The PW circuit limits stretching to less than 0.5 μsec under worst case conditions. The signal characteristics of the amplitude comparator are:

Input PW	0.5 to 31.5 usec
Output PW	0.6 to 32 usec
Input pulse amplitude	1 to 10 volts
Difference bias adjustments	0.5 to 1.5 volts (3 db to 10 db)
Accept PW	maximum: 9 μsec minimum: 3 μsec
Accept pulse amplitude	12 ±1 volts

2.2.6 Receiver Power Supplies

2.2.6.1 Band 1 Power Supply. To incorporate the F-1 klystron oscillator into the F-2 (flts 1, 2) equipment it was necessary to change the band 1 power supply. The input requirements remain as 115 v, 2 kc. The output voltages are:

a. 500 v dc regulated ±5 percent

b. 300 v dc regulated ±5 percent

c. 6.3 v, 2 kc nonregulated

Regulation is achieved by a transistorized amplifier sensing the output voltage error and driving a low-gain magnetic amplifier control winding to oppose the error. Full wave rectification is used to minimize the filtering. The entire unit is encapsulated in solid epoxy.

2.2.6.2 Band 2 Power Supply. The band 2 local oscillator is a VA161 voltage-tunable BWO. The frequency coverage is from 9 to 10 kmc; this range requires a normal 200 to 300 v sweep of anode voltage. This anode voltage and the BWO bias voltage power supply operates from 115-v, 2-kc power. The requirements for the supply for band 2 operation, assuming an overall accuracy of 1 percent, overall stability of 0.25 percent, and a maximum frequency deviation of 100 kc due to power supply ripple, are shown in Table 2-2.

A schematic diagram of the band 2 power supply is shown in Figure 2-24. Two outputs are provided from the power transformer. One output provides up to 50 v dc at 5 milliamperes, which is used for grid voltage. The other provides 320 v at 20 milliamperes and is regulated before being applied to the anode. Diodes CR3 and CR6 constitute a bridge rectifier. A capacitor input filter is used for ripple reduction.

Table 2-2

BAND 2 POWER SUPPLY CHARACTERISTICS

Parameter	Magnitude (volts)	Accuracy (percent)	Stability (percent)	Ripple (millivolts)
Input Voltage	115 ac	±5	-	-
Anode Voltage	200 to 300 dc nominal	±2*	±0.67*	5
Grid Voltage	up to 50 dc	+5	-	10

*Percentage of maximum voltage.

Regulation is achieved by the use of a differential amplifier controlling series transistors. Transistor Q1 is controlled by the difference between the reference voltage (VR1 and VR2) and the voltage from the output voltage divider (R6, R7, and R8) The collector current of Q1 flows through resistors R5 and R6. The voltage drop across these resistors, which are effectively in series with the output, controls the output voltage. Transistors Q3 and Q5 divide the total voltage drop; Q2 and Q4 are current amplifiers. Stability of the regulator depends on the stability of the voltage reference tubes and the output divider (R6, R7, and R8). The reference element is a 6308 cold-cathode, gas-filled, glow-discharge tube. R6 and R8 are metal-film resistors with temperature coefficients matched to potentiometer R7 which is used to control the output from 200 to 300 v. The sensitivity of the VA161 BWO to change in bias voltage is such that no grid voltage regulation is required A simple full-wave bridge is used in the output with a resistor-capacitor network for filtering.

Since the grid current is constant over the frequency band, voltage adjustment can be accomplished by means of a series dropping resistor. Voltage adjustment is needed to fix the power output of the BWO at the proper value.

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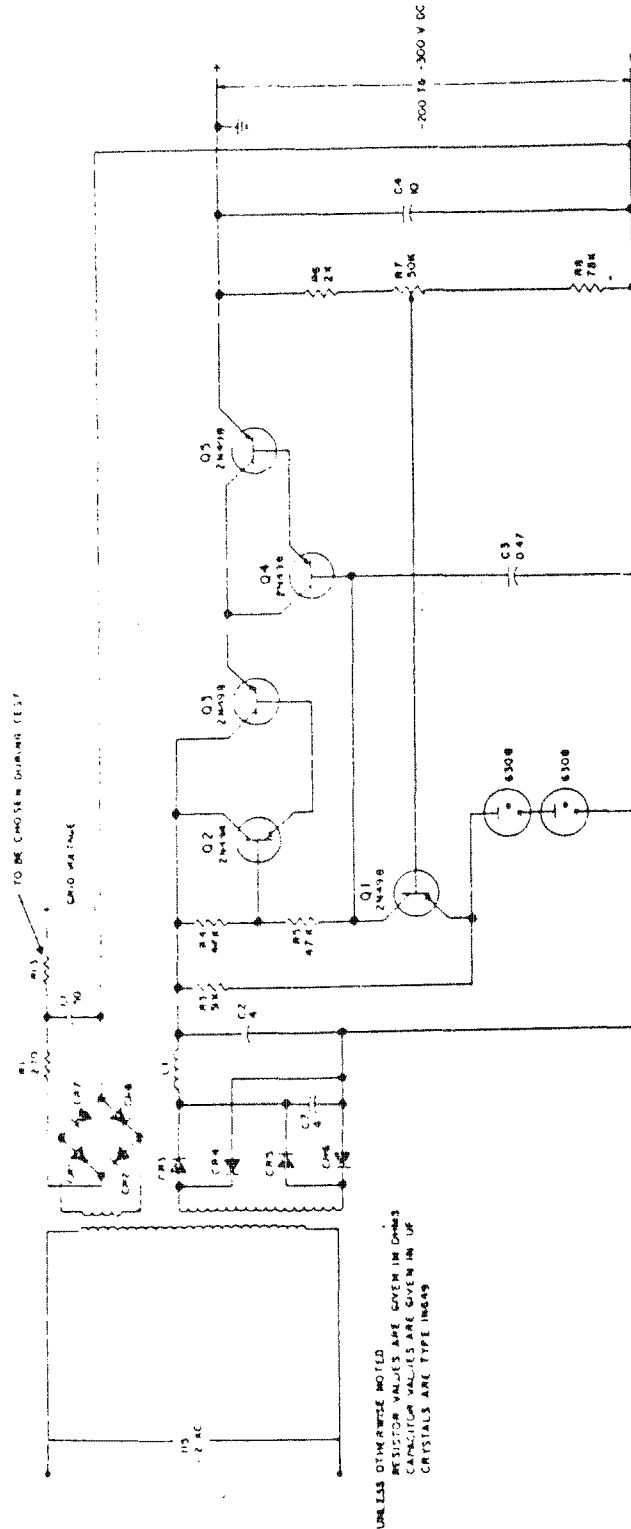
Figure 2-24 Schematic Diagram of Band 2 Power Supply

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2.2.6.3 Filament Transformers. Bands 1 and 2 receivers required the following filament transformer characteristics:

Input Voltage	115 v, 2 kc
Output Voltage	Band 1 6.3 v ac at 0.68 ampere
	Band 2: 9.0 v ac at 1.0 ampere

Initial surge currents are limted by using transformers with magnetic shunts.

2.2.7 Frequency Encoder

Each receiver contains a 9-bit gray code shaft encoder that is geared to the receiver frequency scan drive mechanism. Rotation of the drive shaft is proportional to the receiver frequency. The shaft encoder is used in such a manner that channel information is in one's-complement-gray-code form. Errors that might result from reading out of the code wheel position during rotation are minimized by the use of a gray code in which only one bit changes at a time, when going from one channel number to the next higher number. The 9-bit encoder will accommodate 512 frequency channels. Since the number of I-F channels is 280 in band 1, and 200 in band 2, the encoder provides adequate capacity.

2.2.8 Band Switch Control

The receiver band switch control unit is a portion of the system control and has the following functions in each receiver:

a. Starts the scan motor on command from the system repeat cycle timer

b. Supplies power to the receivers

c. Blanks and unblanks the receiver's output at exact times in the scan sequence

d. Identifies which receiver is on

e. Stops the scan motor

To accomplish the above functions the band switch control unit recognizes start and stop commands from the repeat cycle timer and specific binary

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numbers from the shaft encoder. Paragraph 2.5.8.2 in this section gives the detailed sequence of this timing operation.

2.3 PAYLOAD DATA HANDLER

The payload data handler is a transistorized digital device that performs the data handling function required in the ferret equipment. By examining the video pulses issued by the ferret receivers the data handler (a) determines the acceptability of these signals (verification), (b) analyzes the signals for period between pulses (PRF), and (c) measures the PW of the signal. The data handler also reads out the frequency channel codes from the receivers' shaft encoders and notes the time of intercept. All of this information is expressed in digital form.

As shown in the block diagram in Figure 2-25, the data handler is divided into four sections which are described briefly in the following paragraphs.

a. Verification, PRF, and PW Measurement - This section determines whether the signal received is a valid intercept. If the signal is a valid intercept, this section generates binary words representing PW and PRF, more correctly, pulse interval. The logic diagram of this section is shown in Figure 2-26.

b. Frequency and Time - For each intercept this section performs readout of time, readout of frequency shaft encoders, and readout of band code matrix. The logic diagram is shown in Figure 2-27.

c. Data Interrogation - This section causes the stored binary data in the circuit preceding it to be read out into the recording circuits in serial order. The logic diagram is shown in Figure 2-28.

d. Recorder Control - This section controls the start-record-stop cycles of the recorder, and it shapes, combines, and distributes data pulses going to and from the recorder. The logic diagram is shown in Figure 2-29.

2.3.1 Operation of Verification

Accept pulses from the amplitude comparator are subjected to a verification test before their characteristics are recorded. This test is necessary to prevent the noise pulses that will occasionally be present in the receivers,

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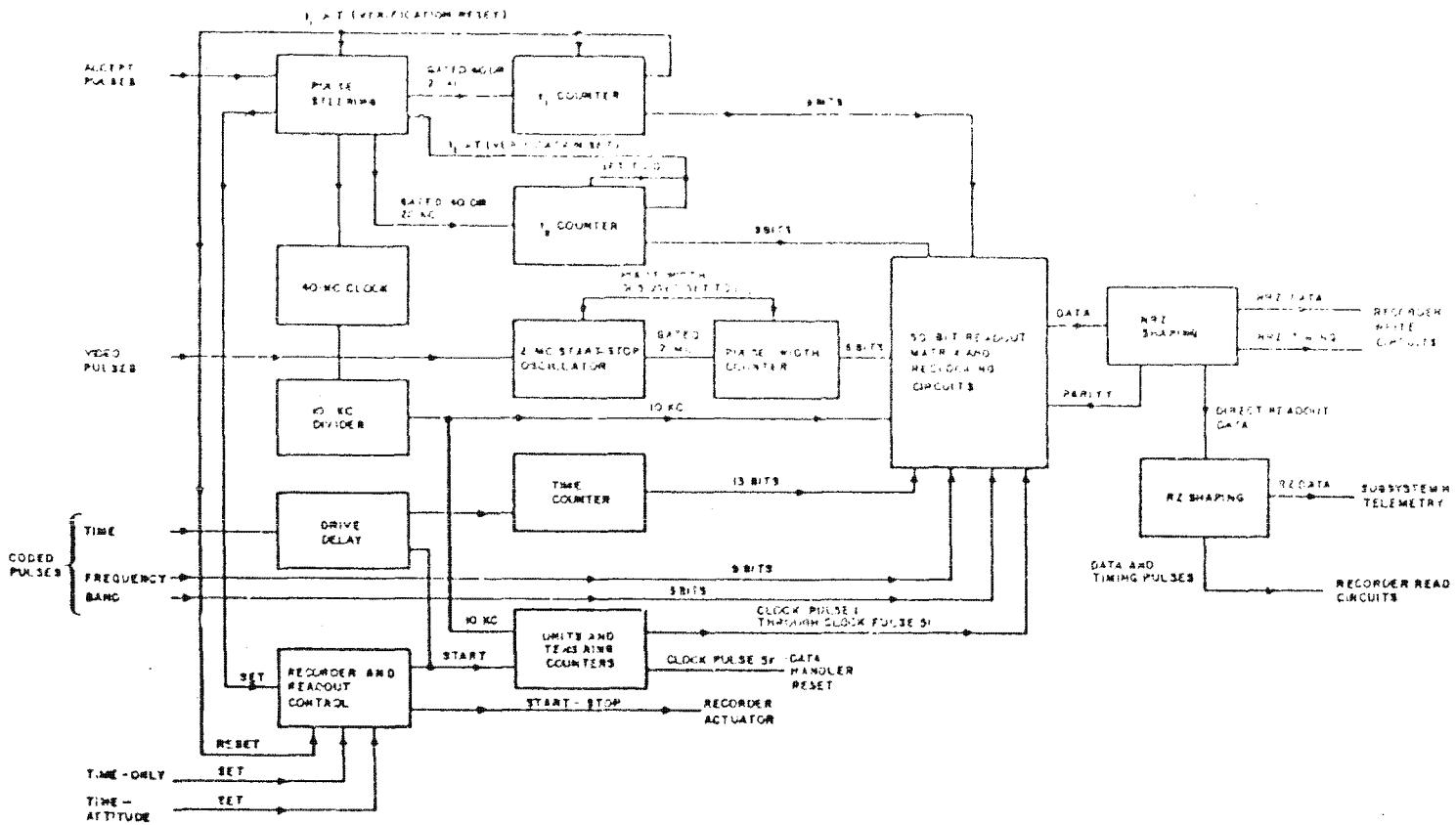
Figure 2-25 Block Diagram of Payload Data Handler

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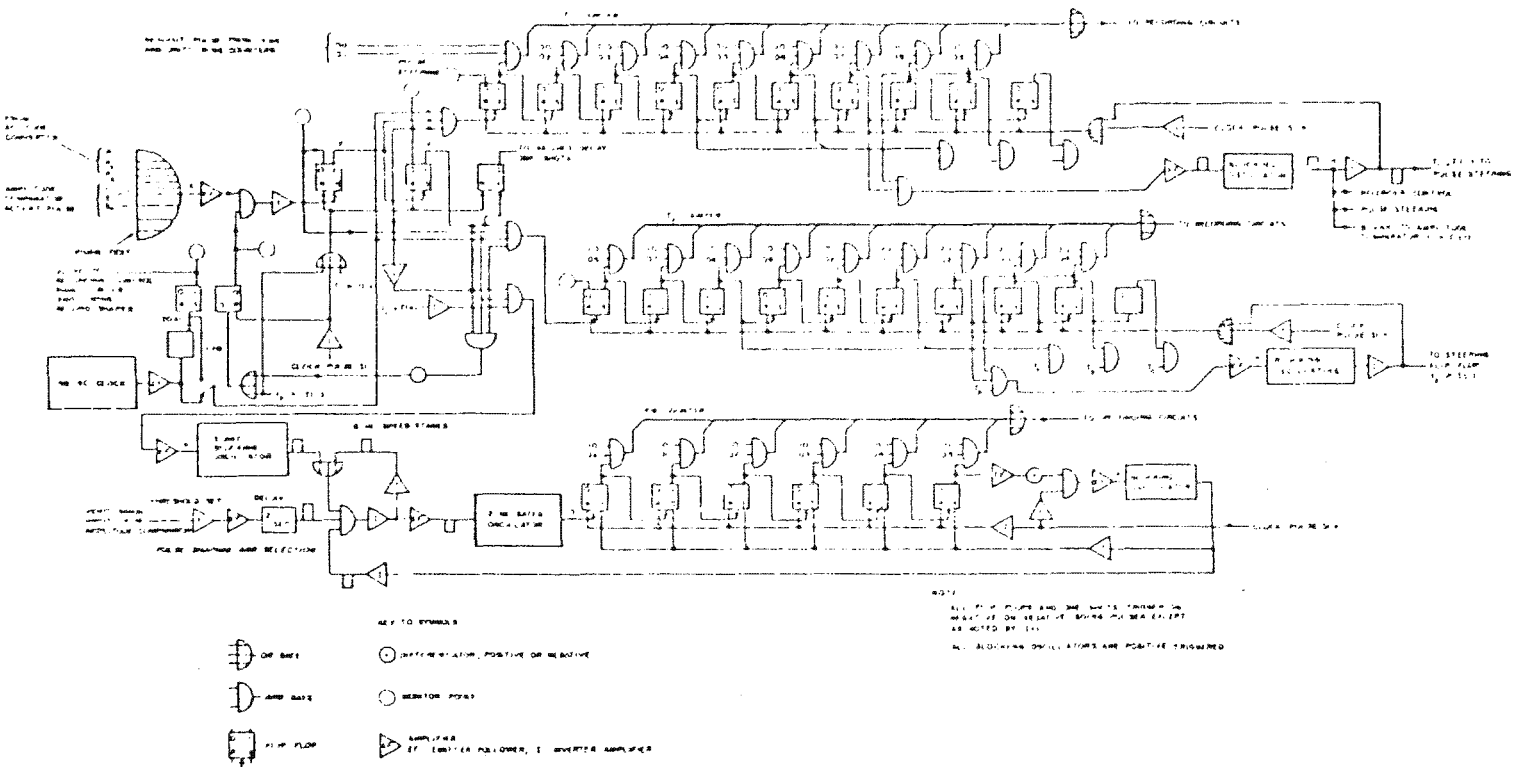
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Figure 2-26 Logic Diagram: Verification, PRF and PW
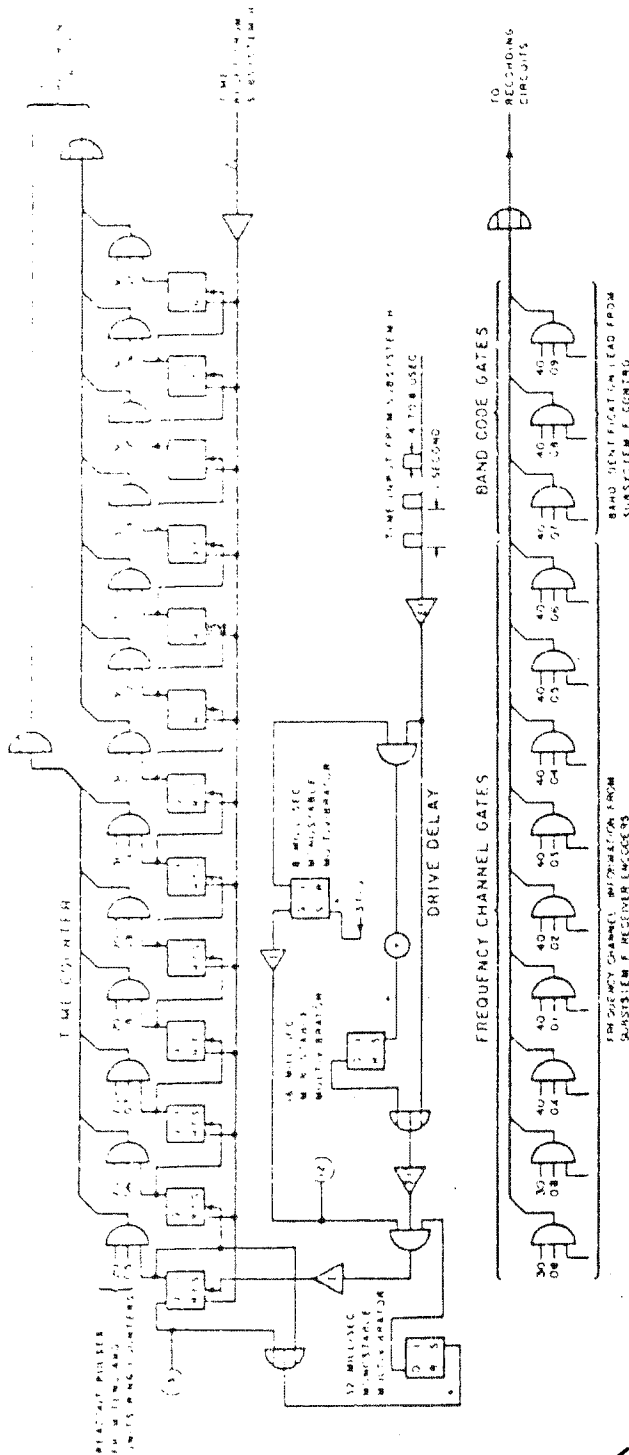
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Figure 2-27 Logic Diagram: Frequency and Time

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Figure 2-28 Logic Diagram: Data Interrogation

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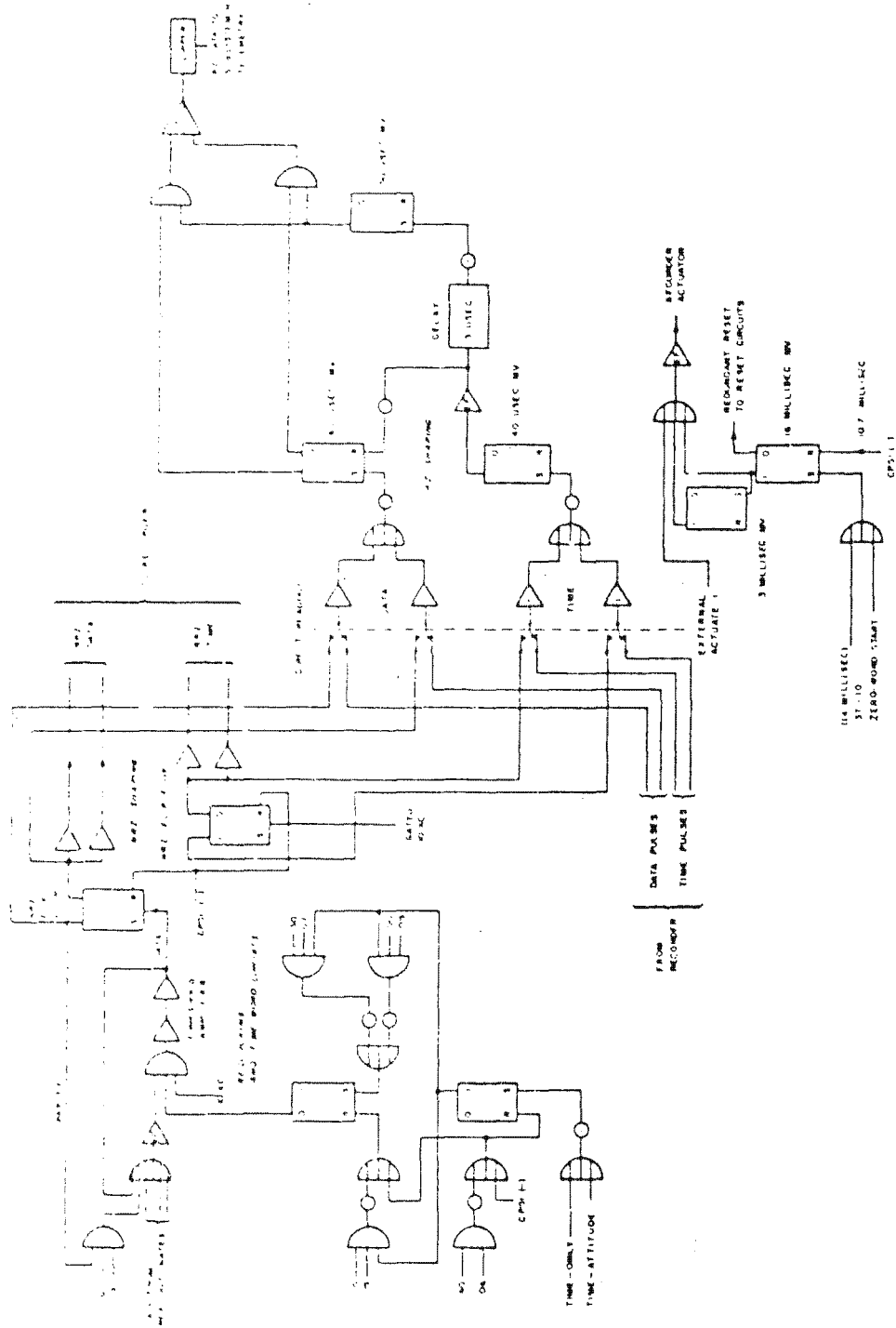
Figure 2-29 Logic Diagram: Recorder Control

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from being considered as received radar pulses. For a signal to be re-
corded as an intercept, at least two pulses must be received with a period
of time equal to the longest interpulse period expected in the particular band
under investigation. The maximum interpulse period expected and allowed
for in each band is 8 milliseconds. If a received signal is not verified, the
data handler is reset and made ready to accept the next signal.

2.3.2 Measurement Cycle

The measurement cycle includes the measurement of the interval between
the first and second pulses, the interval between the second and third pulses,
and the PW of the second pulse. Two pulse interval measurements are made
so that the presence of two or more radars or PRF modulation can be de-
tected. The PRF measurement reliability is also increased by the use of
two counters. The PW of the second pulse is measured so that the pulse
distortions at the edges of the pass band will have minimum effect on the
measurement.

2.3.3 Readout Cycle

The data handler's readout cycle includes the interrogation of both of the
PRF counters, the PW counter, the time counter, the frequency channel
shaft encoders, and the band indication matrix; the serialization of these
data; and the reset of the measurement and verification circuits. A
parity-check bit is generated at the end of this process, and it appears at
the end of the data. After an intercept has been verified, the recorder is
instructed to start and is permitted to reach proper recording speed. Then,
the data are read out and sent to the recorder's write circuits. When the
readout process is completed, the entire data handler is cleared. Although
the time counter is in the data handler, it is controlled by the satellite clock
and continuously provides satellite time. The frequency encoders and the
band code matrix are located in the receivers and in the power and control
assembly, respectively. They provide continuous frequency and band
information to the data handler.

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2.3.4 Measurement Information

2.3.4.1 PRF (9 bits):

Minimum PRF (pps)	125
Maximum PRF (pps)	40,000
Quantum (μsec)	25
Accuracy (μsec)	± 25

2.3.4.2 PW (6 bits):

Counter Capacity	0 to 31.5 μsec
Accuracy	5 percent and ± 0.5 μsec
Quantum	0.5 μsec

2.3.4.3 Time (13 bits):

Counter Capacity	8192 counts
Accuracy	+0, -1 count
Quantum	1 second

2.3.4.4 Data Format.

The data handler issues information in the following order to the tape recorder of the data link. All the data are furnished in a straight binary code except for frequency data, which are read out in one's-complement-gray-code. The bit numbers increase as significance increases.

Bits	Parameter
1 to 9	PRF-1 (t_1)
10 to 15	PW
16 to 24	PRF-2 (t_2)
25 to 37	Time
38 to 46	Frequency (channel number)
47 to 49	Band
50	Parity

2.3.4.5 Cycle Time.

Cycle time is defined as the time between receipt of the first accept pulse and the end of the recording process. In the F-2 (Flts 1, 2) equipment, it is 24 milliseconds.

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2.3.5 Operation During a Typical Intercept

Figure 2-30 contains timing diagrams for the payload data handling system.
The first pulse of the pulse sequence enters the pulse steering circuit, which
is a two-stage binary counter. Entry of a pulse into the pulse steering cir-
cuit opens a gate that permits the continuously running crystal-controlled
multivibrator to trigger the 9-bit PRF-1 or t_1 counter. If the count in the
t_1 counter reaches the limit of the verification time (a preset binary number
for each band) a nonverified reset pulse is generated in the counter. The
t_1 counter resets itself to the initial state, prevents readout, and resets the
pulse steering circuit to its initial state.

If the first PRF interval is acceptable, the second incoming video pulse
causes the pulse steering circuit to shut off the clock pulse gate to the t_1
counter, and permits a clock pulse gate to trigger the PRF-2 or t_2 counter.
The t_2 counter counts clock pulses until the third input video pulse is re-
ceived by the pulse steering circuit. The third pulse shuts off all clock-
pulse gates and closes the pulse steering circuits, thus keeping out additional
pulses until the information stored in the PRF counters is read into the tape.
If the second PRF interval is longer than the band verification time the t_2
counter resets itself to zero and closes the pulse steering circuit input to
additional pulses in the same manner in which the circuit is closed when a
third pulse has been received. Readout proceeds normally.

The pulse steering circuit performs the additional function of permitting the
2-Mc start-stop oscillator to be turned on for a time corresponding to the
width of the second received pulse. The PW of the second pulse will then be
registered on the 6-bit PW counter. A pulse longer than the counter capa-
bility of 31.5 μsec will cause the counter to overflow. All pulses longer
than 31.5 μsec will register as 32 μsec. Entry of the first pulse of a se-
quence into the pulse steering circuit also starts the recorder control and
readout action.

The 13-bit time counter receives pulses from Subsystem C & C at 1-second
intervals. The maximum count is 8192 seconds. To minimize the possibility

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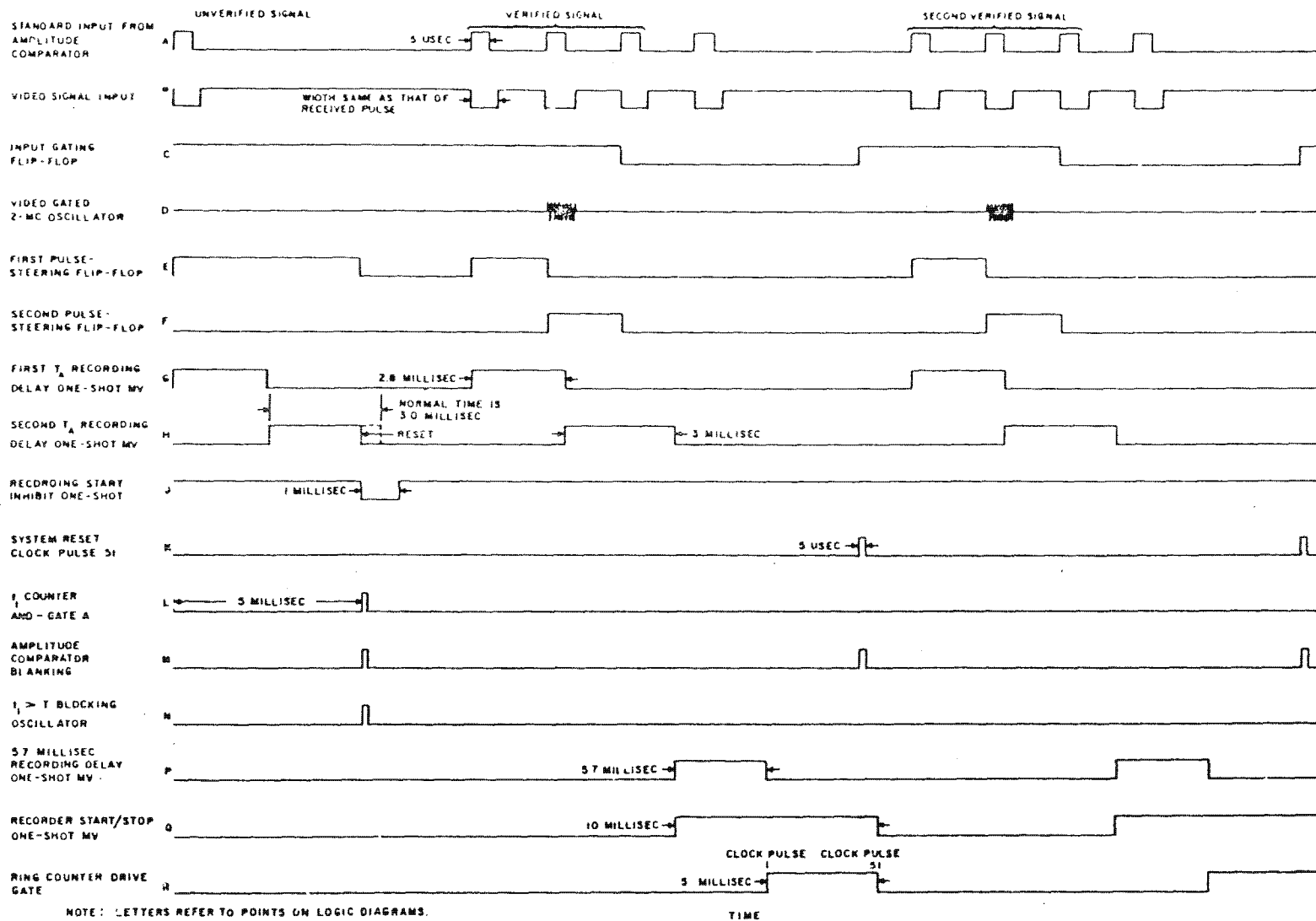
Figure 2-30 Intercept Timing Diagram

NOTE: LETTERS REFER TO POINTS ON LOGIC DIAGRAMS.

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of error, a portion of the time counter circuits prevents the time counter from changing count during readout. Time pulse that occurs during readout is delayed and then added to the counter after readout. Every 8192 seconds a pulse is supplied by Subsystem C & C to reset the counter and ensure synchronism with the vehicle clock.

One-shot delay multivibrators, which are triggered by the pulse steering circuit, start the recorder three maximum pulse intervals minus 10 milliseconds after the first received pulse. The recorder requires less than five milliseconds to reach recording speed. Three maximum pulse intervals minus five milliseconds after the first received pulse, the readout counter, which generates clock pulses 1 to 50 at a 10-kc rate, is started.

The binary numbers in each information counter and on the frequency shaft encoder are read out by the clock pulses through AND gates in the data sampler matrix section. A parity-check bit is also added. The write portion of the recorder circuits transforms the data to non-return-to-zero (NRZ) form for entry into the tape recorder. Four tracks are recorded-- two each of data and 10-kc timing pulses. Clock pulse 51 stops the tape drive and resets the data handler to its initial conditions.

The reproduce section of the recorder circuits combines the information on the redundant timing and data tracks of the tape recorder and converts combined information to return-to-zero (RZ) form for telemetry transmission to the readout station. The order of the RZ output format will depend on whether the recorder playback is in the reverse or forward direction (first or second readout). During readout the recorder operation is controlled by RTC's from the TAS.

The data handler readout of time information alone or time and attitude information alone can be controlled from the power and control assembly. The attitude measurement is made by driving the data handler with a signal consisting of a three-pulse sequence derived from the attitude converter described in paragraph 2.5.4. The time between the first and second pulses is proportional to the pitch reference voltage; the time between the

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second and third pulses is proportional to the roll reference voltage. The sequence is fed into the pulse steering circuit and appears as a PRF measurement of the t_1 and t_2 counters; however, no frequency or PW measurement will appear in this word. This attitude word is produced once for each complete frequency scan cycle (located between band 1 and 2 words).

A one-bit parity counter that is triggered by each preceding data pulse during readout adds a "1" if the number of 1's on bits 1 through 49 is odd. This provides the TAS with a means for detecting bit errors in recording or data transmission.

Provision is made for permitting the data handler's output to bypass the recorder upon command. By using this direct readout and by inserting a test signal input to the data handler, the data are transmitted directly over the data link without recording, thereby providing a direct check on the operation of the data handler alone. This check can be used to determine whether the redundant handler should be switched in.

2.4 TAPE RECORDER

The tape recorder can record digital information in a start-stop fashion on magnetic tape, and can, on command, play back this information continuously in either a forward or reverse direction. The start-stop operation is used to economize on tape; the tape moves only when information is available for recording or when it is being read out. Stored information may be read out in discrete blocks (for ground testing) or continuously.

The recorder is designed to accept an NRZ type digital signal. In this type of word signal, each change of voltage level designates a 1 bit, and each absence of level change designates a 0 bit. The digital word contains 50 bits of information and is of five milliseconds duration. The recording is accomplished by completely saturating a flexible one-quarter-inch-wide magnetic tape in alternating directions. Four separate and identical channels are available for recording. Two channels are used to redundantly

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record 50-bit data words, and the remaining two are used to redundantly record 50-bit synchronous timing words. A schematic diagram of a single channel read and write amplifier is shown in Figure 2-31. Four such circuits are included on separate printed-circuit cards in the recorder. The write circuit consists of four transistors set up in an "H" fashion to switch current in the recording head from one direction to the other. When a zero level input signal is applied, transistor switches Q7 and Q10 are conducting, and current passes through the head and completely saturates the tape in one direction. When a 28-v write signal is applied, transistor switches Q7 and Q10 are cut off, and Q8 and Q9 conduct. Current now passes in the opposite direction. Each change in the input from 0 to 28 v or 28 to 0 v results in the tape being saturated in the opposite direction.

The speed at which the tape moves in the recorder is determined by two factors:

    a.   The electronic consideration of pulse packing density on the tape

    b.   The mechanical consideration of starting, moving, and stopping the tape and associated mechanisms at rates in keeping with the system requirements

For the particular read head and amplifiers involved, tape speeds of approximately 18 ips or faster give adequate response. Conversely, tape speeds of 30 ips or faster impose mechanical resonance problems and pose difficulties in bringing the tape to the correct speed in the desired time. The speed of 22.5 ips was selected as a practical compromise of the two factors. In particular, the reduction from 30 to 22.5 ips improves the mechanical operation by:

    a.   Reducing the quantity of tape required (reduced inertia of tape to pull)

    b.   Lowering the final tape speed (easier start-time requirement)

    c.   Shortening the length of tape to move per burst of words (reduces reel oscillation)

The tape transport mechanism is set up so that a 13.7 ±1.1 millisecond rectangular pulse supplied to the actuator circuits will activate the tape pinch rollers and brake release. The amplitude of this pulse is from 5 to

2-48
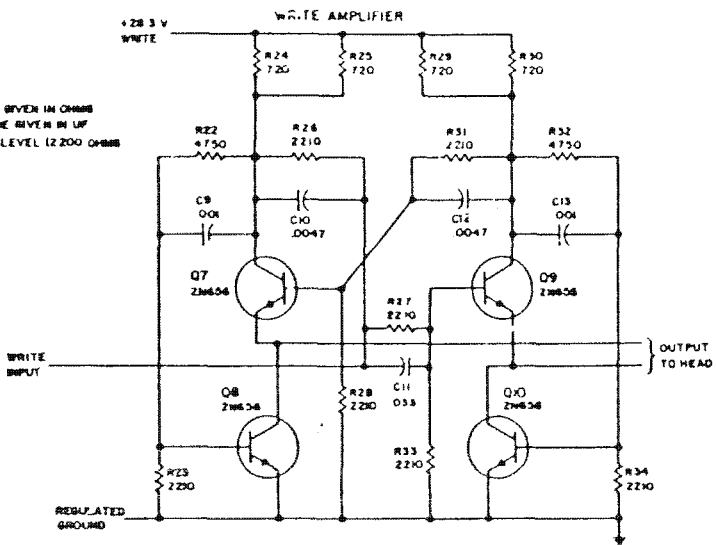
WRITE AMPLIFIER
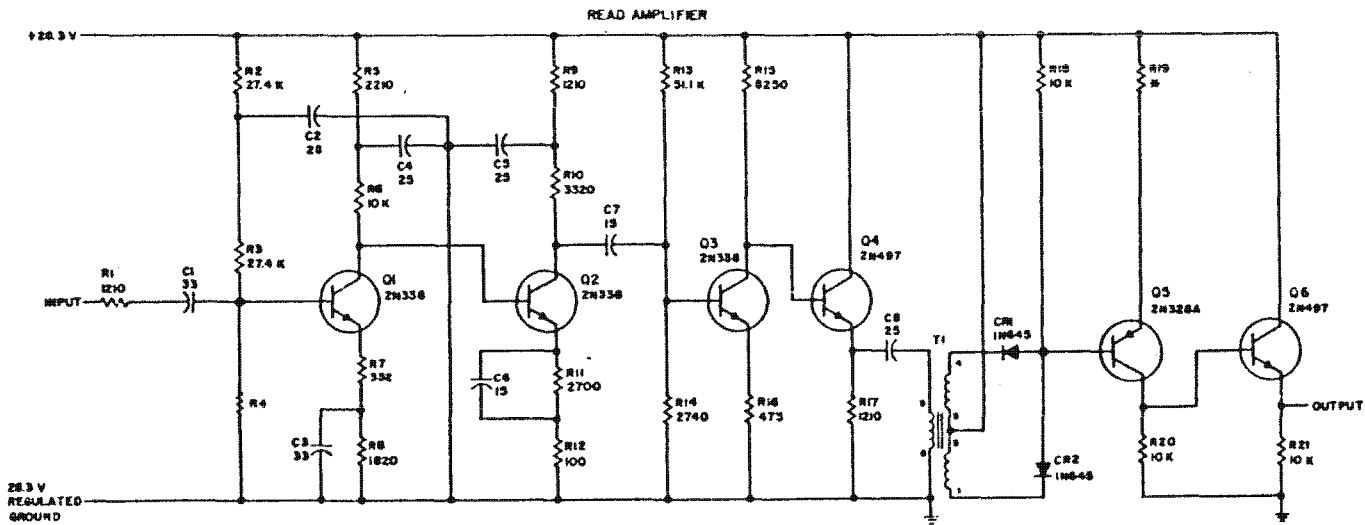
READ AMPLIFIER

Figure 2-31 Schematic Diagram of Single Channel Read and Write Amplifier

12 v. The leading edge of the actuator square wave is 5.7 ±0.7 milliseconds
ahead of the first digit in the information word. The 5.7-millisecond interval
permits the tape to reach the operating speed of 22.5 ±4.5 ips. The end of
the actuator square wave extends nominally 3 milliseconds beyond the last
digit of the word. At the end of the actuator square wave, the pinch roller is
pulled away from the tape and braking torque is applied by the brake. The
maximum actuate rate of the recorder is 66 actuations per second. The tape
length is sufficient for 10,000 recorded words. The actuator and recorder
control electronics are shown in Figure 2-32. When an input pulse is applied
to Q1, it conducts, causing Q2 to conduct which in turn causes Q3 to conduct.
Current drawn through Q3 energizes the brake coil (which releases braking
torque) and also draws current through the low-resistance pulse coil of the
actuator.

To accomplish continuous tape motion a separate actuator line (to a high re-
sistance actuator coil) and a separate brake line are supplied. A grounding
signal can be supplied through these separate lines to maintain steady-state
conditions. Less power is required in the steady-state mode than in the
pulsed mode.

In the readout mode, each change of state on the tape produces a positive
output pulse in its respective output channel. A zero bit on the tape (no
change of state on the tape) results in no signal being issued on the particular
channel. The circuit that accomplishes the readout--the read amplifier cir-
cuit--is shown in Figure 2-31. The stages that include Q1 through Q4 are
biased somewhere between saturation and cutoff. When a change of state is
sensed by the head, either a positive or negative pulse--depending upon the
direction of saturation of the tape--is introduced into the input of the read
amplifier. Depending upon the polarity of the input pulse Q1 becomes more
conductive or more cut off. Each succeeding stage amplifies the input pulse
in a similar manner until a pulse is introduced into the pulse transformer.
The output pulses are full-wave rectified and only the negative-going pulse
will pass through to Q5. When a pulse passes to Q5, Q5 will conduct causing
emitter follower Q6 to conduct, resulting in a positive pulse at the output.
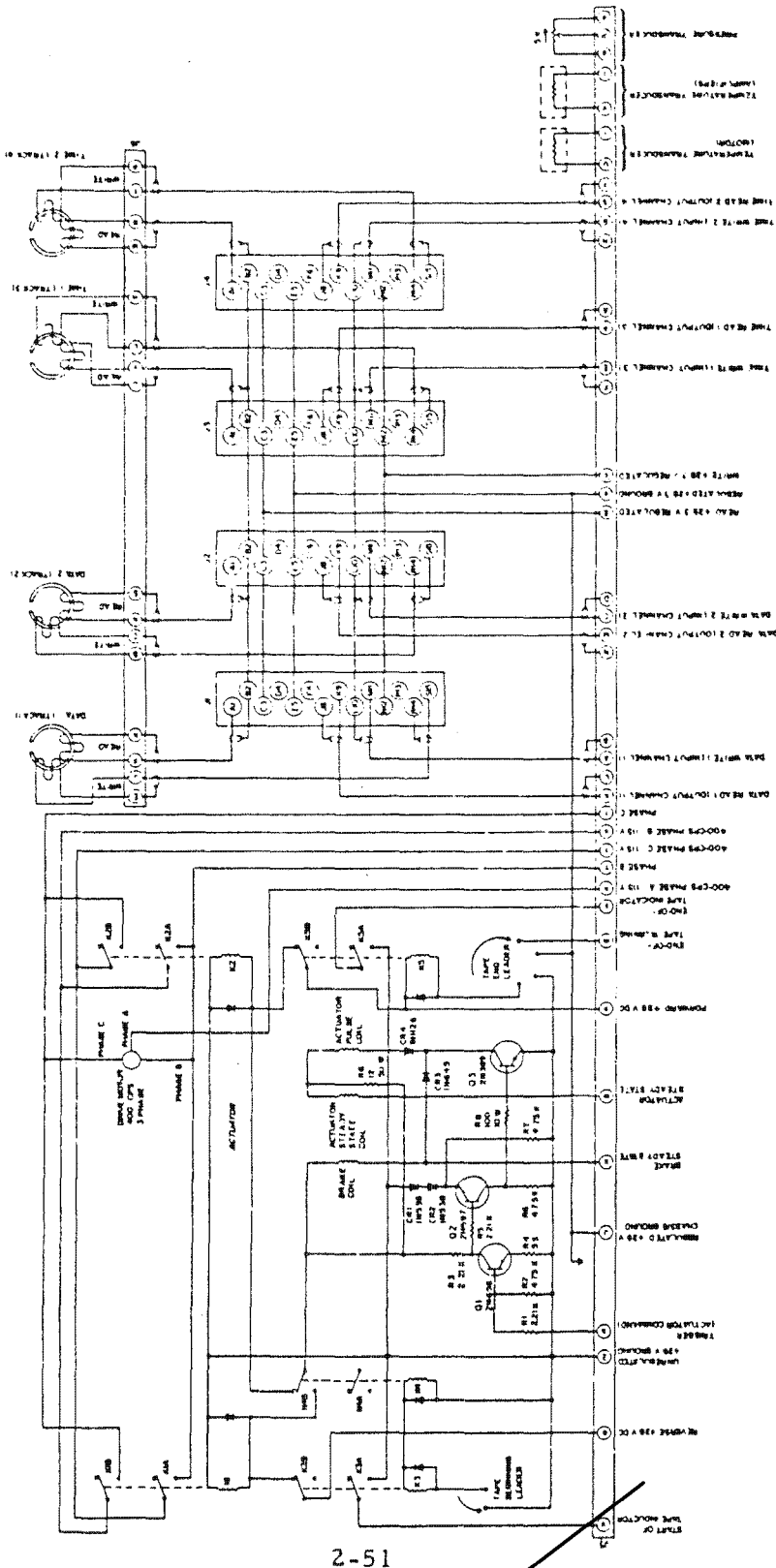
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Figure 2-32 Actuator and Recorder Control Electronics

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An electrically conducting leader is spliced to each end of the tape and is connected to the supply reels. In the event that the system fails to supply the proper stop signals, sensors are provided which automatically prevent the tape from leaving the supply reels. A summary of the tape recorder specifications follows:

Number of Tracks:	4 (two for information and two for synchronization)
Steady-State Recording Speed:	22.5 ips
Steady-State Readout Speed:	22.5 ips
Start-Record-Stop Cycle:	5 milliseconds for each interval (nominal)
Bit Density:	445 bits per inch (nominal)
Tape Capacity:	sufficient for 10,000 record blocks
Tape Length:	250 feet (nominal)
Tape Width:	0.25 inch

When the back end of the tape has reached the record heads, the recorder will automatically rewind and the ferret equipment will be ready for new intercept data.

2.5 PAYLOAD CONTROL EQUIPMENT

The control functions for the payload are performed by the power and control assembly shown in Figure 2-33. A block diagram is shown in Figure 2-34. The power and control assembly consists of the following:

a. Repeat Cycle Timer - This unit controls the band-switch cycle.

b. Low-Voltage Power Converter - This unit supplies 12 v for the transistor circuits in the receivers and data handlers.

c. Internal Programmer and Band Code Matrix - This unit generates the signals that place the start-stop time words on the tape, and provides for receiver blanking during the recording of these words. It also provides a digital indication of the receiver that is actively scanning.

d. Test Generator - This unit provides a test signal to check the performance of the receivers and/or data handlers.

2-52
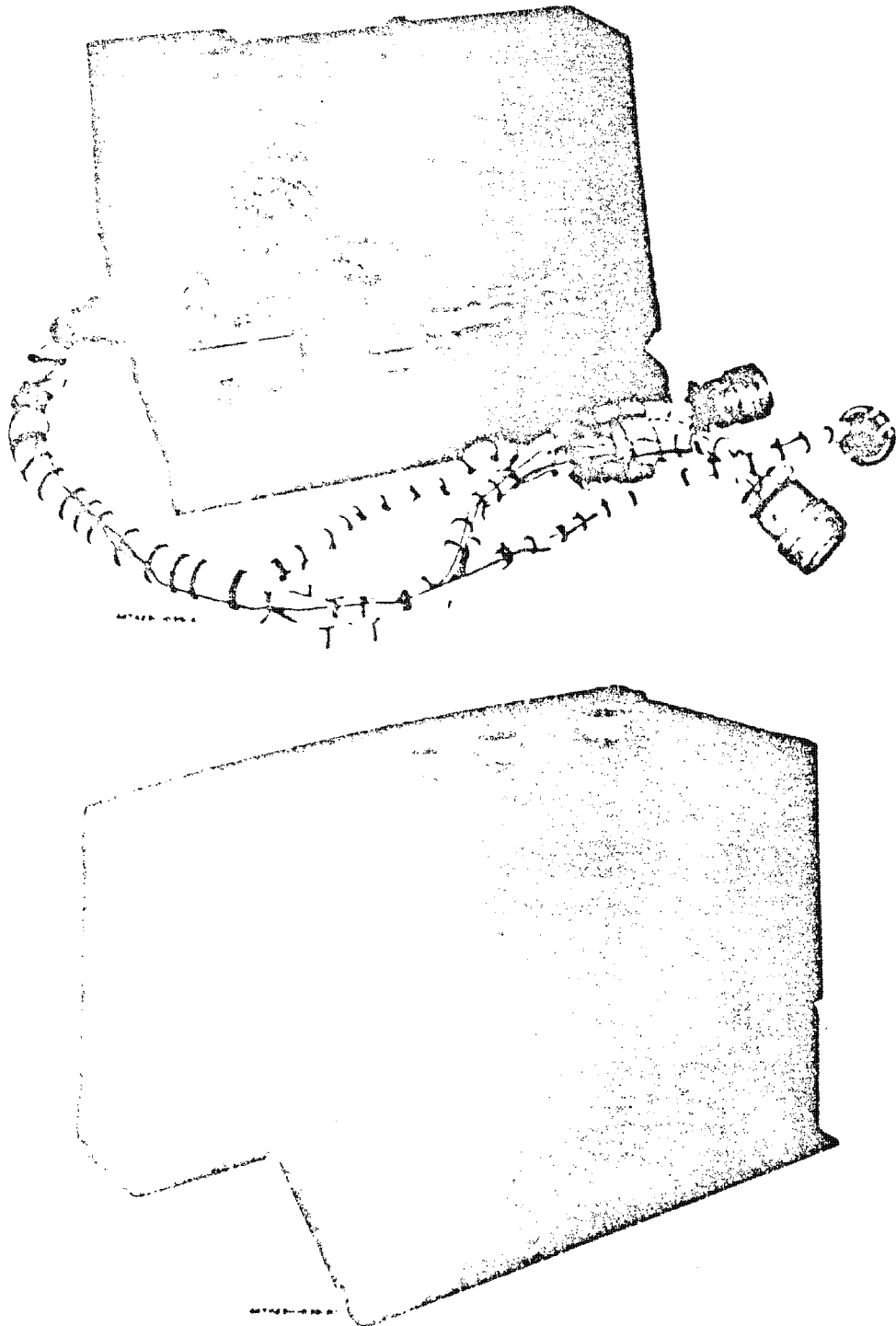
Figure 2-33 Power and Control Assembly

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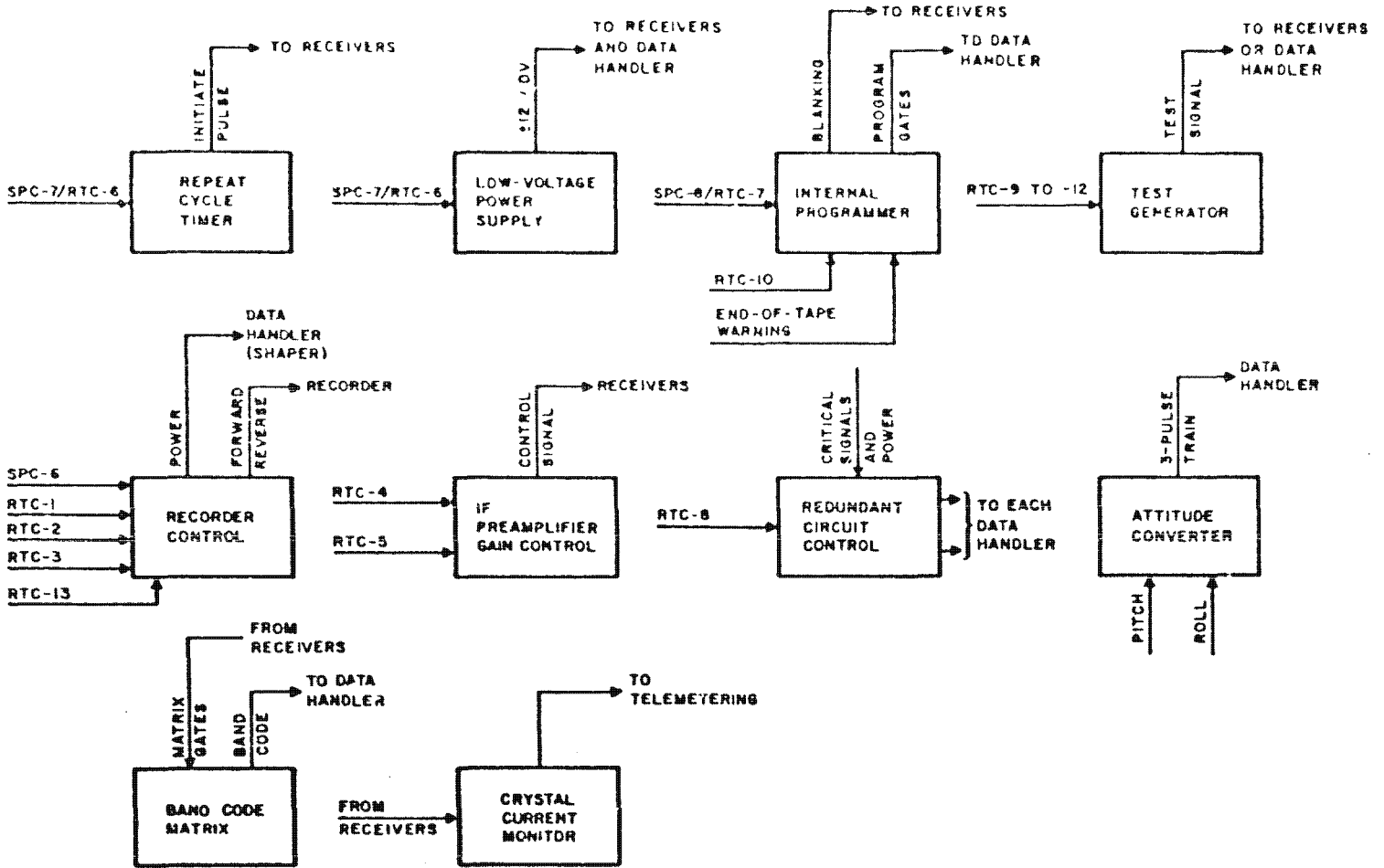
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Figure 2-34 Block Diagram of Power and Control Assembly

e. Recorder Control - This unit controls the power for the readout circuits. It also programs the tape drive motor in the proper direction for recording and readout.

f. I-F Preamplifier Gain Control - This unit permits the gain of each preamplifier to be changed in 1-db steps. Eleven steps and one off position are provided.

g. Redundant Circuit Controls - This unit is a switchover network that switches critical signals from one data handler to the other.

h. Attitude Converter - This unit is a d-c level-to-pulse interval converter. It converts the analog voltages--pitch and roll--to pulse format for digitization and recording on the tape.

i. Crystal-Current Monitor - This unit is made up of a set of magnetic amplifiers that amplify crystal currents to a level suitable for telemetering purposes.

These units control the basic operations of the receiving and data handling equipment. The selections of modes of operation (Table 2-3) are accomplished by the real-time commands (RTC) and stored program commands (SPC) supplied by Subsystem C&C to the payload. These commands are received in the form of relay contact connections.

2.5.1 Modes of Operation of Payload Equipment

There are five basic modes of operation of the payload equipment; they are listed in Table 2-3. The table indicates the SPC's or RTC's that initiate the respective modes. The normal-receive mode, which can be activated by either SPC's or RTC's, has a large number of variations.

The variations have to do with the bands that are energized. This mode, when controlled by SPC's, is completely flexible; when it is controlled by RTC's, all bands are actuated. The receive-with-direct-readout mode is the same as the RTC-actuated normal-receive mode except that the recorder is bypassed--that is, the digital data are read out into the data link without being recorded.

In the normal readout mode the recorder runs in the reverse direction. The first intercept word read out is the last one recorded. When all the data have been read out, the read heads of the tape recorder are at the front end of the

2-5

Table 2-3

MODES OF OPERATION OF F-2 (FLTS 1, 2) FERRET EQUIPMENT

Mode	SPC (in required time order)	RTC
1. Normal receive		
a. Energizes band 1	1, 7, 6, 8	
b. Energizes band 2	2, 7, 6, 8	
c. Energizes any combination of above bands	any, (1 to 5), 7, 6, 8	
d. Energizes all bands		14, 6, 2, 7
2. Receive with direct readout (all bands)		14, 6, 13, 7
3. Normal readout		3, 1
4. Second readout		2, 1
5. Test receive--direct readout		
a. Equal signals to I-F strips		14, 13, 6, 9, 10, 12*
b. 3-db attenuation of inhibit signal		14, 13, 6, 9, 10, 11, 12*
c. 7-db attenuation of inhibit signal		14, 13, 6, 9, 10, 11, 12
d. Video supplied to data handler		14, 13, 6, 9, 12*

In addition, there are two other functions performed by the RTC's and that can be considered modes of operation.

1. I-F gain adjustment		4, 5
2. Change data handler		8, 12*

*RTC 12 must be opened for reset.

tape. If the recorder is now commanded to run in the forward direction, a second readout of data may be accomplished. Intercept words are now read out in the same order in which they were recorded.

The test-receive mode is used to check the performance of the I-F amplifiers, amplitude comparator, and payload data handling system. This mode is a receive-with-direct-readout mode, except that a test generator is energized and the receiver local oscillators are not energized. The test mode has four phases: (a) equal I-F signals are fed to all I-F amplifiers, (b) the I-F signals fed to the inhibit channels are 3.0 db less than those fed to signal channels, (c) the I-F signals fed to the inhibit channels are 7.0 db less than those fed to the signal channels, and (d) a video signal is fed directly to the data handler. Although I-F signals are applied to all I-F amplifiers, responses are obtained only from the actuated band. During the test-receive mode of operation all critical points are monitored.

Two other operational functions can be activated by RTC's. They are I-F gain adjustment, and the substitution of the redundant data handler. An I-F gain correction can be made if the operation in the test-receive mode indicates the necessity. These gain corrections are made on each I-F amplifier by a two-step process: first, the amplifier whose gain is to be corrected is selected, second the gain correction is made. These corrections can be made to compensate for changes in the gain of an individual I-F amplifier or in the preceding stages. The capability of switching to the redundant data handler is provided in case of failure in the original unit. The failure of a data handler will be determined by analysis of the monitoring data and intercept data.

2.5.2 On-Off Control and Internal Programming

The payload is placed in its various operating modes by means of SPC's or RTC's. RTC's are used when the satellite is within range of a TAS. At other times SPC's with proper time indexing perform the turn-off and turn-on operations.

2.5.2.1 <u>Stored Program Commands</u>. A list of SPC's required for the payload are tabulated in Table 2-4. Six commands are required. These commands are provided in the form of sets of relay contacts that perform the following functions:

    a.   Activate either or both receivers.

    b.   Permit the tape recorder drive motor to turn in the forward direction.

    c.   Turn on low voltage supplies, start the repeat cycle timer.

    d.   Turn on power for the local oscillator; put a preliminary identification word on the tape (via the internal programmer), and then unblank the receivers.

2.5.2.2 <u>Real-Time Commands</u>. The RTC's required for the payload are tabulated in Table 2-5. Fourteen commands are required. These commands are also in the form of sets of relay contacts that perform the following functions:

    a.   Permit the tape recorder drive motor to turn in the reverse direction (the direction for data readout).

    b.   Apply power to the read electronic circuits.

    c.   Permit the tape recorder drive motor to turn in a forward direction (the direction for a second readout of data if a second readout is required).

    d.   Activate all receivers.

    e.   Turn on low voltage power supplies (similar to SPC-7).

    f.   Turn on power for local oscillators (similar to SPC-8).

    g.   Permit a gain adjustment for any preamplifier. A gain adjustment is made in 11 steps of 1 db each. An off position is also provided.

    h.   Permit operation of test generator for checking on-orbit operation of receivers and data handling equipment.

    i.   Permit switchover to standby data handler (and return).

    j.   Permit a direct readout from data handler (bypassing recorder).

2.5.2.3 <u>Timing Diagram</u>. A timing diagram of the sequence of SPC's for the normal receiver cycle is shown in Figure 2-35.

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Table 2-4

STORED PROGRAM COMMANDS FOR F-2 (FLTS 1, 2)
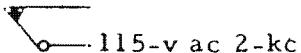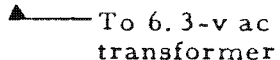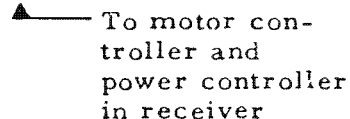
SPC Number	Command Name	Function	Contacts (a)	Contacts (b)
1	ACTIVATE BAND 1	a. Applies filament voltage	115-v ac 2-kc / To 6.3-v ac transformer	+28 v / To motor controller and power controller in receiver
		b. Enables motor controller and power controller to be energized		
2	ACTIVATE BAND 2	a. Applies filament voltage	115-v ac 2-kc to 9.0-v ac transformer	+28 v to motor controller and power controller in receiver
		b. Enables motor controller and power controller to be energized		
3	Not used in F-2 (Flts 1, 2)			
4	Not used in F-2 (Flts 1, 2)			
5	Not used in F-2 (Flts 1, 2)			
6	MOTOR DRIVE FORWARD	Starts tape drive motor in forward direction	To RTC-2 and RTC-3 +28 v tape recorder forward	Not used

Table 2-4 (contd)

SPC Number	Command Name		Function	Contacts (a)	Contacts (b)
7	READY RECEIVERS	a.	Energizes low-voltage power supplies	+28.3 v low-voltage power supply, receivers and data handler circuits	400-cps power for repeat cycle timer
		b.	Starts repeat cycle timer		
8	RECEIVE CYCLE ON	a.	Triggers internal programmer, blanks and unblanks amplitude comparator	2 kc to all receivers	To internal programmer
		b.	Applies power to local oscillator via power controller in each receiver		

Table 2-5

REAL-TIME COMMANDS FOR F-2 (FLTS 1, 2)
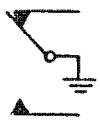
RTC Number	Command Name	Function	Contacts (a)	Contacts (b)
1	READ-OUT	Applies ground to holding circuit on recorder actuator	To recorder actuator and brake To recorder	Permits auto rewind on second readout
2	MOTOR DRIVE FORWARD	a. Applies power to shaper and read amplifier b. Drives tape motor in forward direction c. Starts auto rewind if RTC-1 is closed	To latch relay	To shaper latch relay
3	MOTOR DRIVE REVERSE	Starts tape motor in reverse direction	Interlock for RTC-2	+28 v (from SPC-6) To recorder and read power contactor
4	PREAMPLIFIER SELECT	Selects preamplifier for gain adjustment	To rotary solenoid	Not used
5	GAIN ADJUST	Selects gain position on selected preamplifier	To rotary solenoid via preamplifier select switch	Not used

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Table 2-5 (contd)

RTC Number	Command Name	Function	Contacts (a)	Contacts (b)
6	READY RECEIVER	Same as SPC-7	(see SPC-7)	(see SPC-7)
7	RECEIVE CYCLE ON	Same as SPC-8	(see SPC-8)	(see SPC-8)
8	STANDBY CIRCUIT CONTROL	Switches in standby data handling system	To switchover network	Not used
9	TEST GENERATOR CONTROL	Turns on video test generator	+12 v To pulse generator	-12 v To pulse generator
10	TEST GENERATOR CONTROL	Turns on oscillator, disconnects video generators from data handling system, unblanks receivers	+12 v To oscillators	To relay for switching and to internal programmer
11	TEST GENERATOR CONTROL	Switches in attenuator 3-db	To attenuator relay in test generator	To RTC-12
12	TEST GENERATOR CONTROL	Switches in attenuator 7-db (when RTC-11 is closed)	To attenuator relay in test generator	To data handler reset circuit
	DATA HANDLER RESET	Resets data handler		To RTC-8

Table 2-5 (contd)

RTC Number	Command Name	Function	Contacts (a)	Contacts (b)
13	REAL-TIME READ-OUT	Connects output of data handling system directly to data link (bypass recorder)	+28 v Control relay and read power contactor	Interlock for read amplifier power
14	ACTIVATE ALL BANDS	Activates all receiver bands	+28 v To each receiver	Auxiliary relay for filament power

ON-CYCLE

SPC-1 AND -2 CLOSE
FILAMENT WARM-UP STARTS

48 SECONDS

SPC-7 CLOSES
LOW-VOLTAGE POWER SUPPLIES ON;
TIMER MOTOR STARTS; BAND SWITCHING CYCLE ON

56 SECONDS

SPC-6 CLOSES
TAPE DRIVE MOTOR RUNS IN FORWARD DIRECTION
ALL RECEIVERS BLANK

64 SECONDS

SPC-8 CLOSES AND PROVIDES POWER
TO LOCAL OSCILLATOR

INTERNAL PROGRAMMER
ON-CYCLE

INITIAL RESET

75
MILLISEC

TIME ONLY
(USE TRAILING EDGE)

UNBLANK
RECEIVERS
18
MILLISEC

OFF-CYCLE

SPC-1 AND -2 OFF
SPC-8 OFF, REMOVE
POWER TO LOCAL OSCILLATORS

ALL RECEIVERS BLANKED

75
MILLISEC

TIME ONLY
(USE TRAILING
EDGE)

18
MILLISEC

ZERO
WORD
START

16 SECONDS
SPC-6 AND-7 OFF

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Figure 2-35 Timing Diagram of System On-Off Control

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a.   At time T_O, SPC-1 and SPC-2 permit filament power to warm up the local oscillators and also permit motor control relays and power control relays to be energized.

b.   At T_O + 48 seconds, SPC-7 turns on low voltage power supplies and starts the repeat cycle timer.

c.   At T_O + 56 seconds, SPC-6 starts the tape recorder motor in the forward direction. The motor has 8 seconds to get up speed before the receivers are turned on. The receivers are blanked at this time.

d.   At T_O + 64 seconds, SPC-8 turns on power to the local oscillators. The internal programmer is triggered at this time. The following signals are generated:

1.   An initial reset signal is sent to the data handler.

2.   A 75-millisecond gate is generated and is used to pull in the recorder capstan and to put a short space on the tape. The trailing edge of this gate is used by the data handler to write a time only start word on the tape.

3.   Fifteen milliseconds later, the receivers are unblanked.

The order of the turn-off cycle is:

a.   At time T_1, SPC-8 removes power from local oscillators and both receivers are blanked. SPC-1 to 2 open and permit further receiver action:

1.   A 75-millisecond gate is generated. The trailing edge of this gate is used by the data handling system to write a time only stop word on the tape.

2.   A 15-millisecond gate is triggered by the trailing edge of the 75-millisecond gate. The trailing edge of the 15-millisecond gate triggers the recorder start-stop multivibrator in the data handler. This places a small trailer on the tape.

b.   At T_1 + 16 seconds, SPC-7 turns off the low voltage power supplies and removes 400-cps power from the repeat cycle timer. SPC-6 stops the tape motor.

2.5.2.4 Internal Programmer. The internal programmer generates the long delay gates when triggered by the opening and closing of SPC-8 or RTC-7. Figure 2-36 is a block diagram of the circuit. Several trigger circuits are required. These are resistor capacitor networks. When SPC-8 or RTC-7 transfers from off to on position, a capacitor is discharged through a resistor, generating a trigger; this action also starts a 75-millisecond delay

2-65
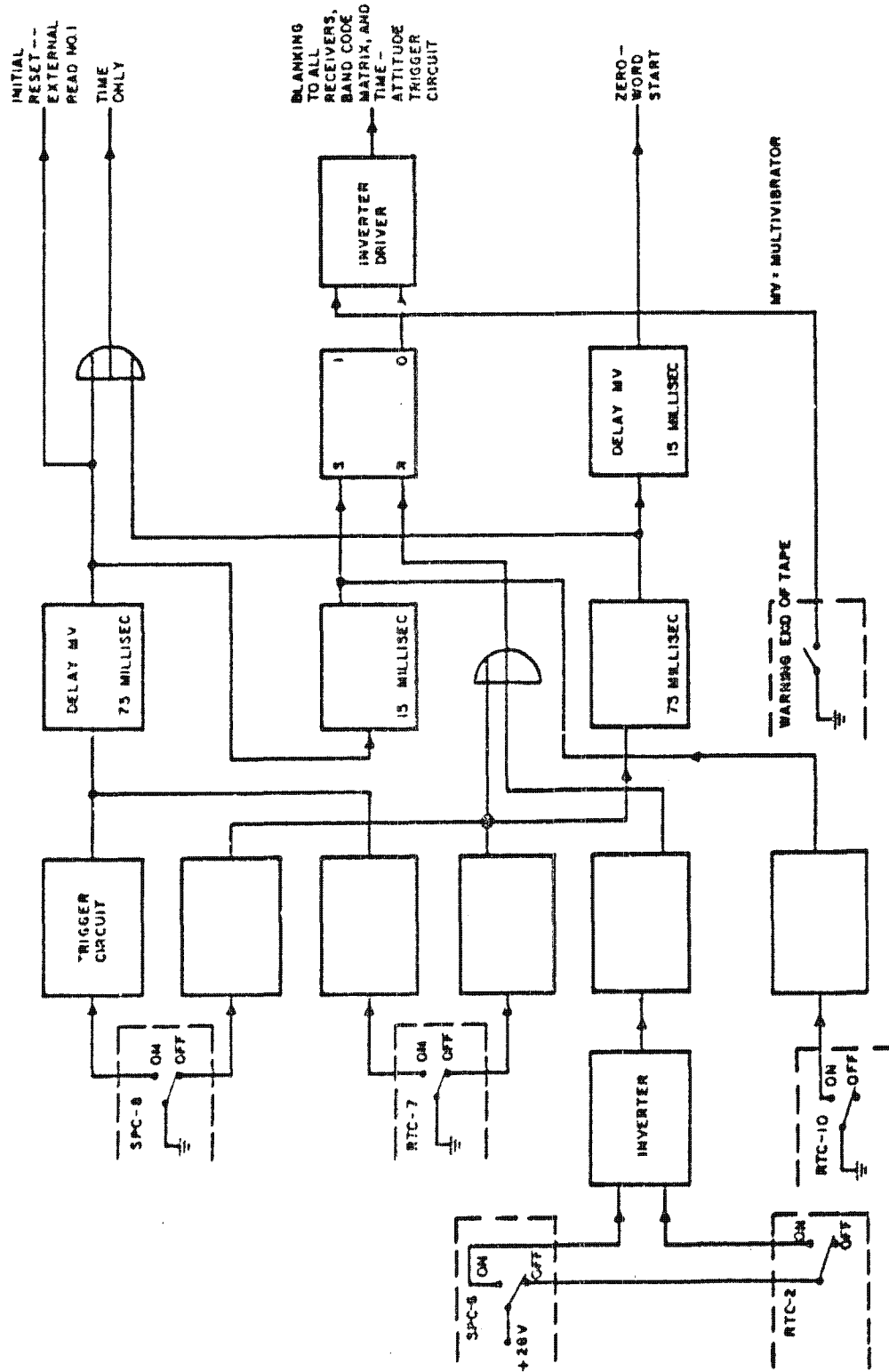
Figure 2-36 Block Diagram of Internal Programmer

2-66

multivibrator. This multivibrator places the zero word leader on the tape. The trailing edge of the multivibrator signal causes the tape data handling system to record a time-only start word. When SPC-8 transfers from the on to off position, a second 75-millisecond delay multivibrator is triggered. The trailing edge of the multivibrator signal causes a time only word to be recorded on the tape. In addition, a 15-millisecond multivibrator is triggered. The trailing edge of its signal, places a zero-word trailer on the tape. A trigger circuit is also included; it unblanks the receivers whenever the test-receive mode is initiated.

2.5.3 Low-Voltage Power Supply

The power available from the vehicle auxiliary power supply does not fill all the needs of the ferret equipment. It is therefore necessary to provide low-voltage regulated power supplies for transistorized circuits. The primary considerations in the design of these supplies are overall efficiency, size, weight, and reliability. Special power supplies that are required by each receiver, including filament transformer power supply, are included in each receiver assembly. The power converter in Subsystem F supplies ±12 v. The regulation is ±1.5 percent under all conditions of load, input, and temperature variations. Maximum output current is 500 ma for each output (+12 and -12 v). A saturable-core square-wave voltage converter is used to supply the ±12 v. To increase the overall converter efficiency, the regulated 28.3 v dc supply voltage is used as the input voltage.

The ±12 v power supplies provide transistor operating voltages for the data handler, control circuits, I-F amplifier, and amplitude comparator.

The ±12 v power supplies have identical circuits (Figure 2-37). The input to each regulator is a rectified and filtered 1-kc square wave derived from a common dc-to-dc converter.

Error amplifier Q8 compares the voltage at the junction of divider R9 and R10 with the voltage from CR7 and CR8. Since R9 and R10 are across the output, the voltage at the emitter of Q8 is proportional to the output. The base voltage of Q8 is fixed by voltage references CR7 and CR8; therefore,

2-67
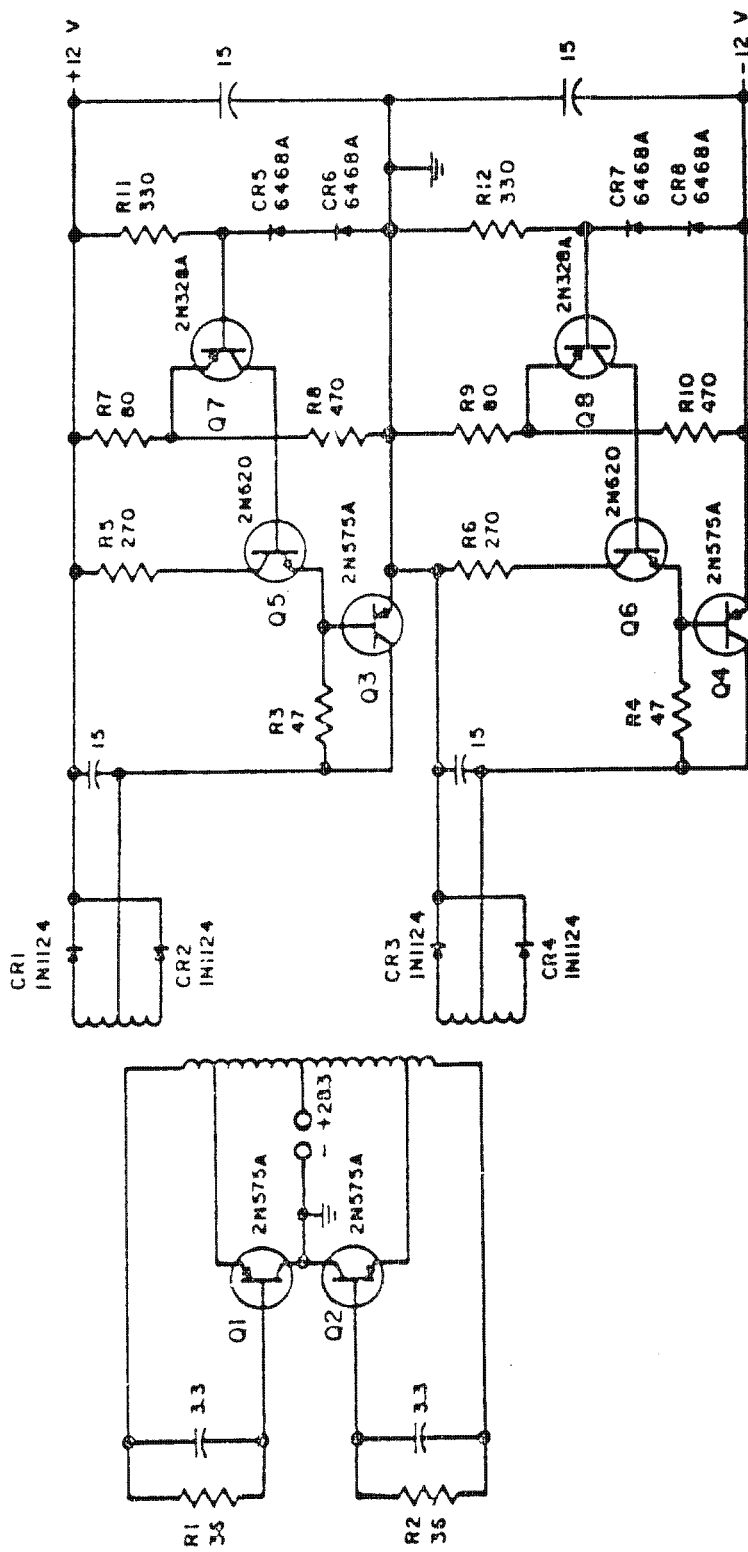
UNLESS OTHERWISE NOTED:
RESISTOR VALUES ARE GIVEN IN OHMS
CAPACITOR VALUES ARE GIVEN IN UF

Figure 2-37 Schematic Diagram of ±12 v Power Supplies

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the collector current of Q8 is proportional to the output voltage. This collector current, amplified by Q6, flows through resistor R4. The voltage drop across R4 is the collector voltage drop of series transistor Q4, which controls the output voltage.

2.5.4 Attitude Converter

To record satellite attitude data with intercept data on the digital tape recorder, it is necessary for the attitude data to be in digital form. The attitude is measured by a horizon sensor (not part of Subsystem F). The outputs of the sensor are d-c voltages that are proportional to the displacement angles (pitch and roll) measured with respect to the satellite axes. The polarity of these voltages depends on the directions of displacement.

The conversion to digital form is a two-step process. First, pulses are generated, with their time separation proportional to the pitch and roll voltages; second, this time separation is measured by digital techniques to produce a digital number.

The conversion from voltage to time is made in the attitude converter shown in Figure 2-38. This unit contains two sweep generators, one for each attitude voltage. The sweep generators start their sweep at the most negative voltages expected and rise through zero to the most positive voltages expected. The first sweep (pitch) is triggered by the payload control system; when the sweep voltage equals the pitch voltage, a pulse is generated that is separated in time from the triggering pulse by a time proportional to pitch voltage. The pulse generated by the pitch measurement triggers the second sweep, which responds to roll voltage in the same manner as the first sweep does to the pitch voltage. Thus, the output of the attitude converter has the form of three pulses. The interval in time between the first two represents the pitch displacement, and the interval between the second and third represents the roll displacement. These three pulses are fed to the data handler which responds to them as if they were a normal intercept; consequently, it measures these two pulse intervals and records them. Attitude data are
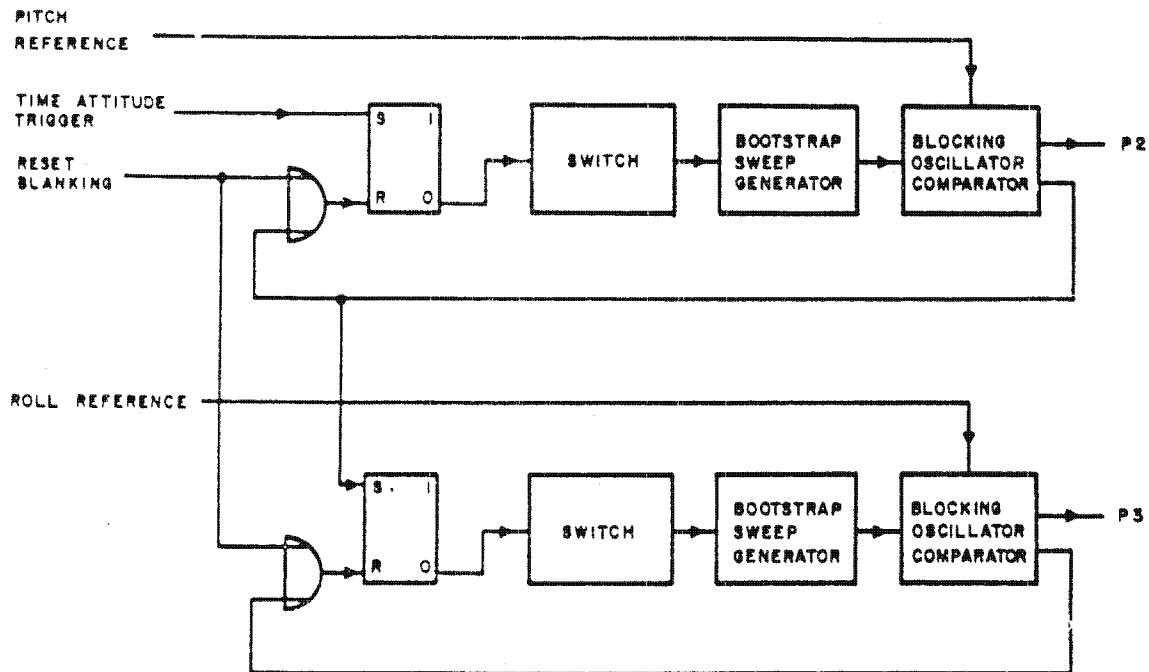
Figure 2-38 Block Diagram of Attitude Converter

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recorded once each frequency scan cycle. The specifications for the attitude converter are listed below.

Range of Input Level	-5 v to +5 v
Digitization Range	3 to 43
Sweep Accuracy	±0.75 v

2.5.5 I-F and Video Test Generator

The test generator will enable on-orbit testing of the I-F and video amplifiers, the amplitude comparator, and the data handler.

The test generator, shown in Figure 2-39, consists of a pulse generator that supplies a video signal to the data handler, and a 60-Mc oscillator which is modulated by the pulse generator. The 60-Mc oscillator supplies a signal to the signal and inhibit I-F amplifiers. Attenuators are included to reduce the signal to the inhibit I-F amplifiers by 3 db and 7 db and to thus check the selection level of the amplitude comparator. The test generator is programmed by four RTC's.

The pulse generator is turned on by RTC-9. The characteristics of the output pulse are listed below.

PW	8.0 µsec
PW Stability	±0.5 µsec
PRF	400 pps
Rise Time	0.5 µsec
Fall Time	1.5 µsec

These pulses are derived from a one-shot multivibrator that is triggered by the 400-cps supply. A detector circuit is included to provide an indication of pulse generator operation. A d-c voltage from the detector is transmitted to the telemetering equipment. The pulses from the multivibrator are normally directed to the data handling equipment.

The 60-Mc oscillator is turned on by RTC-10. The oscillator has a frequency stability of ±0.5 Mc.

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400 CPS, SINGLE PHASE

RTC-9

+12 V

-12 V

AMPLIFIER LIMITER

MONOSTABLE MULTIVIBRATOR

PEAK DETECTOR

FOR MONITORING

DIFFERENTIATION NETWORK

VIDEO TEST TO DATA HANDLER

RTC-10

+12 V

60-MC OSCILLATOR

+28 V

ISOLATION NETWORK

TO SIGNAL PREAMPLIFIERS

ATTENUATOR

ISOLATION NETWORK

TO PREAMPLIFIERS

RTC-11

RTC-12
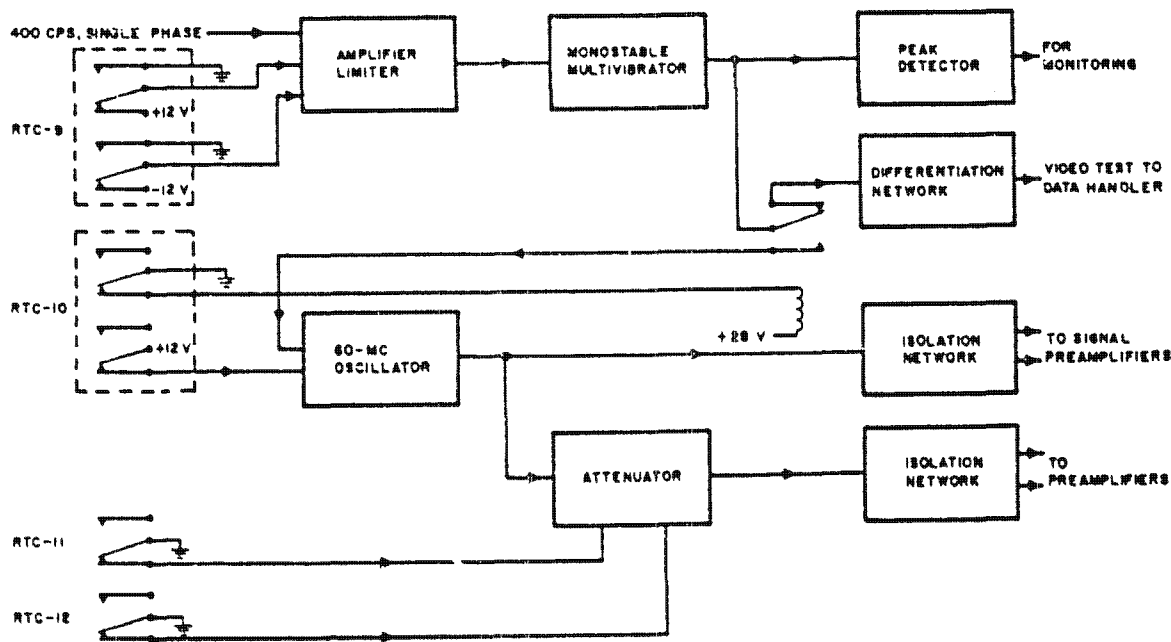
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Figure 2-39 Block Diagram of I-F and Video Test Generator

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When the oscillator is used as a test signal source, the pulse generator is disconnected from the data handler and is used to modulate the oscillator. The oscillator output is directed to each preamplifier through suitable isolation and attenuator networks. RTC-11 and RTC-12 decrease the inhibit signal by 3 db and 7 db, respectively.

The frequency and band information will depend on where the receivers happen to be tuned. There will be no PW measurement because the video signal is injected directly into the data handler, bypassing the amplitude comparator and its video PW measuring circuits. When the pulse-modulated 60-Mc oscillator is used to check the I-F amplifiers, the output from a detector circuit included at the output of each amplifier is monitored to check the gain-tracking characteristics. The test signal sent to the inhibit I-F amplifier is attenuated 3 db by RTC-11. An activity indicator on the output of the amplitude comparator is checked. When the inhibit signal is attenuated 7 db by RTC-12, an accept pulse is transmitted to the data handler. This checks the selection level on the amplitude comparator. The monitoring points provide an indication when the video pulse is accepted by the data handler. A continuous train of intercept words is transmitted to the ground station via the data link. The information in these words is the same as in the video test words, except that a PW measurement is also made.

2.5.6 Monitoring Control

The monitoring points for the payload equipment are summarized in Table 2-6. The selection of the monitoring points was a compromise between equipment simplicity and sufficient monitoring information to sense failures. the frequency response of telemetering equipment limits the monitoring bandwidth to about 0.5 to 8 cps if many points are to be monitored with only one transmitter.

2.5.7 I-F Preamplifier Gain Adjustment

A gain adjustment is provided for the two preamplifiers contained in each receiver. Eleven steps of 1 db each and an OFF position are provided. The

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Table 2-6

MONITORING POINTS

	Description	Measurement Type	Number of Points	Type of Data	Accuracy Required (percent)	Reason for Monitoring
Per System	Mixer crystal current	Voltage	4	Analog	˙5	Indication of mixer crystal drive
	(The mixer crystal monitoring points are switched to the band that is active.)					
Per Receiver (2 used)	Band on-off	Voltage	1	ON-OFF	-	Indication of power applied to receiver
	Amplitude comparator unblanking	Voltage	1	ON-OFF	5	Indication of receiver unblanking
	Most significant digit of encoder	Voltage	1	ON-OFF	-	Indication of encoder and motor rotation
	Preamplifier gain setting	Voltage	4	Analog	5	To check gain setting of each channel
	I-F amplifier output	Voltage	2	Analog	5	I-F amplifier performance
	Amplitude comparator activity	Voltage	2	Analog	5	Amplitude comparator operation
	Special power supply (if required)	Voltage	3	Analog	5	Power supply performance
	Temperature	Resistance	2	Analog	5	Future design information

Table 2-6 (contd)

	Description	Measurement Type	Number of Points	Type of Data	Accuracy Required (percent)	Reason for Monitoring
Per Data Handler (2 used, but only one set of monitoring points)	Activity	Voltage	21	Analog	15	Check circuit operation
	Slow-speed flip-flop	Voltage	2	ON-OFF	-	Check circuit operation
	Temperature	Resistance	2	Analog	5	Future design information
Per Recorder (1 used)	Front end of tape	Voltage	1	ON-OFF	-	Control
	Back end of tape	Voltage	1	ON-OFF	-	Control
	Temperature	Resistance	2.	Analog	5	Future design information
	Pressure	Resistance	1	Analog	5	Check pressurization
Per Power and Control Unit (1 used)	**Test Generator**					
	Video test signal	Voltage	1	Analog	5	Check pulse generator performance
	Attenuator position	Voltage	2	ON-OFF	-	Control purposes
	Power Supply					
	Output voltage	Voltage	2	Analog	5	Check power supply performance
	Input voltage	Voltage	1	Analog	5	Check input to power supply

Table 2-6 (contd)

Description	Measurement Type	Number of Points	Type of Data	Accuracy Required (percent)	Reason for Monitoring
Power Monitoring					
Vehicle supply voltages	Voltage	6	Analog	5	Check power supplied to Subsystem F
Control and Command Equipment					
Relay operation	Voltage	12	ON-OFF	-	Indication of operation
Temperature	Resistance	3	Analog	5	Future design information

Per Power and Control Unit (1 used)

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gain adjustment is made using successive operation of an RTC. A rotary
solenoid changes the position of a wafer switch which in turn varies the re-
sistance in series with the preamplifier. This process is depicted in Fig-
ure 2-40. A voltage divider network provides for telemetering to the TAS
the position of the wafer switch. To allow for expected inaccuracies of the
telemetry equipment, the supply voltages, and the divider network, a four-
level code and two telemetry points per switch are used. The code is listed
below.

Position	Code
1	11
2	12
3	13
4	14
5	21
6	22
7	23
8	24
9	31
10	32
11	33
12	34

Each code number refers to one of four voltages at one of the two monitor
points. These normal voltages are 0.60, 1.76, 2.85, and 3.86 v.

2.5.8 Band-Switch System

Each receiver contains the components necessary to tune the local oscil-
lator, to apply power to the receiver circuits, to unblank the receiver for
the proper interval and to present a digital indication of the frequency to
which the receiver is tuned when an intercept is recorded. The components
required for these functions are:

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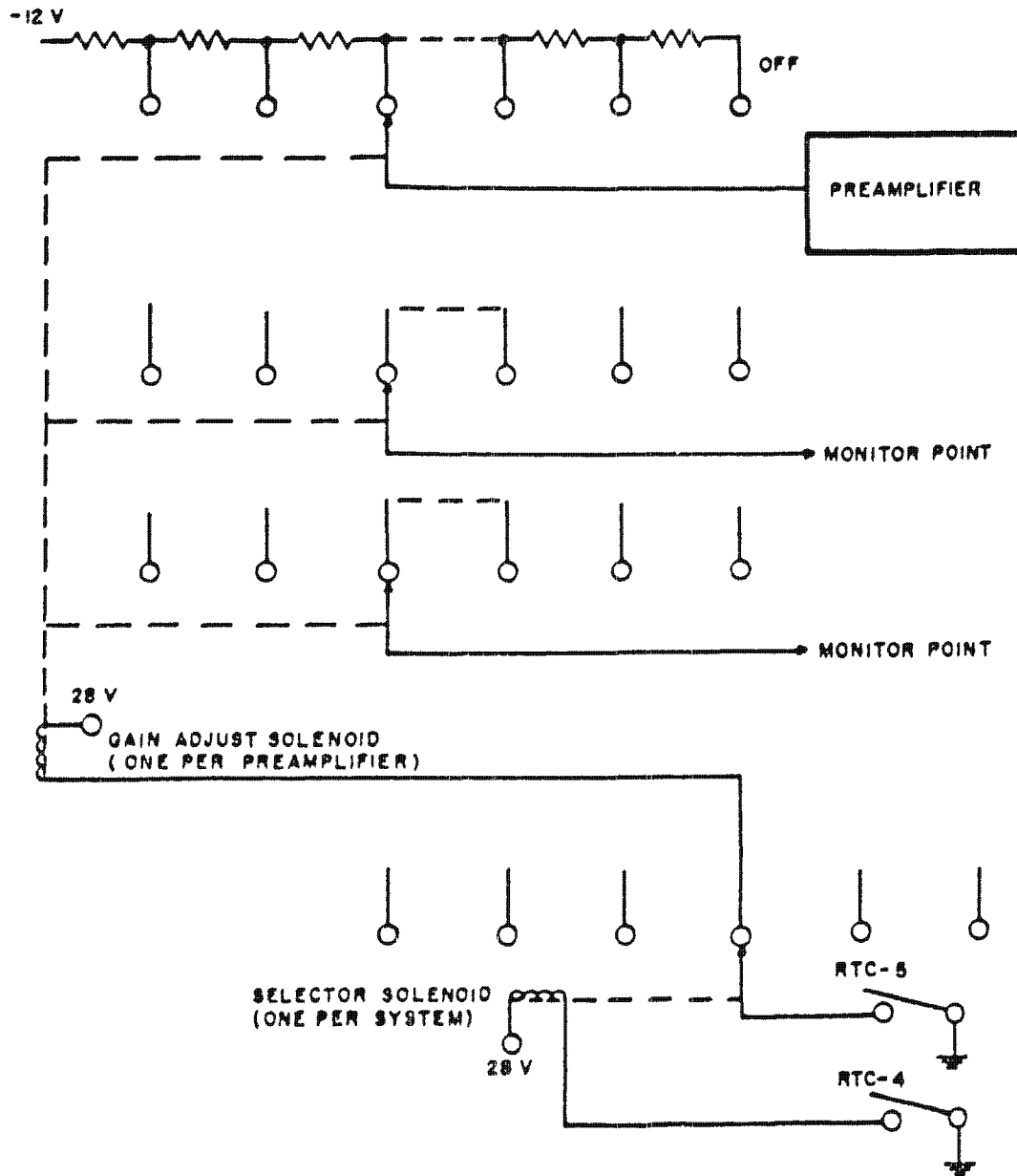
Figure 2-40 Schematic Diagram of I-F Gain Control

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a.   Band-tuning motor (scan motor)

b.   Analog-to-digital shaft encoder (9-bit gray code)

c.   Sensor circuit

d.   Amplitude comparator unblanking circuit

e.   Motor controller

f.   Power controller

2.5.8.1 Band-Switch Control. Figure 2-41 is a block diagram of the band-switch system. A repeat cycle timer generates initiate signals to start the scan motor of each receiver in the proper sequence. The repeat cycle timer is actuated by SPC-7 or RTC-6 (received from Subsystem C&C). The initiate pulses are derived from cam-operated microswitches in the repeat cycle timer. In the F-2 (flts 1, 2) payload, initiate pulses for both bands 1 and 2 have a cycling time of 13.5 seconds. SPC-1, SPC-2, or SPC-3 permit these initiate pulses to pull in a latch relay, the motor controller. Either one of these SPC's also pulls in another latch relay, the power controller (now shown in Figure 2-41). The motor controller starts the receiver scan cycle and rotates the shaft encoder. A sensor unit continuously reads the angular scan shaft position in gray code. The gray code readings for the start and finish signals are indicated in Figure 2-41. A short time after the end-of-scan signal for band 1 is generated, the initiate pulse for band 2 starts the scan cycle for this receiver. The band 1 receiver motor, however, continues rotating until a stop signal is generated from the sensor, unlatching the motor controller and stopping the scan shaft at a reference point; band 2 scan then follows. Figure 2-42 is a timing diagram. The scanning rates are selected to permit each receiver to intercept a minimum of three pulses from an emitter at the lowest expected PRF. Band-switch data are summarized in Table 2-7. Hysteresis synchronous motors are used for tuning. These motors have a maximum start time of 500 milliseconds. Their stop time is 50 milliseconds.

The stop-time requirements are met with the aid of a solenoid brake applied to the motor shaft. The brake normally clamps the shaft. When power is

2-79
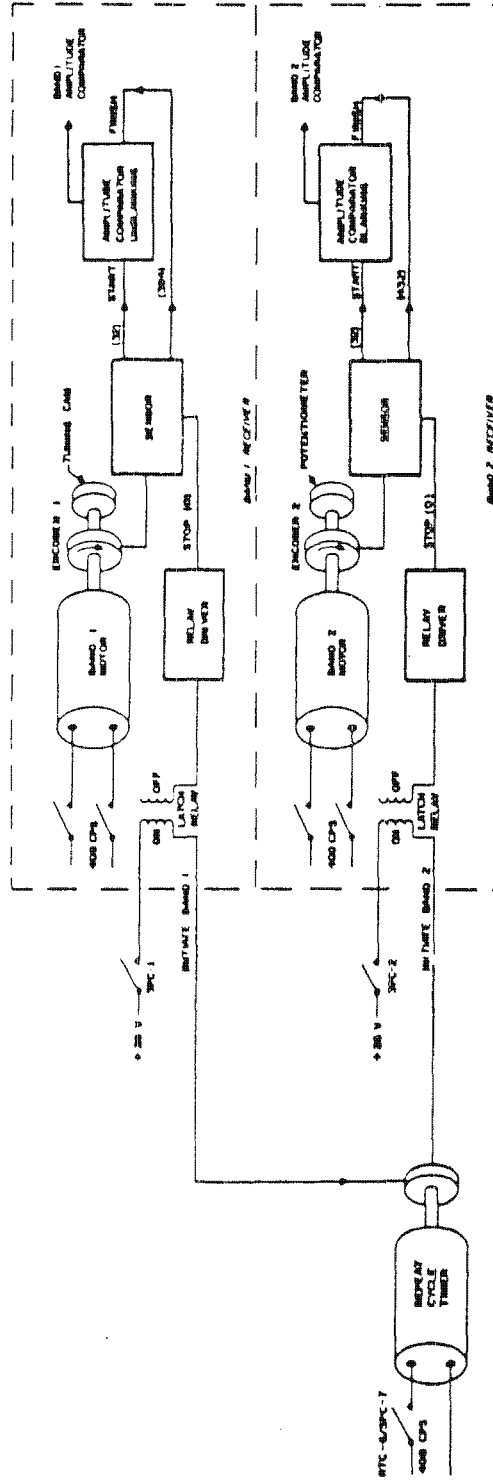
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Figure 2-41 Functional Block Diagram of Band Switching System

2-80

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ALL TIME
IN SECONDS
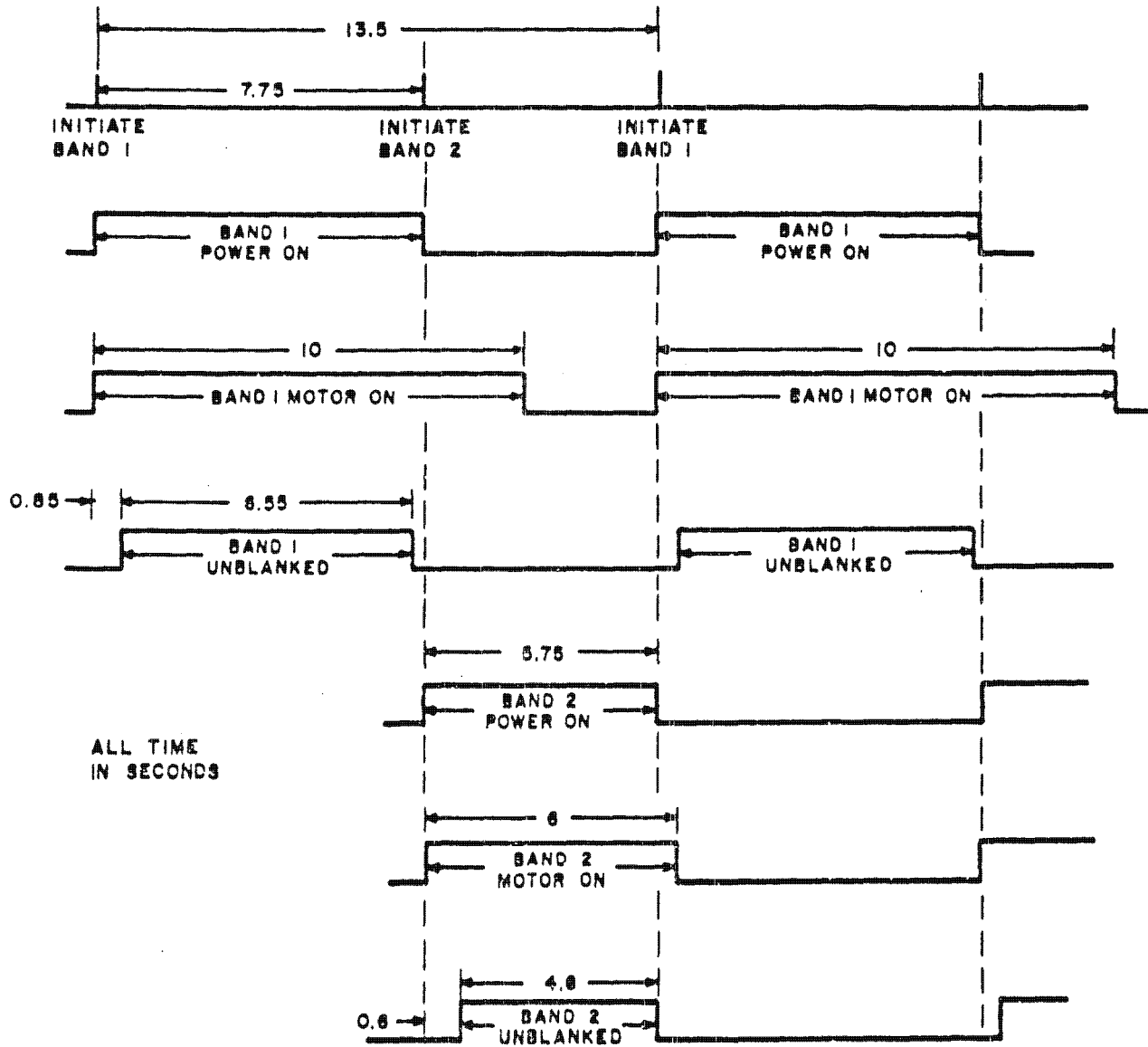
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Figure 2-42 Timing Diagram for F-2 (Flts 1, 2)

2-81

Table 2-7

RECEIVER SCAN CHARACTERISTICS FOR F-2 (FLTS 1, 2) SYSTEM

Band Number	Frequency (Mc)	Minimum PRF (pps)	Time per Channel (milliseconds)	Number of Channels	Channel Bandwidth (Mc)	Time in Band (seconds)	Total Cycle Time (seconds)
1	2500 to 3200	125	24	280	2.5	6.6	13.5
2	9000 to 10,000	125	24	200	5.0	4.8	

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applied to the motor and brake, the brake is disengaged and the motor is free to turn. When power is removed from the motor and brake, the brake stops the motor rapidly.

2.5.8.2 Receiver Control Operation. Figure 2-43 is a block diagram of the control system for a typical receiver requiring plate and filament supplies for operation of the local oscillator. The initiate pulse from the repeat cycle timer latches the power controller and the motor controller if RTC-14, SPC-1 or -2 is activated. The power controller applies power to the local oscillators, I-F amplifiers, and amplitude comparators. The motor controller applies 400-cps power to the band scan motor and disengages the brake from the motor shaft. The shaft encoder presents a continuous indication of the angular position of the scan shaft. The sensor sends start and finish signals to the amplitude comparator unblanking circuit. A delay multivibrator keeps the unblanking signal active for 25 milliseconds after the receiver is blanked. This is sufficient time for the data handler to complete the processing of any intercept received at the edge of the band.

The gating waveform is inverted and then transmitted to the control unit, where it used to actuate the proper verification circuit in the data handler. It is also used to generate in the band code matrix a digital description of the active receiver (Figure 2-44). Power for each receiver is turned off by the initiate pulse for the succeeding receiver.

The receiver blanking input permits external control of the receiver output. If a filament transformer is required, it is energized by one set of contacts on SPC-1 or SPC-2.

2.6 WEIGHT AND POWER SUMMARIES

Table 2-8 lists the peak power requirements of the system.

Table 2-9 lists the weight of the ferret equipment.

2-83
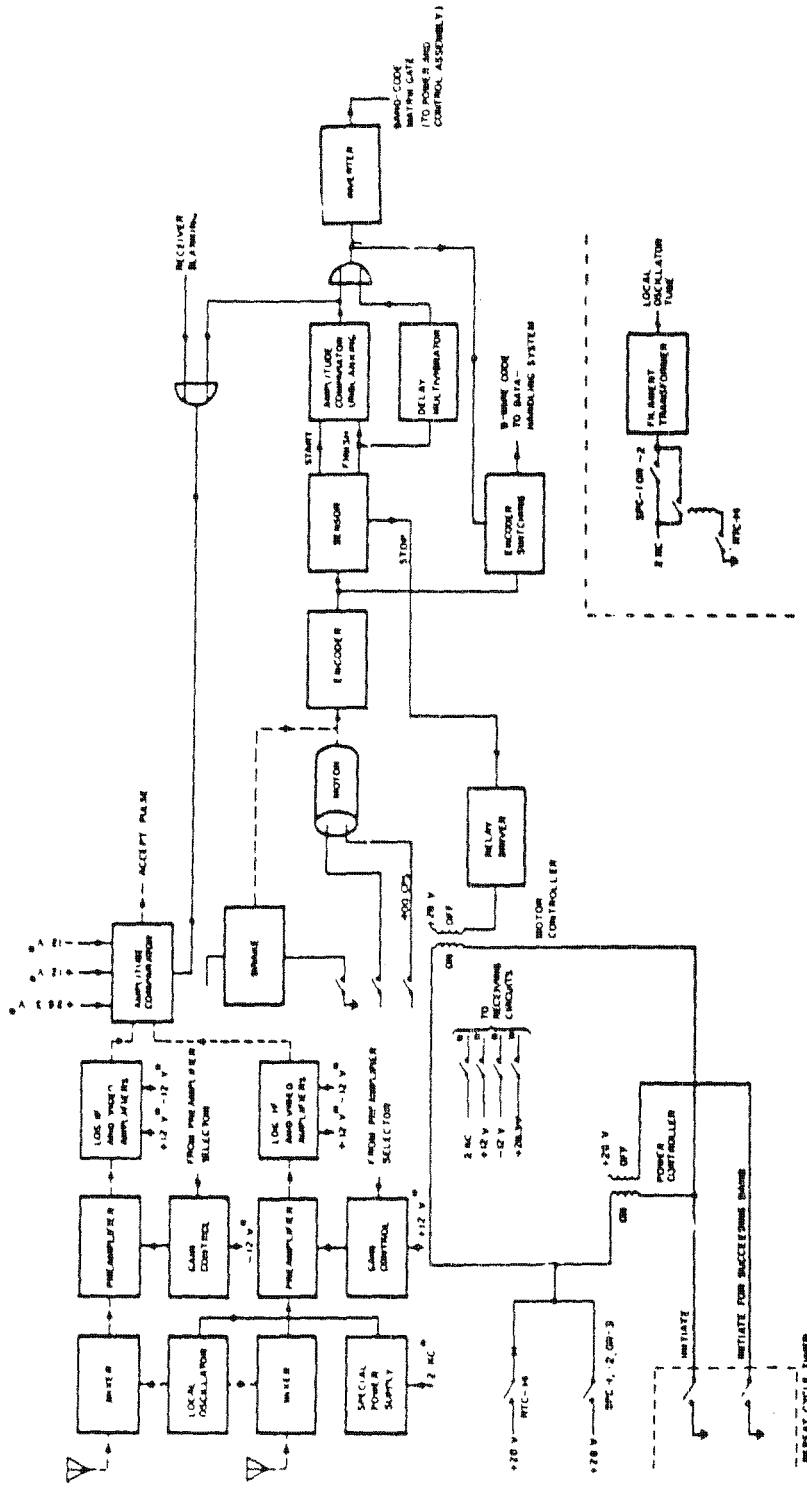
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Figure 2-43 Functional Block Diagram of Receiver Control

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WIRES ①, ② AND ③ YIELD A
BINARY CODE INDICATING WHICH BAND
SHAFT ENCODER IS SUPPLYING OUTPUT
TO DATA HANDLING.
(I INDICATES +12 VOLTS; O INDICATES
GROUND)

OUTPUTS:	I	2	3
BAND I MATRIX GATE	O	O	I
BAND 2 MATRIX GATE	O	I	O
NOT USED IN F-2 (FLTS I, 2,)	O	I	I
NOT USED IN F-2 (FLTS I, 2,)	I	O	O
NOT USED IN F-2 (FLTS I, 2,)	I	O	I
BETWEEN BANDS:	I	I	I

TO RECEIVER
BLANKING MULTIVIBRATOR (WHICH ON
COMMAND, BLANKS ALL AMPLITUDE
COMPARATORS).

| | O | O | O |

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Figure 2-44 Schematic Diagram of Band Code Matrix

2-85

Table 2-8

PEAK POWER REQUIREMENTS FOR F-2 (FLTS 1, 2) PAYLOAD EQUIPMENT

Mode	115 v 400 cps (watts)	115 v 2 kc (watts)	Regulated + 28.3 v (watts)	Regulated - 28.3 v (watts)	Unregulated + 28 v (watts)
Normal Receive	59	17*/35	26	Negligible	45
Readout	30	-	5.5	0.1	20
Standby	-	-	2.2	Negligible	-
Test Receive	29	17*	27.5	0.1	21
Receive with Direct Readout	29	17*/35	27.5	0.1	21
Gain Adjust	-	-	-	-	84

*Warmup power only. Power factor will be corrected to 0.8 minimum.

Table 2-9

ESTIMATED WEIGHTS AND VOLUMES OF F-2 (FLTS 1, 2) PAYLOAD EQUIPMENTS

Item	Weight (pounds)	Volume (cubic feet)
Band 1 Receiver	60	1.21
Band 2 Receiver	50	0.99
Tape Recorder Assembly	20	0.39
Data Handler	18	0.45
Data Handler (redundant)	18	0.45
Power and Control Assembly	26	0.25
Structure	58	1.43
Harness and Connectors	14	
Antennas and Mounting Platform Including Dummy VHF Antenna	38	
Total	302	

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SECTION 3
FERRET 2 (FLIGHTS 3 AND 4) PAYLOAD EQUIPMENT

3.1 ANTENNAS

Band 1 and band 3c antennas are being designed to provide about a 30-degree signal antenna beamwidth, about a 70-degree inhibit antenna beamwidth, circular polarization, and a circular coverage area intercepted on the earth's surface. Since only the composite radiation pattern of the signal and inhibit antennas affects emitter location, beamwidth of the signal antenna can be defined as that angular region in which the gain of the signal antenna is greater than that of the inhibit antenna. Generally it is desirable to have moderate gains, 10 to 20 db, in signal antennas. Such gain is readily obtainable in the Subsystem F antennas at the higher frequencies (above 1 Mc) but is impossible because of antenna size limitations at the lower frequencies.

The band 1 antennas for the F-2 (flts 3, 4) payload will be similar to those used on the F-2 (flts 1, 2) payload. Their placement, however, in the antenna array is necessarily different.

A single antenna structure of a teardrop configuration is used for both signal and inhibit functions in band 3b. This is accomplished by operating the antenna in both the sum and difference modes simultaneously. Because of size limitations imposed on the antenna structure, the resulting radiation patterns provide a swath coverage and consequently result in modified inhibit action.

The band 3c antenna is a double-bay turnstile element with a cross type reflector plane about midway between the turnstiles. Signal and inhibit functions are obtained by simultaneously operating the antenna in both the sum and difference modes.

A photo of an engineering model of the antenna configuration for the F-2 (flts 3, 4) payload is shown in Figure 3-1, on-orbit and prelaunch positions being depicted.

3-1

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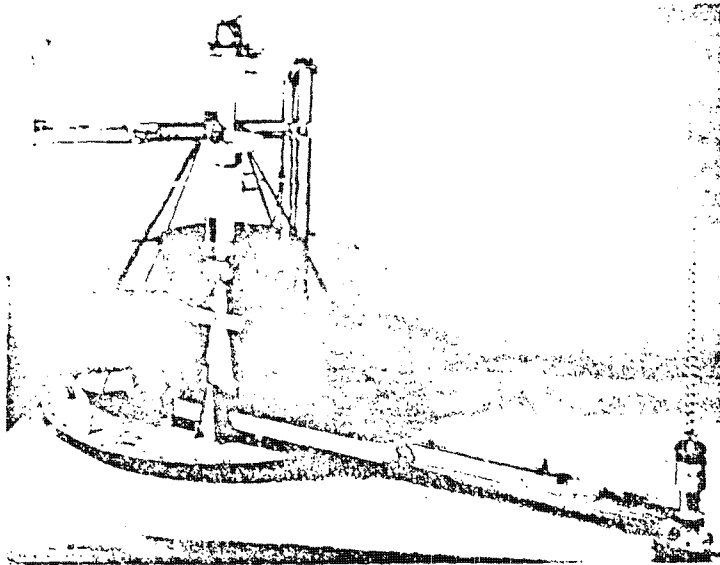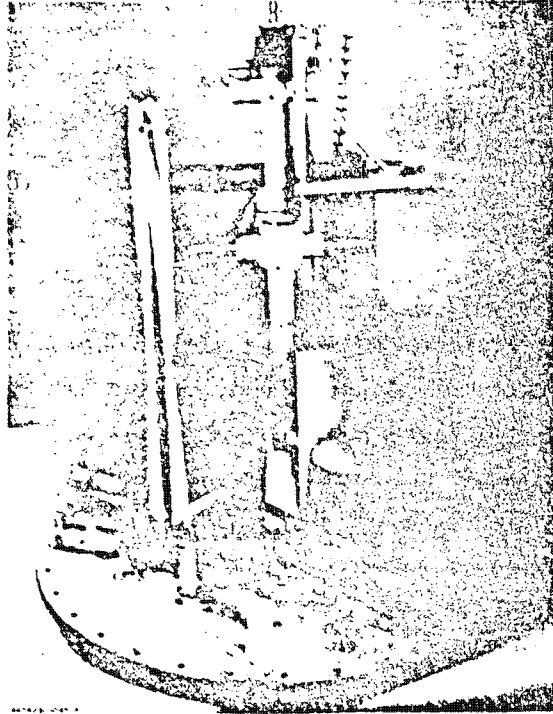
Figure 3-1 Antenna Nest for F-2 (Flts 3, 4) Payloads

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3.2 RECEIVERS

A block diagram of the F-2 (flts 3, 4) receivers is shown in Figure 3-2.
These receivers are generally similar to the F-2 (Flts 1, 2) receivers and
the general design criteria as given in Section 2 for superheterodyne re-
ceivers apply. The amplitude comparator, however, has been modified to
provide signal and inhibit video outputs and an "acceptable" pulse output to
supply data that result in increased capabilities of the F-2 (flts 3, 4) pay-
load. Since the band 1 receiver is the same except for these modifications,
the description given in Section 2 is not repeated here. The receivers for
bands 3b and 3c are used for the first time in F-2 (flts 3, 4) payloads and
are described below.

The receiver for each band provides the necessary outputs to the data hand-
ling circuits: namely, signal video, inhibit video, standard "accept," and
acceptable pulses. The signal video pulse is used for PW and amplitude
measurements. Both the signal and inhibit video pulses are used for ampli-
tude difference measurements. The accept pulse is a standard 5-μsec
pulse, generated when the signal video amplitude exceeds the inhibit video
amplitude by a preset threshold amount. The accept pulse is used for data
handler control and PRF measurement. Acceptable pulses are supplied to
the single-frequency sequential detector.

Preliminary receiver scan characteristics of the F-2 (flts 3, 4) receivers
are shown in Table 3-1.

3.2.1 Preselectors

Preselector design concept and the band 1 preselector are discussed in
paragraph 2.2.1. A general schematic of the lumped-constant type of pre-
selector is shown in Figure 3-3. In band 3b the image attenuation is greater
than 20 db, the bandwidth is 15 Mc, and the insertion loss is less than 0.8 db.
In band 3c (Figure 3-4) the image attenuation is greater than 20 db, the band-
width is 16 Mc, and the insertion loss is 1 db.

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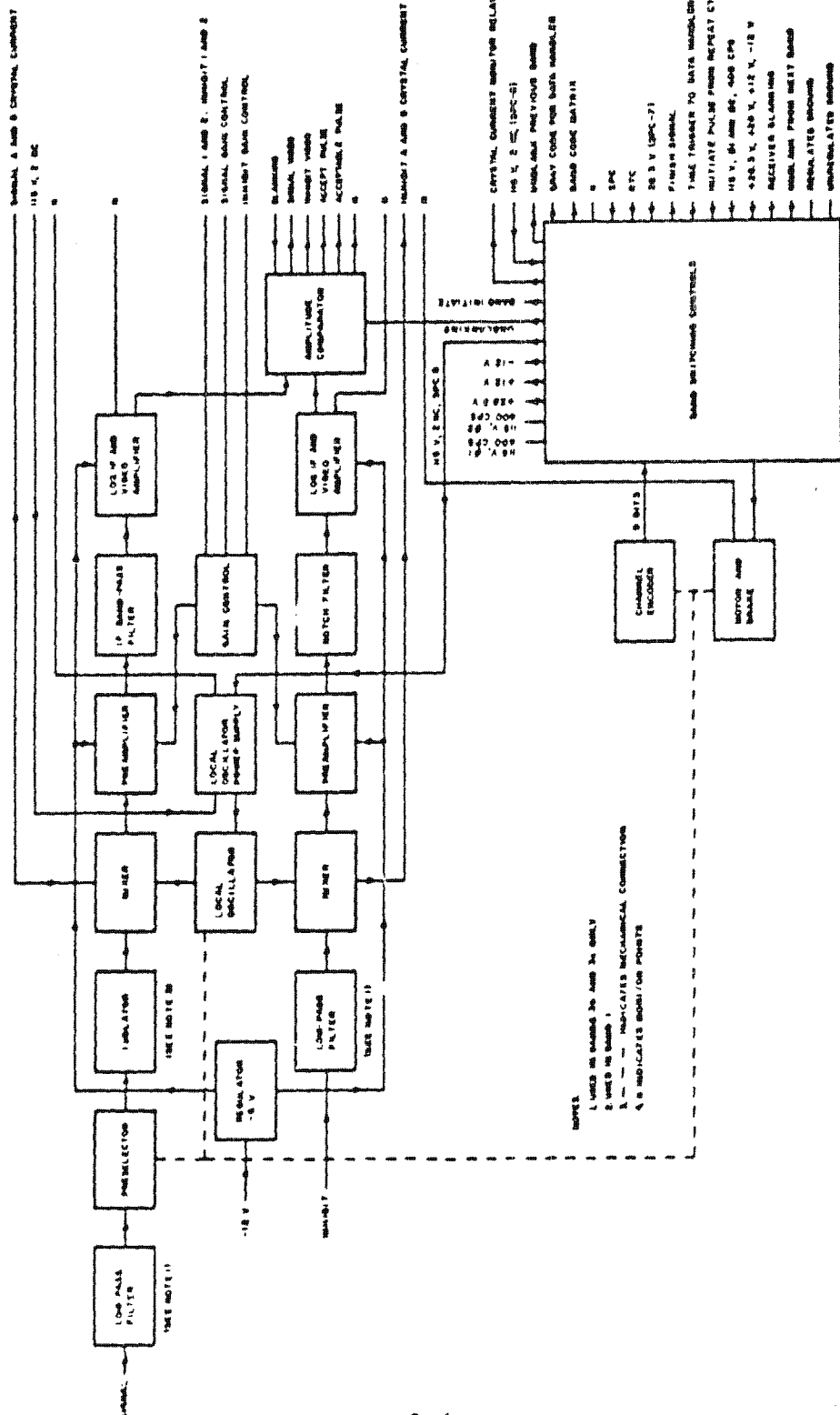
Figure 3-2 Block Diagram of F-2 (Flts 3, 4) Receivers

3-4

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Table 3-1

RECEIVER SCAN CHARACTERISTICS FOR F-2 (FLTS 3, 4) SYSTEM

Priority Number	Frequency Range (Mc)	Minimum PRF (pps)	Time per Channel (seconds)	Channel Width (Mc)	Number of Channels	Time in Band (seconds)
3b	130 to 290	80	0.0375	2.5	64	2.4
3c	290 to 650	80	0.0375	2.5	144	5.4
1	2500 to 3200	200	0.015	2.5	280	4.2
						12.0

Total Band Switching Time: About 1.8 seconds

Total Cycle Time: About 13.8 seconds

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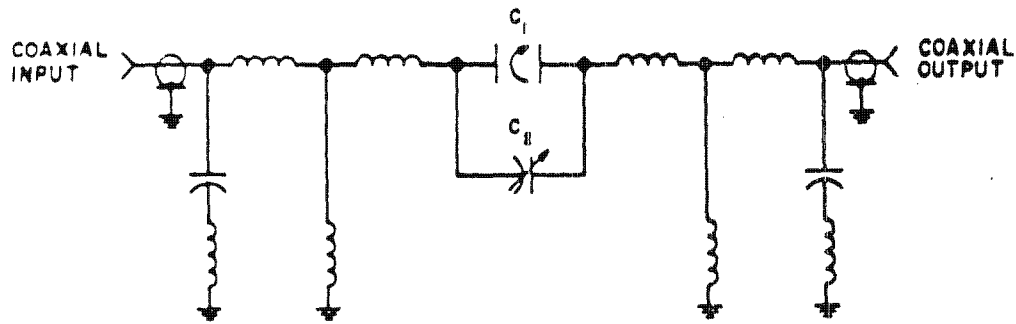
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Figure 3-3 Schematic Diagram of Lumped-Constant Preselector
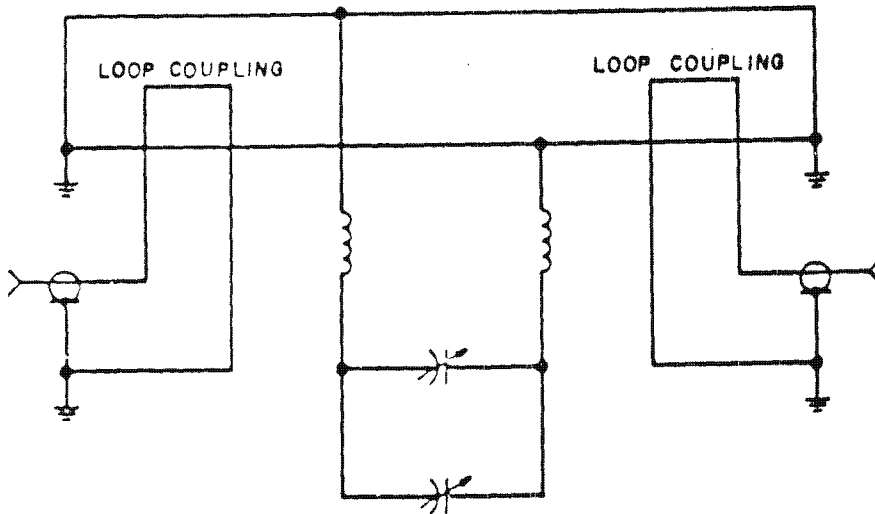
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Figure 3-4 Schematic Diagram of Preselectors for Band 3c

3-6

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3.2.2 Local Oscillator

Band 1 local oscillator information is given in paragraph 2.2.2. Band 3b uses a type 2N1143 transistor in an oscillator circuit. A vacuum tube oscillator circuit employing a GE 7077 triode is used for band 3c. Schematic diagrams are shown in Figures 3-5 and 3-6.

3.2.3 Mixers

Mixer design concept and band 1 mixers are discussed in paragraph 2.2.3. A lumped constant mixer using ferrite cores for the transformer and hybrid circuits has been designed for use in the band 3b mixer (Figure 3-7). It has a 1.5 to 1 SWR in the R-F band and requires 2 milliwatts of local oscillator power. The band 3c mixer is a Tyminski-Hylas hybrid ring. Ferrite transformers are used to match the crystals to the ring. An SWR of better than 2 to 1 is achieved in this configuration shown in Figure 3-8.

3.2.4 I-F Amplifiers

Although the appearance of the log I-F strips used in the F-2 (flts 3, 4) receivers is similar to that of the strips for the F-2 (flts 1, 2) receivers (see paragraph 2.2.4), some changes (to increase bandwidth) have been made in the circuits. The circuit used in this model of I-F strips is therefore shown in Figure 3-9. The bandwidth characteristics of the I-F filters are shown in Table 3-2. The filters are designed for 50-ohm source and load impedance. The insertion loss is less than 5 db and the SWR is less than 1.2. At minimum insertion loss the response does not deviate more than 0.2 db from a maximally flat (Butterworth) response.

To help discriminate against spurious responses in the signal channel, it is desirable to make the inhibit channel bandwidth as wide as possible. For the inhibit channel, a notched filter is being considered as an alternate to the pass-band filter described above. This filter (60-Mc center frequency) has the attenuation characteristics shown in Figure 3-10. Comparative tests on receivers with the two types of filters will determine which filter provides
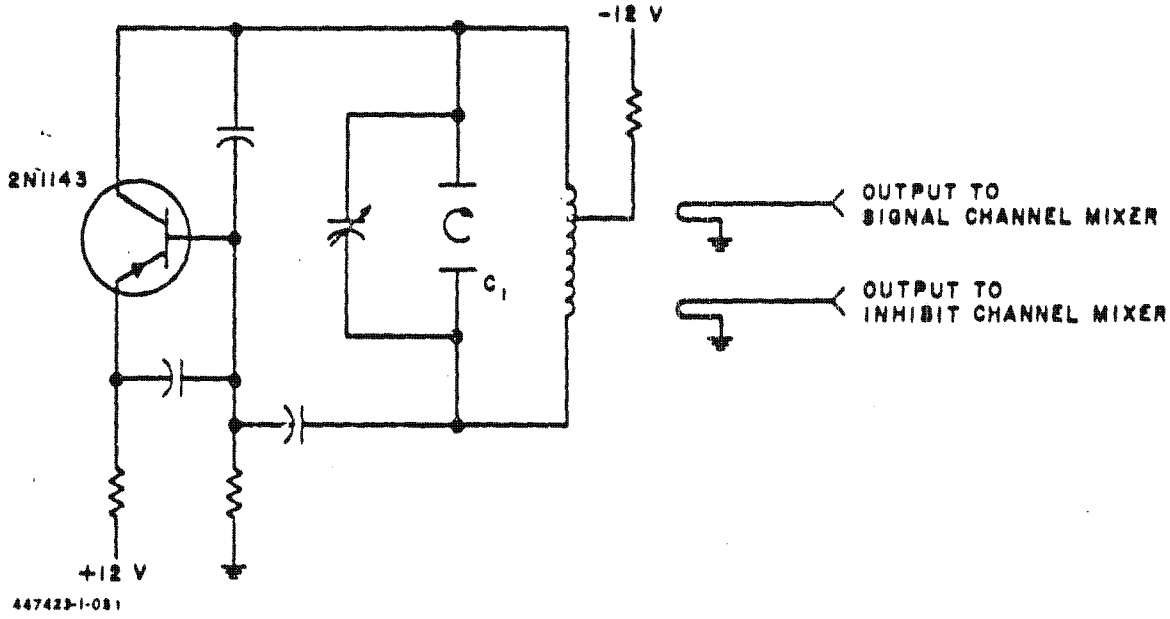
Figure 3-5 Schematic Diagram of Band 3b Local Oscillator
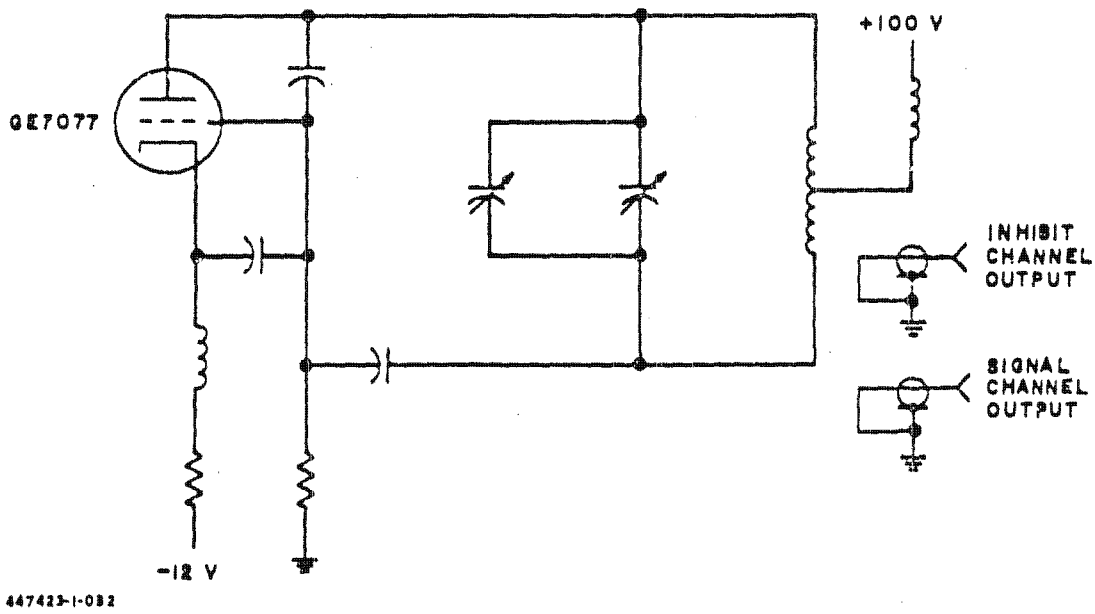
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Figure 3-6 Schematic Diagram of Band 3c Local Oscillator
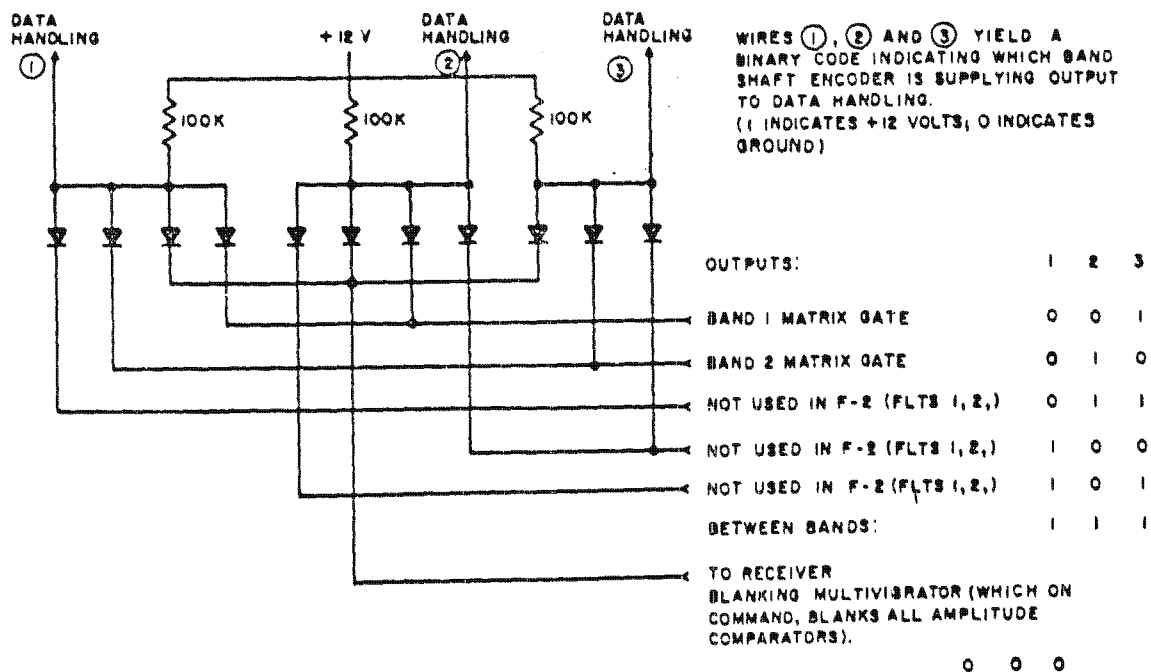
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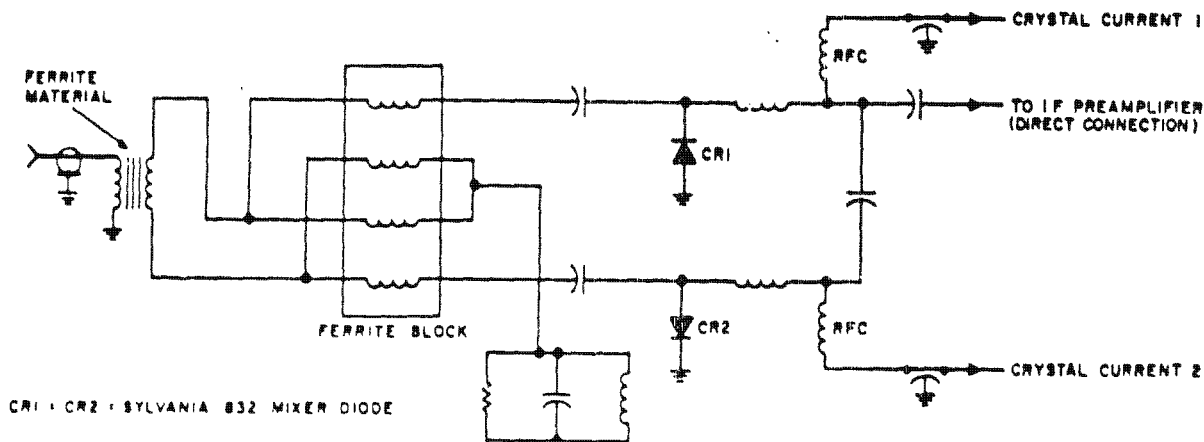
Figure 3-7 Schematic Diagram of Band 3b Mixer
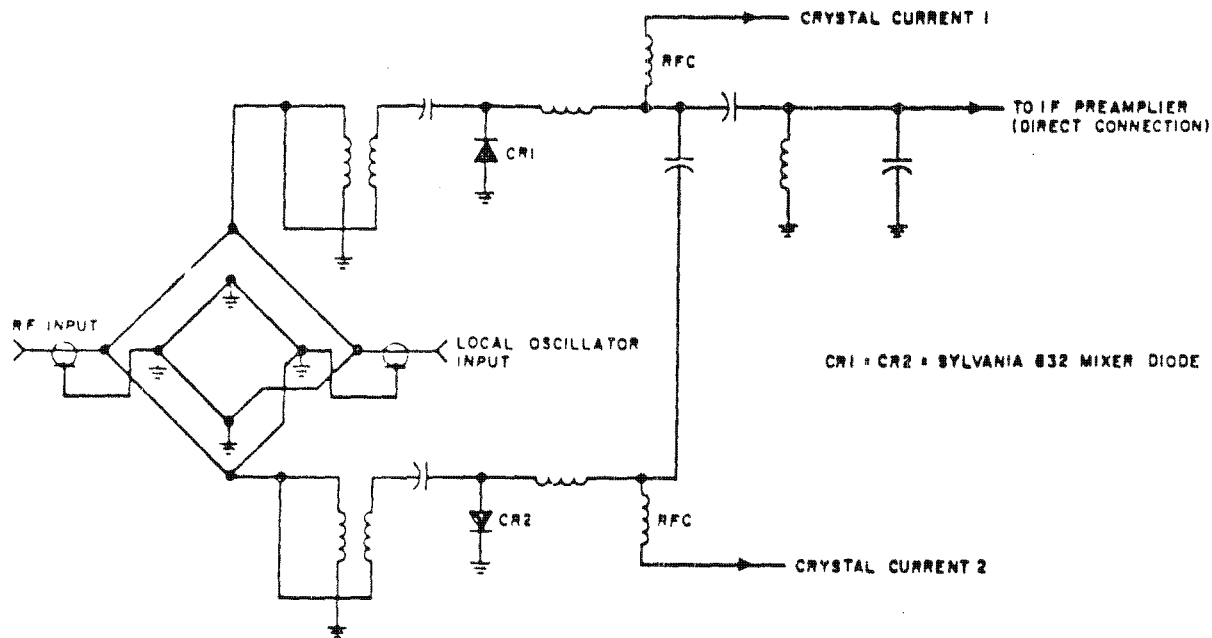
Figure 3-8 Schematic Diagram of Band 3c Mixer

3-9
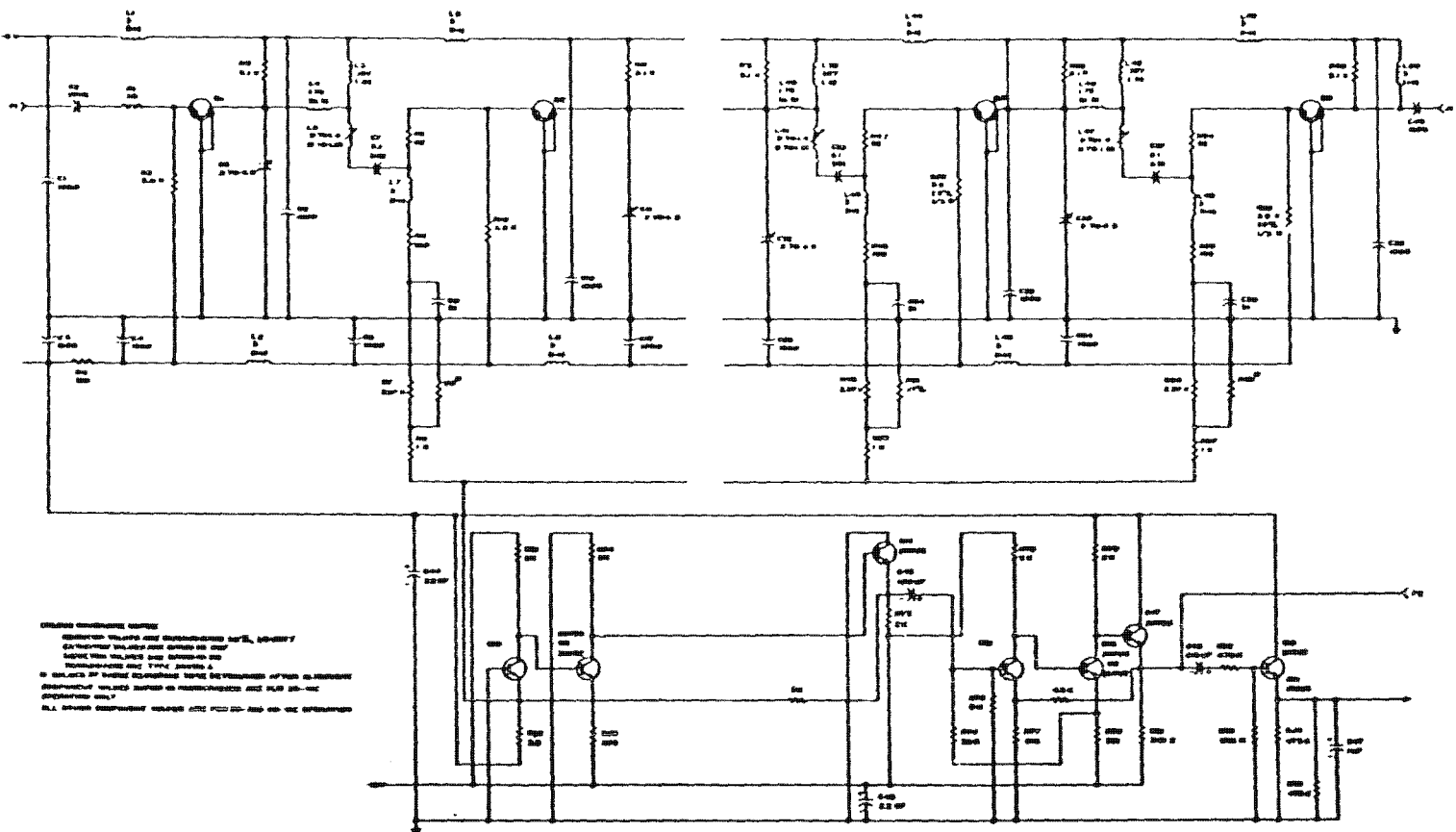
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Figure 3-9 Schematic Diagram of Log I-F Strip For F-2 (FLTS 3, 4) Receivers
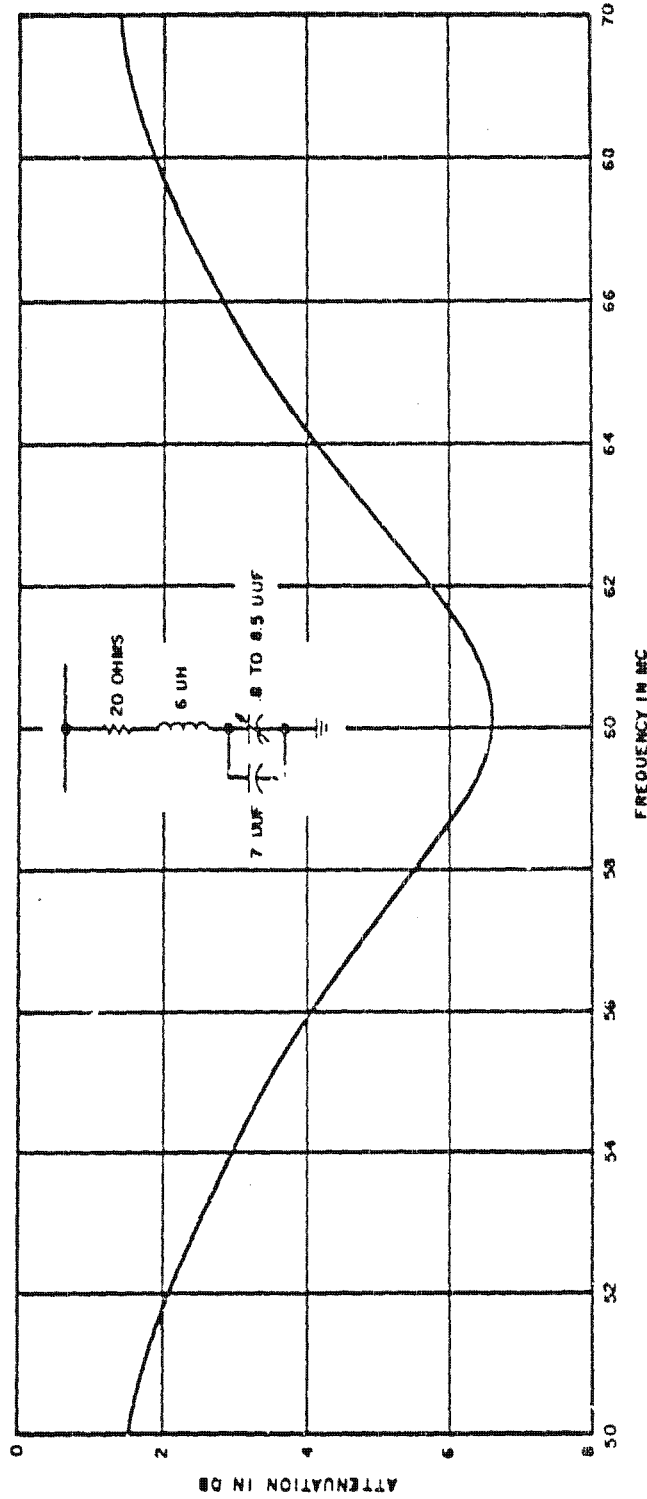
Figure 3-10 Characteristics of Notch Filter

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3-11

the more desirable performance. Characteristics of the preamplifiers and log I-F amplifiers are listed in Tables 3-3 and 3-4.

Table 3-2

BANDWIDTH CHARACTERISTICS OF I-F FILTERS FOR
F-2 (FLTS 3, 4) BANDS 1, 3B, AND 3C

3-db Bandwidth		60-db Bandwidth		
Signal (Mc)	Inhibit (Mc)	Signal (Mc)	Inhibit (Mc)	Center Frequency (Mc)
2.5 ± 0.2	4.0 ± 0.3	$6.5 \begin{smallmatrix} +1.5 \\ -1.0 \end{smallmatrix}$	$14.0 \begin{smallmatrix} +2.0 \\ -1.0 \end{smallmatrix}$	60 ± 0.4

Table 3-3

CHARACTERISTICS OF 60-MC I-F PREAMPLIFIERS

Gain	30 ± 1 db
3-db bandwidth	13 ± 1 Mc
Noise figure (50-ohm input impedance)	6 db
Saturation deviation with input of -30 dbm	1-db max
Response to 30-Mc signal at -30 dbm level	29 db below 60-Mc signal response
Respone to 30-Mc signal at -50 dbm level	30 db below 60-Mc signal response

3.2.5 Amplitude Comparator

The amplitude comparator indicates whether or not a signal originates within the desired region of coverage by comparing the amplitudes of the video pulses from the signal and inhibit channels. A difference bias determines the amount by which the amplitude of the signal channel pulse must exceed that of the inhibit channel pulse to produce an accept signal condition.

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Table 3-4

CHARACTERISTICS OF 60-MC LOG I-F AMPLIFIERS

Input dynamic range	-70 to -10 dbm
Output dynamic range (video)	1 to 10 v
3-db bandwidth (I-F)	8 ± 1 Mc
Maximum deviation from log transfer characteristics at center frequency	0.1 v
Maximum deviation from log transfer characteristics at 60 ± 2.5 Mc	0.2 v
Maximum tracking error of matched pair at 60 ± 2.5 Mc	0.2 v

If the signal-to-inhibit amplitude ratio exceeds the threshold level, the comparator generates a 10-v acceptable pulse having a PW equal to the interval during which the threshold is exceeded. The acceptable pulse initiates a 5-v, 5-μsec accept pulse that can have a repetition rate not greater than one per 35 μsec. Thus several acceptable pulses can be generated for each accept pulse. The accept pulse, the acceptable pulses, and buffered video signal and inhibit channel pulses are the outputs from the amplitude comparator to the data handling and recording circuits.

The amplitude comparator (Figure 3-11) consists of a difference amplifier, Schmitt trigger, and blocking oscillator. The difference amplifier consists of Q1, Q2, and Q3, and will operate with Q3 normally cut off by an amount equal to the threshold setting. The output of Q3 is diode coupled to Q6 which inverts and drives the Schmitt trigger circuit consisting of Q7 and Q8. The design of this Schmitt trigger is dictated by the dual requirements of direct coupling and referencing the output to ground. This output (the acceptable pulse) is then buffered (Q9) to drive a cable and differentiated (Q8) to drive the blocking oscillator. The blocking oscillator, having fired, is blanked by its own negative overshoot that holds its base negative for 35 μsec. This blanking period is determined by R28, R29, and CR13.

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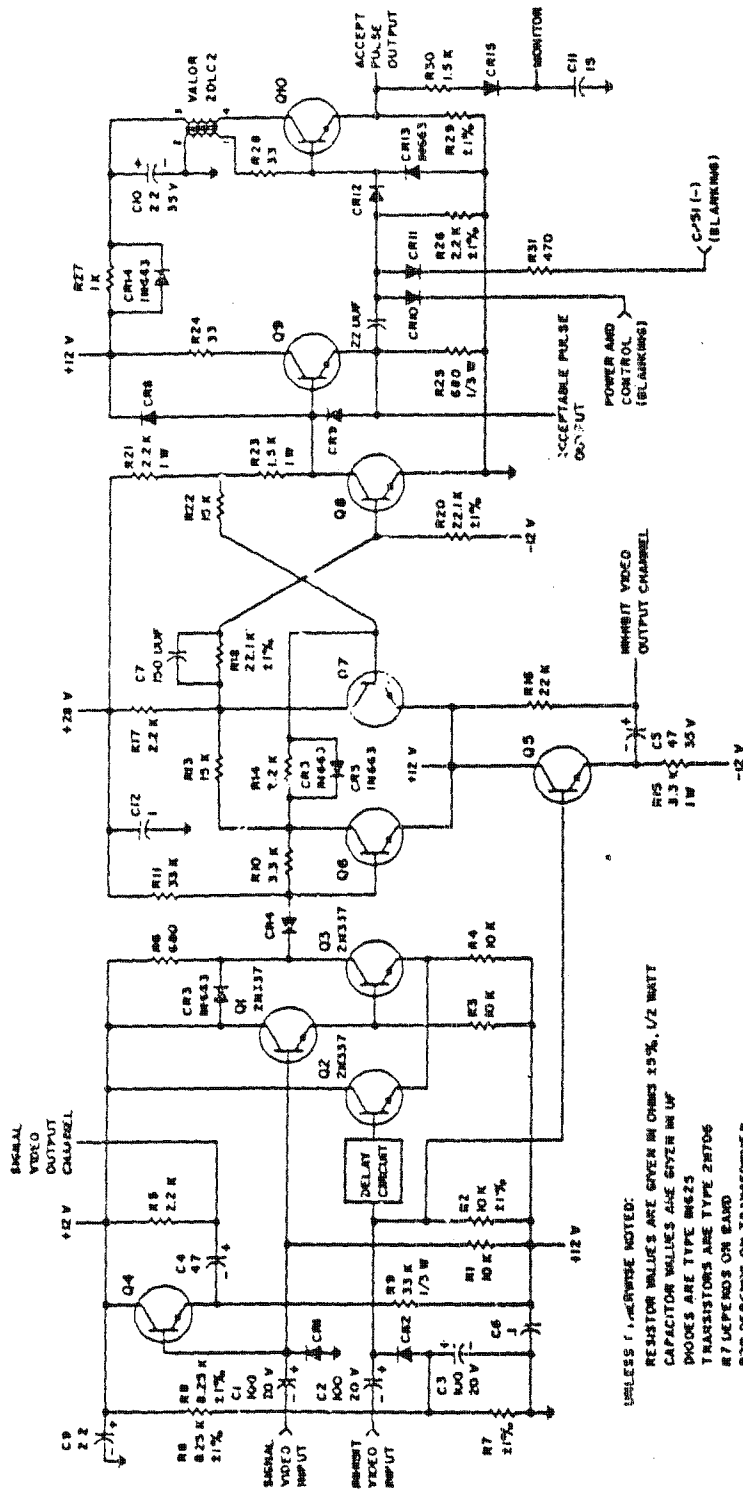
Figure 3-11 Schematic Diagram of F-2 (Flts 3, 4) Amplitude Comparator

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A delay network is inserted in series with the base of Q2. This network delays the inhibit video to the same extent that the signal video has been delayed in the signal channel pass-band filter, and degrades the inhibit rise time to match that of the signal video. Additional blanking inputs function during band switching and data handler reset periods.

Q4 and Q5 are the signal and inhibit cable drivers. The need for a low resistance to shunt the cable capacitance (150 $\mu\mu$ f) together with the transistor power limitation, dictates the capacitance coupling (C4 and C5) that limits the duty cycle capability to 15 percent. The generation of accept and acceptable pulses, however, is independent of the duty cycle.

3.2.6 Frequency Encoder

The 9-bit encoder used in all F-2 receivers provides 512 frequency channels. The number of channels required, however, depends on the bandwidth of each receiver. Band 1 receiver requires 280 channels, band 3b receiver requires 64 channels, and band 3c receiver requires 144 channels. The frequency encoder provides adequate frequency resolution. A description of the encoder is given in paragraph 2.2.7.

3.3 PAYLOAD DATA HANDLER

The payload data handler is a transistorized digital system that provides the necessary data handling functions required in the ferret equipment. The data handler examines the video pulses from the payload's ferret receivers and:

a. Determines the acceptability of the signals (verification) in those bands where verification is desired

b. Measures the pulse interval to determine PRF

c. Notes when variable PRF occur

d. Measures PW and pulse amplitude of signals

e. Notes when pulses longer than 32 μ sec have been measured

f. Reads out the frequency channel code from the shaft encoders in the receivers, and the frequency band code from the band code matrix

g. Notes the time of intercept

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h. Measures the difference in amplitude of signal and inhibit pulses

i. Notes reception of single frequency sequential pulses

j. Expresses the above information in digital form--a 68-bit digital word

Figure 3-12 is a simplified block diagram of the data handler, and Figure 3-13 shows the digital word format. The data handler can be divided, according to function, into several sections:

a. Verification, PRF, and PW Measurement. This section determines whether the signal received is a valid intercept, and if so, generates binary words representing PW and PRF, or more correctly, pulse interval. Figure 3-14 is the logic diagram for this section.

b. Complement Counter. This section notes pulse interval difference to detect variation in PRF. If nonuniform PRF is detected, an alarm bit is generated. Figure 3-15 is a logic diagram of the complement counter. Figure 3-16 is the timing diagram.

c. Frequency and Time. For each intercept, this section accumulates time bits, enables readout of frequency shaft encoders and readout of band code matrix. Figure 3-17 is the logic diagram of this section.

d. Pulse Amplitude Digitizer and Amplitude Difference Digitizer. This section measures the amplitude of the signal channel video signal and the difference between the signal and inhibit channel video signals. Figure 3-18 is the logic diagram for these units.

e. Single Frequency Sequential. Upon detection of this special signal an alarm bit is generated. Figure 3-19 is the logic diagram for this unit.

f. Data Sampler and Reset Control. This section causes the stored binary data in the preceding circuits to be fed to the recording circuits in serial order. Figure 3-20 is the logic diagram for the sampler and control.

g. Digital Recorder Control. This section controls the start-stop-record cycles of the digital recorder, and shapes, combines, and distributes data pulses going to and from the recorder. Figure 3-21 is the logic diagram for the recorder control.

3.3.1 Operation of Verification

In the bands where verification is used, accept pulses from the amplitude comparator are subjected to a verification test before their characteristics are recorded. This test prevents noise pulses that occasionally will occur from being considered as received radar pulses. For a signal to be

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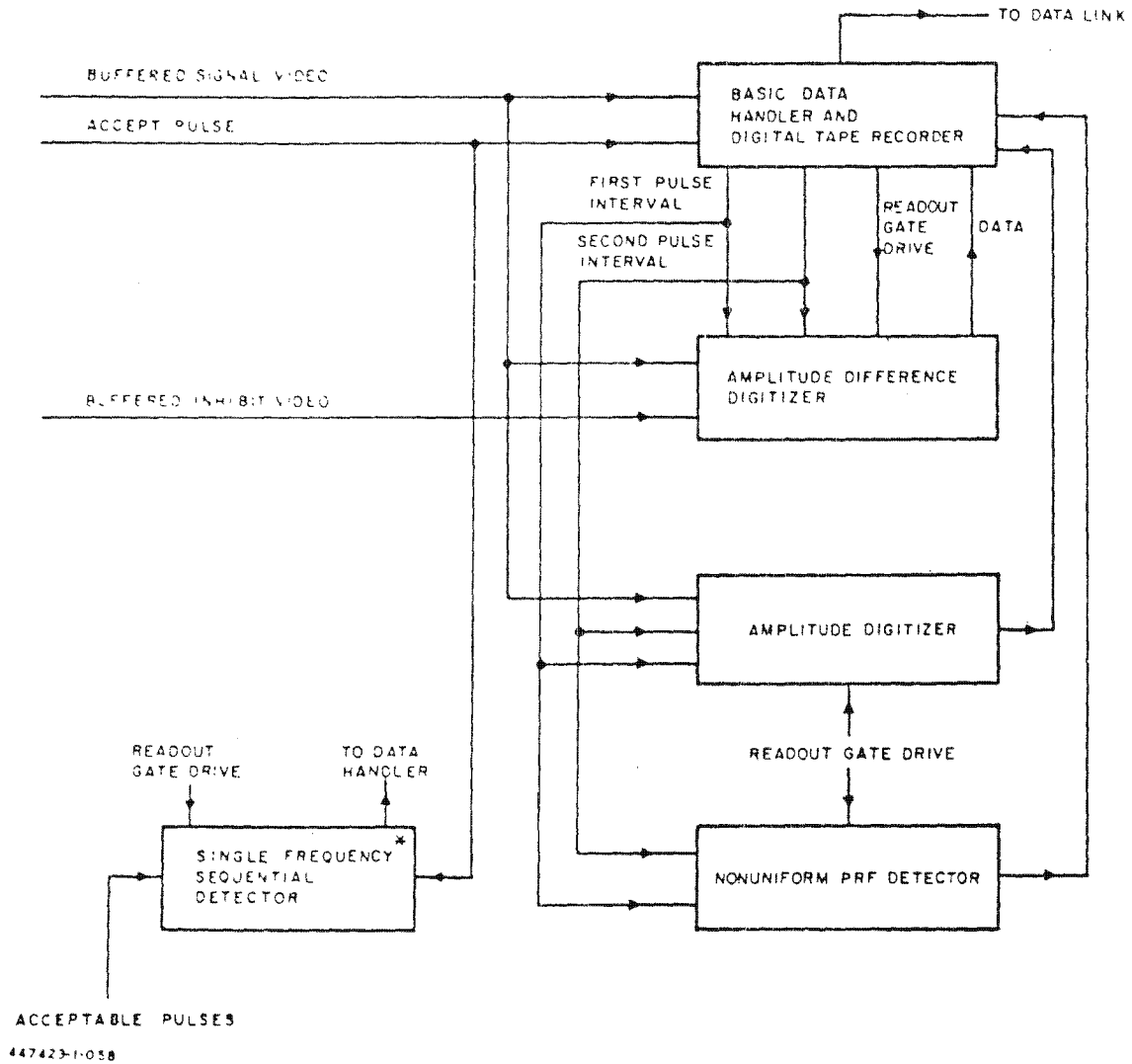
Figure 3-12   Block Diagram of F-2 (Flts 3, 4) Payload Data Handler

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NUMBER OF BITS	BIT NUMBER	
9	1 - 9	PRF - 1
6	10 - 15	PULSE WIDTH
5	16 - 20	PULSE AMPLITUDE
3	*21 - 23	AMPLITUDE DIFFERENCE
1	24	NONUNIFORM PRF
1	25	WIDE PULSE (>32 USEC)
1	*26	SINGLE - FREQUENCY SEQUENTIAL PULSE
1	*27	SIMULTANEOUS MULTIFREQUENCY PULSE
6	28 - 33	SPARES
9	34 - 42	PRF - 2
13	43 - 55	TIME
9	56 - 64	FREQUENCY
3	65 - 67	BAND
1	68	PARITY

NOTE.
   THE SYSTEM RESETS ON CLOCK PULSES 69 AND 51
   *THESE ARE SPARE BITS IN F-3a EQUIPMENT
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Figure 3-13 F-2 (Flts 3, 4) Digital Data Format

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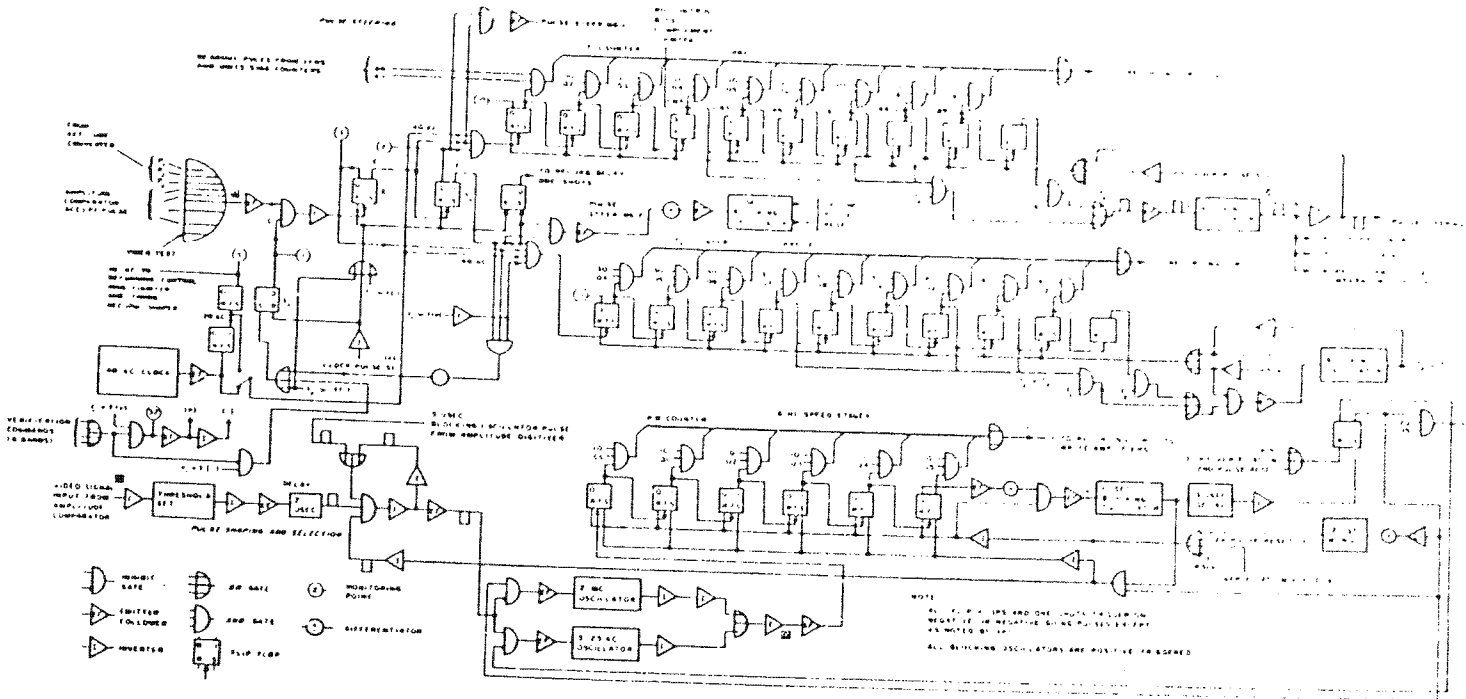
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Figure 3-14 Logic Diagram: Verification, PRF, and PW
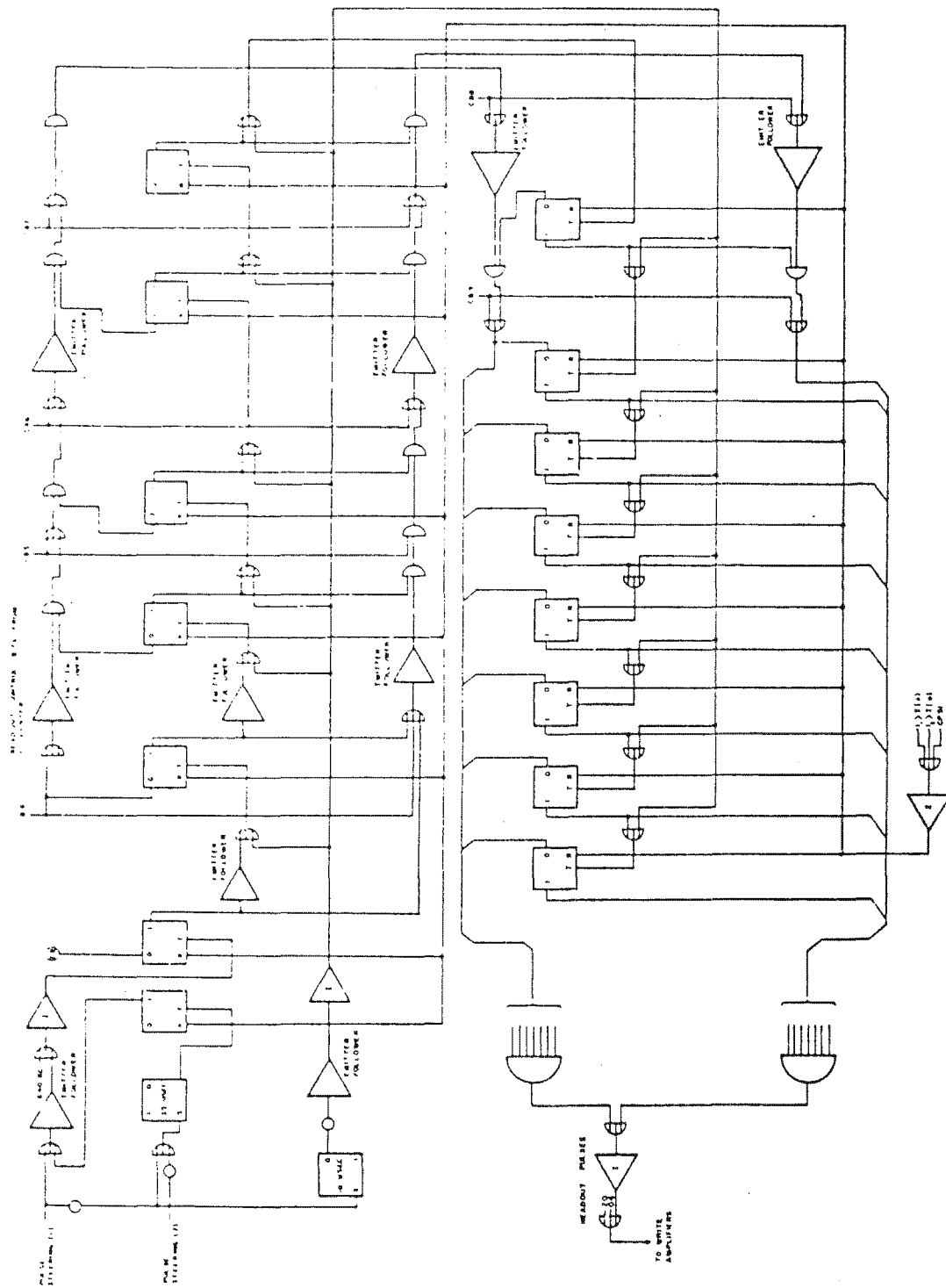
Figure 3-15 Logic Diagram: Complement Counter (Nonuniform PRF)

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t_1 GATE

t_2 GATE

CLOCK DELAY
MONOSTABLE MULTIVIBRATOR

25 USEC   25 USEC

GATED CLOCK
PULSE ENVELOPE

25 USEC

COMPLEMENT PULSE INPUT
(COMPLEMENT DELAY
MONOSTABLE MULTIVIBRATOR)

10 USEC

COMPLEMENT PULSE

5 USEC

OUTPUT ($t_1 \cdot t_2$)

OUTPUT ($t_1 \cdot t_2$)

READOUT DURING
THIS INTERVAL

RESET
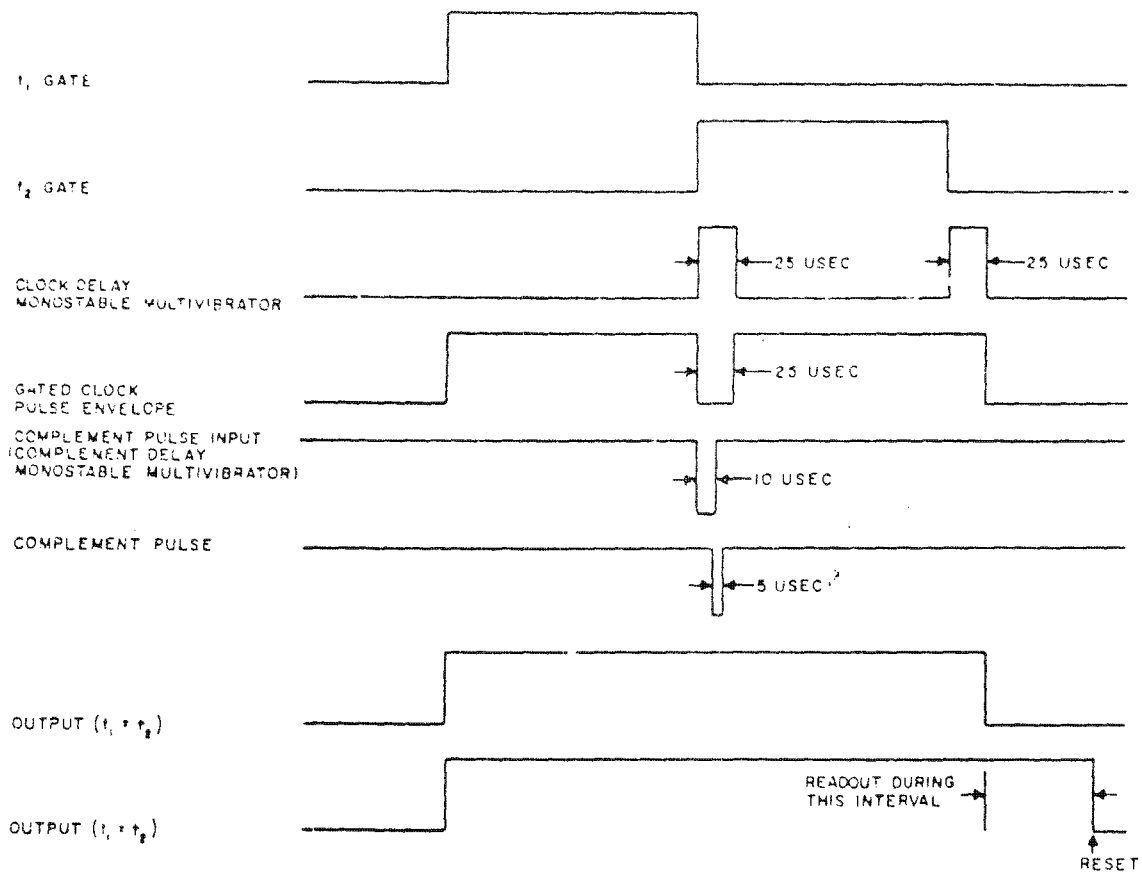
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Figure 3-16 Timing Diagram of Complement Counter

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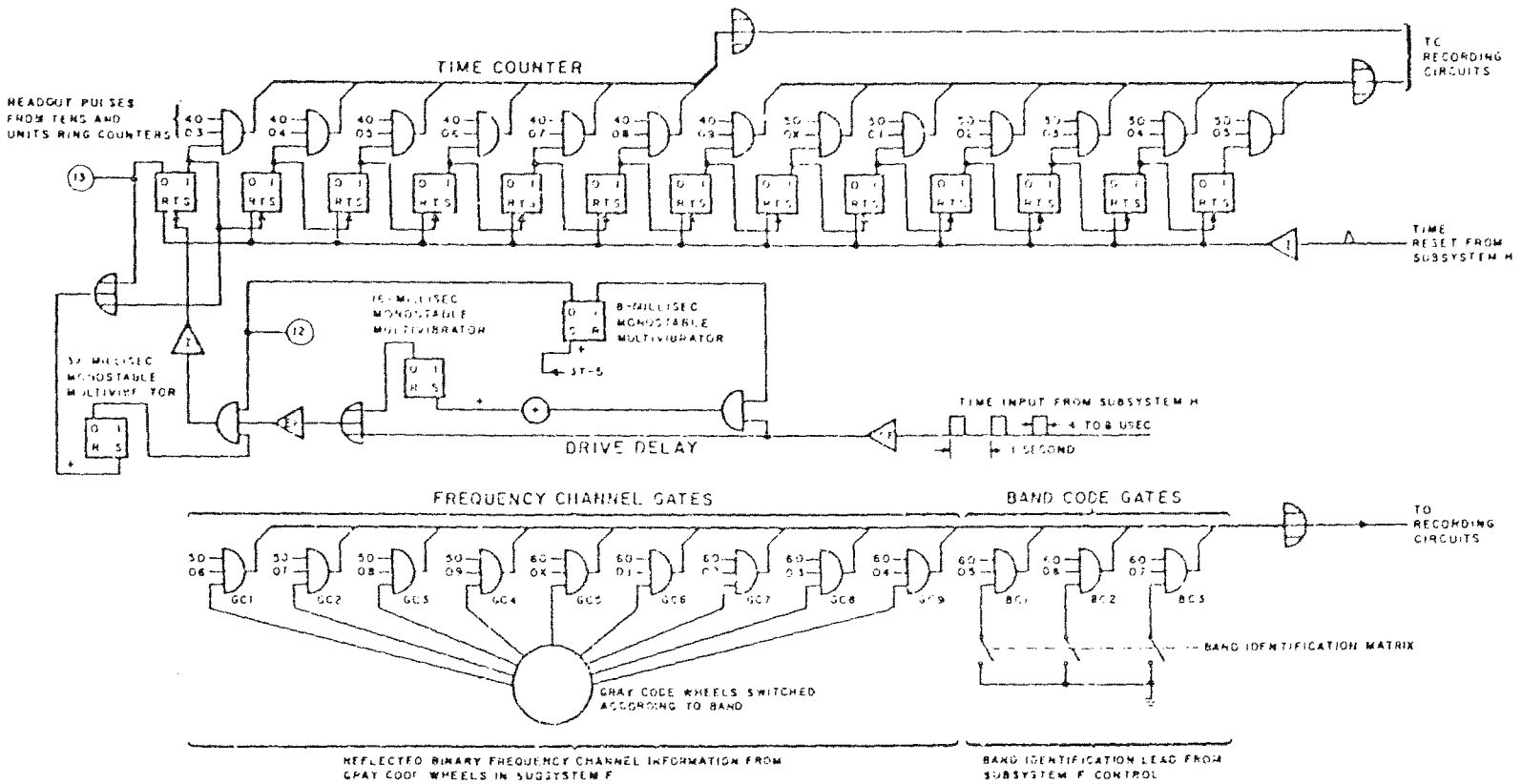
Figure 3-17 Logic Diagram: Frequency and Time

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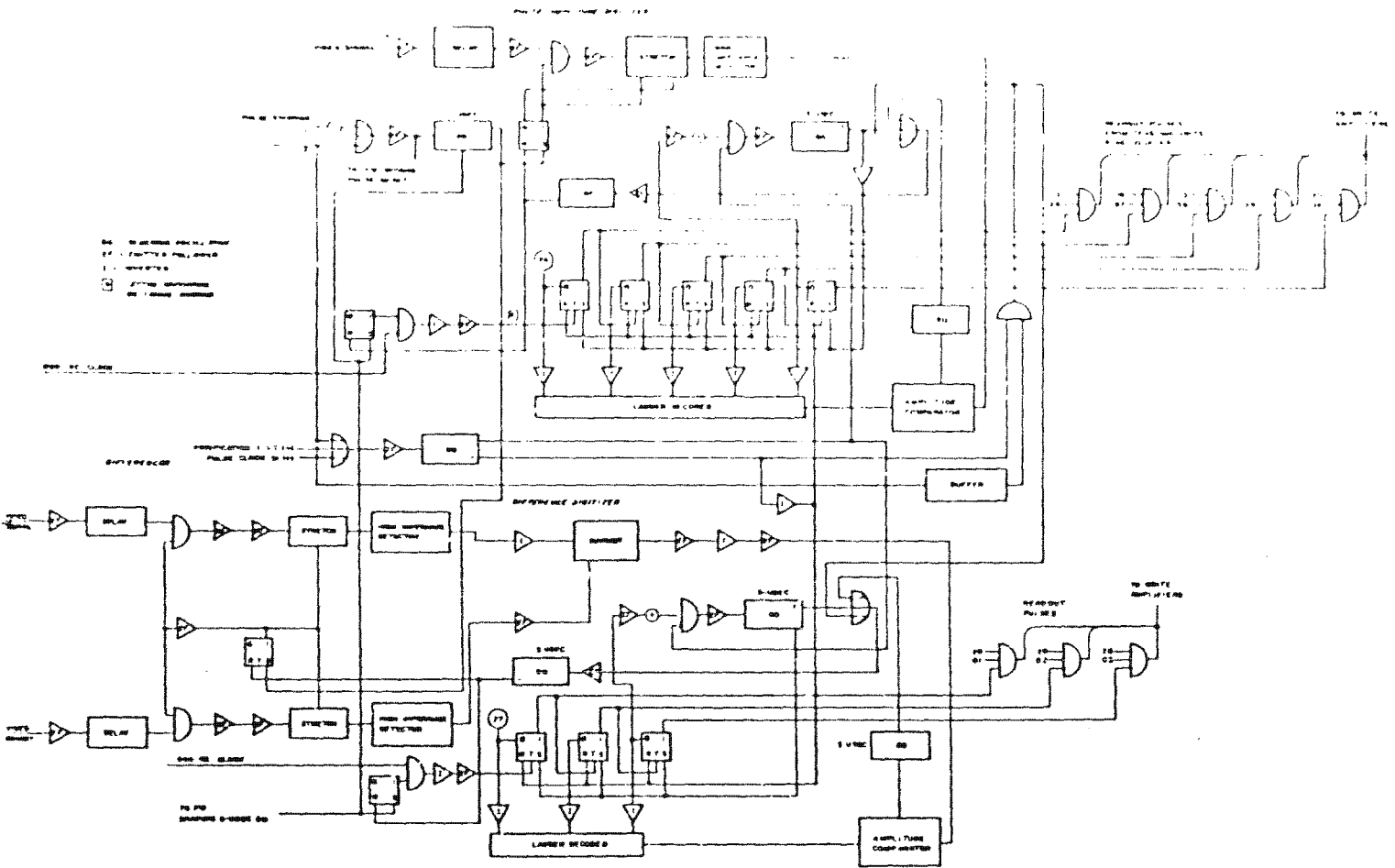
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Figure 3-18 Logic Diagram: Pulse Amplitude and Amplitude Difference
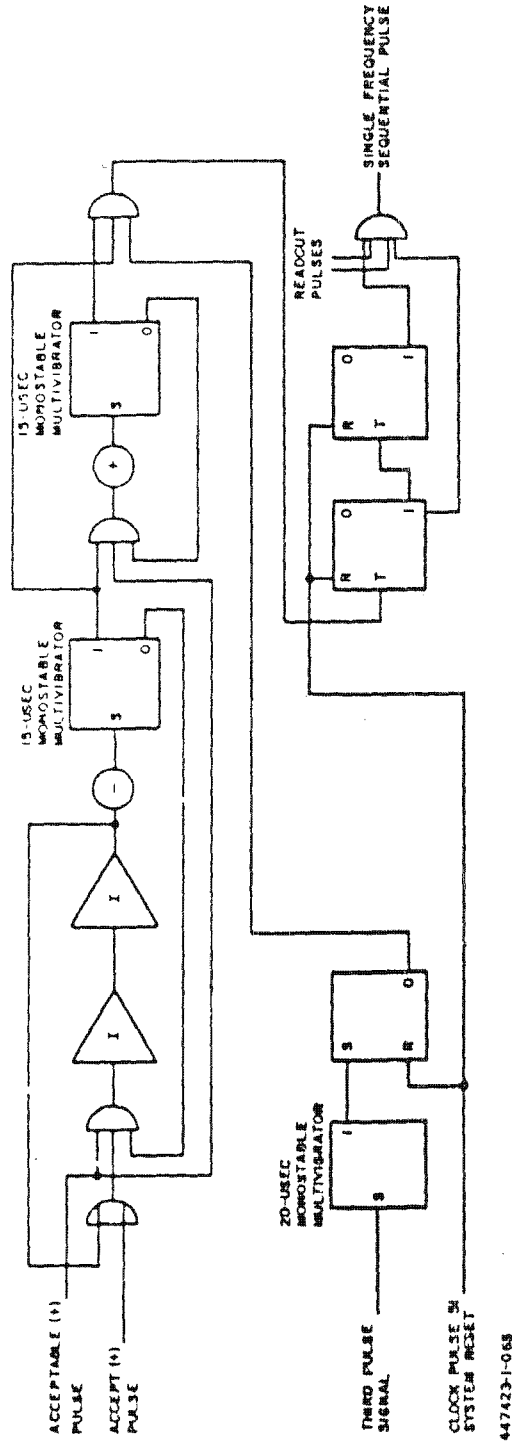
Figure 3-19 Logic Diagram for Single-Frequency Sequential Pulse Detector

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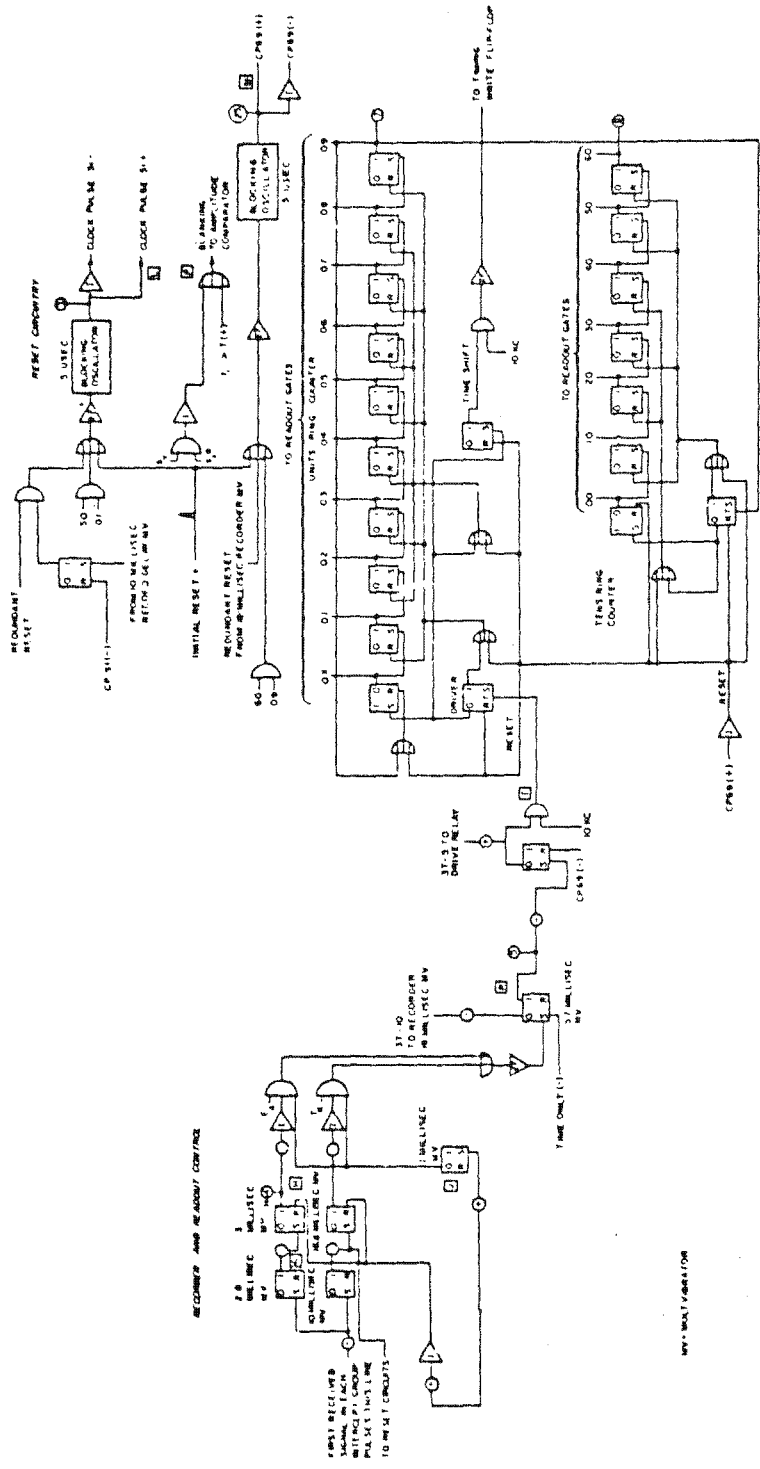
Figure 3-20 Logic Diagram: Data Sampler and Reset Control

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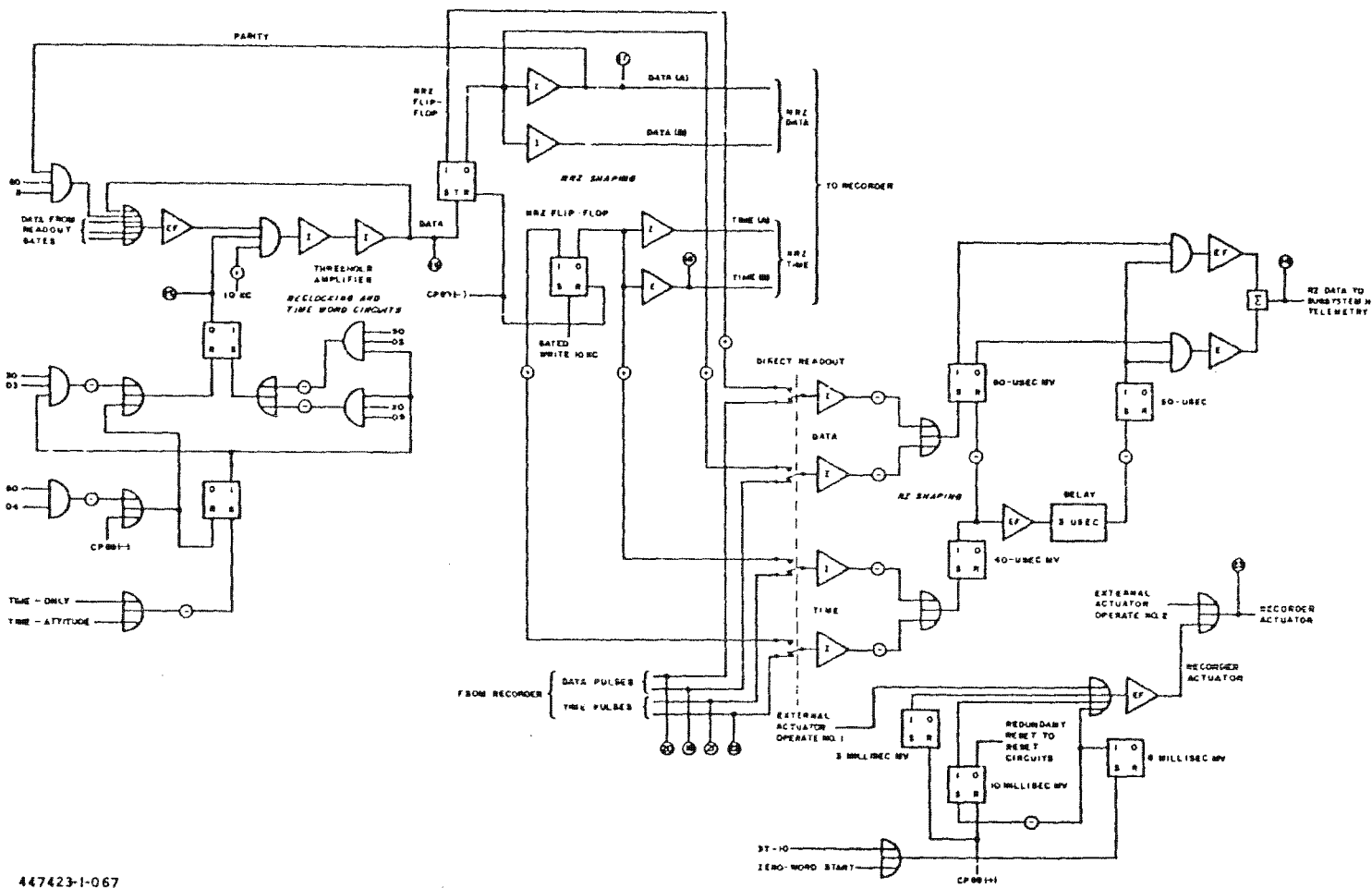
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Figure 3-21 Logic Diagram: Controls for Recorders

recorded as an intercept, at least two pulses must be received within a period of time equal to the longest interpulse period expected in the particular band under investigation.

The verification times (one maximum pulse period) for the receivers are:

Band	Time (milliseconds)	Minimum PRF (PPI)
1	5	200
3b	12.5	80
3c	12.5	80

If a signal is not verified, the data handler is reset and prepared to accept the next signal. This verification technique, however, is not incorporated in bands where single pulses are processed. When the system is operating in the single-pulse mode, the receiver gain can be decreased to diminish the number of spurious noise signals. While operating in this mode, the equipment is capable of receiving frequency jumper type radars. This mode is not optional after the payload has been launched. The single-pulse mode operation requires a wiring change in the data handler prior to launch.

3.3.2 Measurement Cycle

3.3.2.1 PRF Measurement. The PRF measurement cycle consists of the measurement of the intervals between the first and second pulses and between the second and third pulses. Two-pulse interval measurements are made to detect either the presence of two or more radars within the frequency channel or PRF modulation. Additionally PRF measurement reliability is increased by the use of two counters. The equipment also generates (via the complements counter) and records unmatched PRF alarms when a second PRF measurement is not within 1 percent of the first (except for very short pulse intervals). The readout accuracy of the complements counter is shown in Table 3-5. In addition the equipment is capable of single-pulse operation in selected bands for the purpose of detecting frequency-jumping radars that change frequencies from pulse to pulse. When the equipment is in

Table 3-5

READOUT ACCURACY OF COMPLEMENT COUNTER WITH 40-KC T_1 CLOCK

Largest T_1 Counter Bit Acceptable for Range	Readout Control Bus Number	Range of T_1 (μsec)	$\dfrac{T_2 - T_1}{}$		
			Difference Counts	Accepted μ sec	Percent
1, 2, 3, 4	0	100 - 375	±2	3.12	6.2 - 0.84
5	1	400 - 775	±4/3	4.53	1.1 - 0.59
6	2	800 - 1575	±8/7	10.9	1.4 - 0.69
7	3	1600 - 3175	±15	23.4	1.5 - 0.74
8	4	3200 - 6375	±31	48.4	1.5 - 0.76
9	5	6400 - 12,750	±63	98.2	1.5 - 0.77

Clock = 640 kc

the single-pulse mode of operation and only one pulse is received during the maximum time interval, the PRF-1 counter is automatically reset at the end of the interval. The PRF counters operate with 25-μsec increments with a maximum count of 12.5 milliseconds.

3.3.2.2 <u>PW Measurements</u>. The PW measurement is made on the first pulse, and when a second pulse occurs during the verification time, the width of the second pulse is measured. This second measurement will supersede the first. The PW counter has a measuring capability of $0.5\,\mu$sec to slightly over 2 milliseconds. PW's between 0.5 and $31.5\,\mu$sec are measured in 0.5-μsec increments by means of a pulsed 2-Mc oscillator. If the PW exceeds $31.5\,\mu$sec, an alarm is generated and the 6-stage counter is reset. The next count occurs at $50\,\mu$sec, giving greater accuracy in the range between 31.5 and $50\,\mu$sec where the pulses are likely to occur. The PW is then measured in 32-μsec increments by a 31.25-kc pulsed oscillator. Pulses longer than 2.03 milliseconds register as 2.03 milliseconds. A schematic diagram of the oscillators is shown in Figure 3-22.

3.3.2.3 <u>Pulse Amplitude Measurement</u>. A pulse amplitude measurement is made to determine the signal strength of intercepted signals. The pulse amplitude measurement is made on the first pulse and when a second pulse occurs during the verification time, the amplitude of the second pulse is measured and the second measurement supersedes the first. The pulse to be measured is stretched and applied to one input of a voltage comparator while 1280-kc clock pulses are applied to a counter input. The stages of the counter, control constant current drivers that feed a linearly-weighted ladder network whose output is a series of linearly-increasing voltage steps. These series of steps are fed to the other input of the comparator that provides a trigger pulse when the staircase amplitude equals that of the stretched pulse. This trigger pulse stops the counter whose binary content is proportional to the pulse amplitude.

UNLESS OTHERWISE NOTED:
RESISTOR VALUES ARE GIVEN IN OHMS
CAPACITOR VALUES ARE GIVEN IN UUF
TRANSISTORS ARE TYPE 2N338
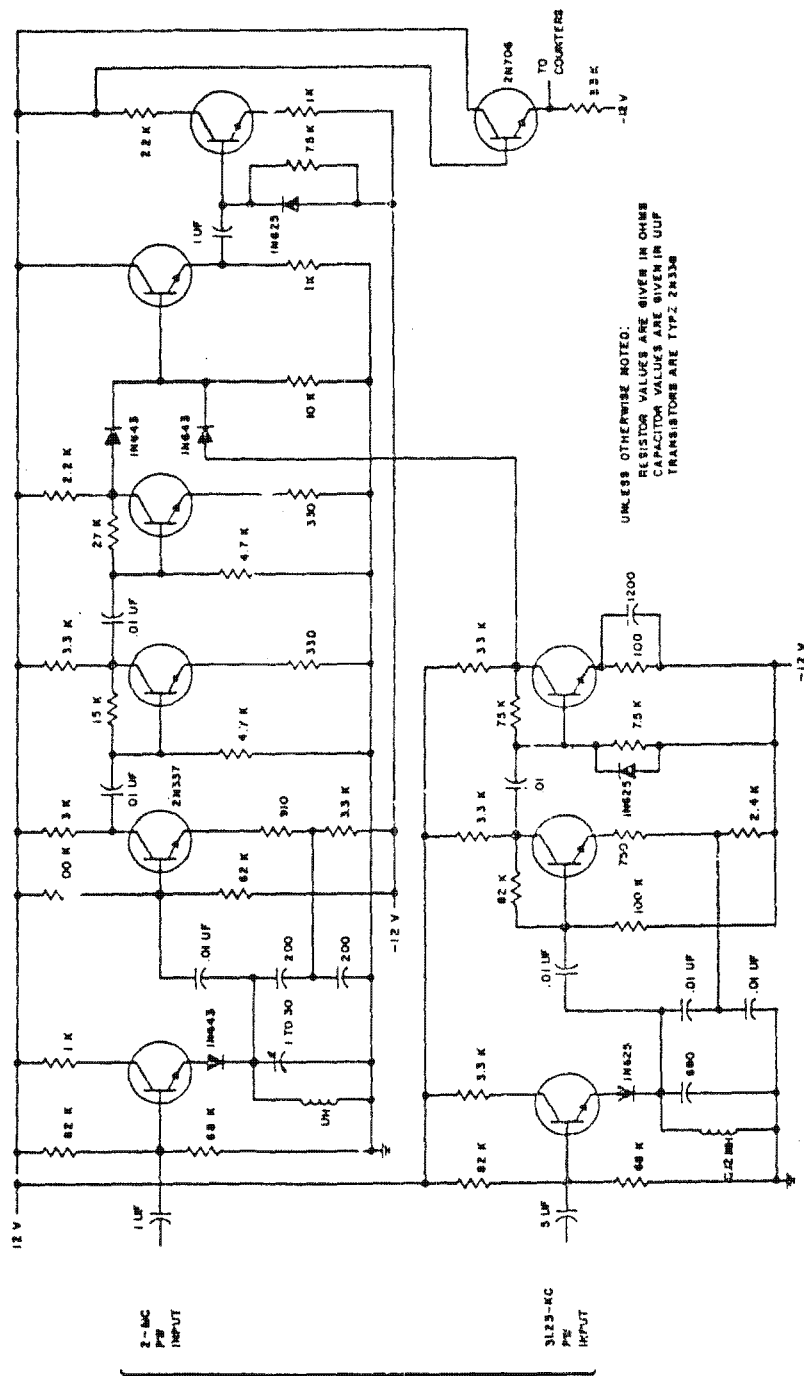
Figure 3-22 Schematic Diagram of 2-Mc And 31.25-kc Oscillators

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3.3.2.4 <u>Pulse Amplitude Difference Measurements.</u> A measurement is
made to determine the difference between the amplitude of the signal channel
video signal and the inhibit channel video signal of an intercept. The pulse
amplitude difference measurement is made on the first pulse and if a second
pulse occurs during verification time, the difference amplitude of the second
pulse is measured and the second measurement supersedes the first. The
signal and inhibit video pulses are fed into a difference network which sup-
plies a video pulse proportional to the difference. The pulse is digitized in a
manner similar to that used in the pulse amplifier digitizer except at a 640-
kc rate.

3.3.3 <u>Single-Frequency Sequential Pulse Detection</u>

The logic diagram of a single-frequency sequential pulse type radar detector
is shown in Figure 3-19. Single sequential pulses are detected as follows.
When an accept pulse is generated, an end-of-pulse trigger is produced at
the trailing edge of the corresponding acceptable pulse. This trigger opens
a 15-μsec gate that samples the acceptable pulse. If at least one pulse oc-
curs during each gate interval for three successive accept pulses, an inter-
cept of the single-frequency sequential type is recorded.

3.3.4 <u>Readout Cycle</u>

The data handler's readout cycle is the interrogation of the counters contain-
ing intercept data, the serialization of these data, and resetting the measure-
ment and verification circuits. A parity-check bit is generated at the end of
this process and appears at the end of the data. After the intercept has been
verified, the digital recorder is instructed to start, and is permitted to reach
proper recording speed. The data then are interrogated and issued to the
recorder's write circuits. The readout process is completed and the entire
data handler is cleared.

The readout of the complete intercept word requires about 7 milliseconds.
Because of this it is necessary to use two reset pulses in the data handler to
meet the channel dwell time and scan rate requirements. Therefore, the

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counter and circuits containing word bits 1 to 42 are reset by CP 51 and are prepared to receive new data. The counters and circuits containing word bits 43 to 68 contain parameters that do not change rapidly as a function of input signal and are reset by CP 69. Although the time counter is in the data handler, it is controlled by the satellite clock and continuously provides satellite time. The frequency encoder and band code matrix are located in the receiver, and the power and control assembly, respectively, and provide continuous frequency and band information to the data handler.

3.3.5 Operation During Typical Intercept

Timing diagrams for those receiver bands using verification are shown in Figure 3-23. Operation is generally the same as that for the F-2 (flts 1, 2) equipment. One exception is that the pulse steering causes PW measurements to be made on the first received pulse. If a second pulse is received, the second pulse is measured and the second measurement supersedes the first. The parity bit for this data handler is bit 68. Clock pulse 69 resets part of the data handler. Other portions are reset by CP 51. Three milliseconds after CP 69 occurs the tape brake is actuated.

3.4 DATA STORAGE

The digital recorder model is that used in F-2 (flts 1, 2) equipment. It is described in paragraph 2.4.

3.5 PAYLOAD CONTROL EQUIPMENT

The control functions are performed by the power and control assembly. It consists of the following subassemblies:

a. Redundant Electronic Timer - This unit controls the band switching cycle when any band drive motor fails.

b. Low-Voltage Power Converter - This unit supplies ±12 v for the transistor circuits in the receivers and data handlers.

c. Internal Programmer - This unit generates the signals that place the start-stop words on the tape, and provides for receiver blanking during the recording of these words.

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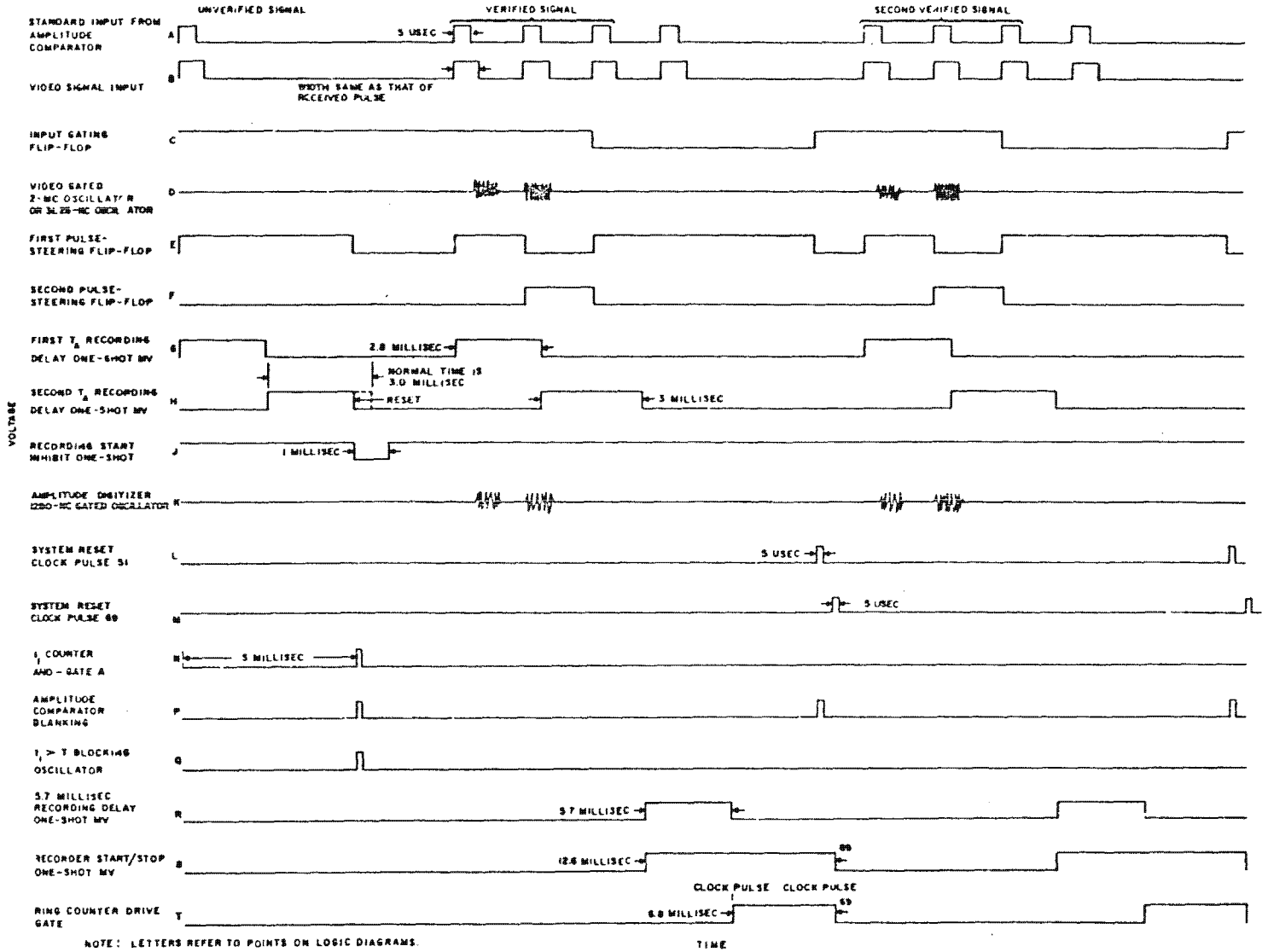
Figure 3-23 Intercept Timing Diagram (for Bands Using Verification)

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d.   Test Generator - This unit provides test signals to check the
     performance of the receivers and/or data handlers.

e.   Auxiliary Command Circuits - This unit contains circuits for con-
     trolling the recorder. It also contains the circuits for switching
     signals from one data handler to the other. Various minor func-
     tions including power monitoring points are also included in this
     unit.

f.   I-F Preamplifier Gain Control - This unit permits the gain of each
     preamplifier to be changed in 1-db steps. Eleven steps and one
     "off" position are provided.

g.   Attitude Converter - The horizon sensor (not part of Subsystem F)
     measures vehicle attitude (pitch and roll) and supplies the data in
     the form of d-c voltages to the Subsystem F attitude converter. The
     converter transforms the d-c voltages into pulse format for digital
     conversion and recording on the digital tape.

h.   Band Code Matrix - This unit provides a digital indication of the
     active scanning receiver.

i.   Crystal Current Monitor - This unit is a set of magnetic amplifiers
     used for amplifying crystal currents to a level suitable for tele-
     metering purposes.

j.   Control Equipment - These units control the basic operation of the
     receiving and data handling equipment. The control equipment is
     operated by RTC's and SPC's supplied by Subsystem C&C in the
     satellite. These commands, in the form of relay contacts, produce
     the required mode of operation.

3.5.1 Modes of Operation

There are five basic modes of operation of the F-2 (flts 3, 4) payloads. The
modes of operation are initiated by a succession of SPC's or RTC's. These
modes are the same as those for the F-2 (flts 1, 2) payloads (see paragraph
2.5.1). The program of the internal test mode is necessarily different so
that it will check out the F-2 (flts 3, 4) data handler. The four test phases
of the internal test mode are:

a.   Video signals of unequal PRF are fed directly to the data handler.

b.   A long pulse is fed to the inhibit channel at an amplitude 9 db below
     the corresponding signal fed to the signal channel.

c.   I-F signals with unequal PRF are fed to the inhibit channel at an
     amplitude 9 db below the corresponding signal fed to the signal
     channel.

d.   I-F signals of equal amplitude are fed to both signal and inhibit
     channels.

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3.5.2 On-Off Control and Internal Programming

The F-2 (flts 3, 4) payloads are placed in the various operating modes by means of SPC's or RTC's. RTC's are used when the satellite is within range of a TAS. At other times, SPC's with proper time indexing perform the turn-off and turn-on operation.

3.5.2.1 Stored Program Commands. A list of SPC's required for this payload is shown in Table 3-6. Six commands are required. These commands are sets of relay contacts that activate various portions of the equipment during operation.

Table 3-6
PROPOSED STORED PROGRAM COMMANDS FOR
F-2 (FLTS 3, 4) PAYLOADS

SPC Number	Function
1	Activate band 1
3	Activate band 3b
4	Activate band 3c
6	Digital tape transport forward
7	Ready receivers
8	Receive cycle on

3.5.2.2 Real-Time Commands. A list of RTC's and their functions required for this payload is shown in Table 3-7; thirteen commands are required. These commands are set by relay contacts that also activate portions of the ferret equipment when the satellite is within range of TAS.

3.5.3 Test Signal Generator for F-2 (Flts 3, 4) Payload

The internal testing of the ferret equipment is accomplished in four modes with three RTC's. RTC-9 supplies ±12 v to the circuit and is on during all

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Table 3-7

PROPOSED REAL TIME COMMANDS FOR F-2 (FLTS 3, 4) PAYLOADS

RTC Number	Function
1	Readout
2	Motor drive forward
3	Motor drive reverse
4	Preamplifier select
5	Gain adjust
6	Ready receivers
7	Receive cycle on
8	Spare
9	Test generator on
10	Test generator control a
11	Test generator control b
12	Spare
13	Activate all bands

four modes of operation. RTC-10 and RTC-11 are used to activate various relays. A block diagram of the test signal generator is shown in Figure 3-24.

Mode 1 is initiated by RTC-9 and RTC-10. Unequally spaced 10-μsec video pulses are sent to the data handler. This is accomplished by triggering both a 10-μsec and a 640-μsec monostable multivibrator. The 10-μsec pulse is fed directly to the data handler. The trailing edge of the 640-μsec pulse triggers the 10-μsec monostable multivibrator, thus sensing a 10-μsec pulse to the data handler 640 μsec later. This is repeated at a 400-cps rate. Besides testing the data handler, these pulses also generate the nonuniform PRF signal, thus providing a test for that alarm.

Mode 2 is initiated by RTC-11 and RTC-9. During this test only the 640-μsec monostable multivibrator is triggered. The pulse is modulated by the 60-Mc oscillator and fed to the signal and inhibit channels of the receivers. Aside from testing the receivers, the amplitude comparator, and data handler, this mode tests the long-pulse alarm. RTC-9 initiates mode 3. The same wave shape as used in mode 1 is generated, except that in mode 3, it modulates the 60-Mc test oscillator and is sent into the receiver I-F strips.
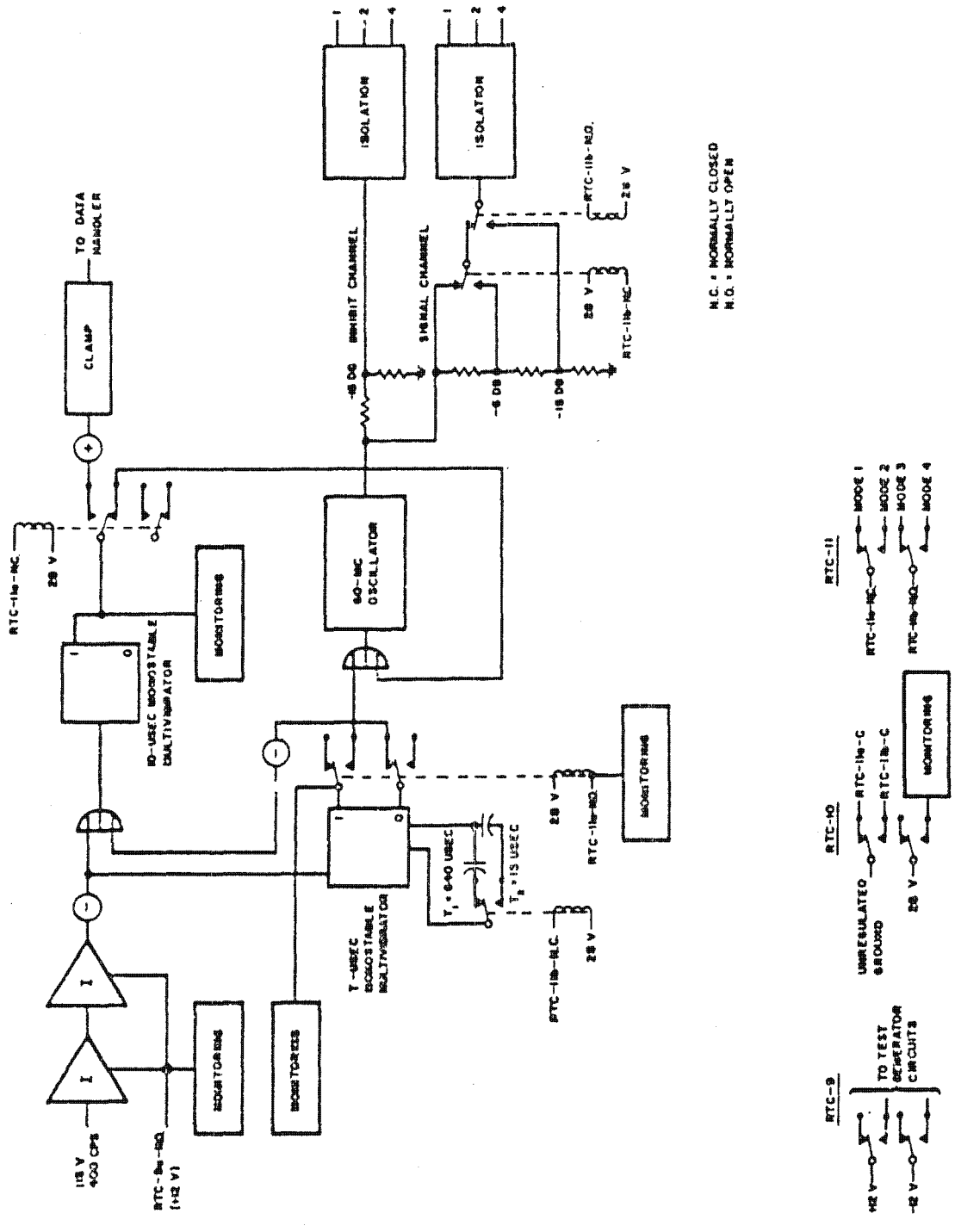
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Figure 3-24 Functional Block Diagram of F-2 (Flts 3, 4) Test Signal Generator

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Mode 4 is similar to mode 3, except the relative attenuation will be such that the signal should not pass through the amplitude comparator. This mode is accomplished by the use of RTC-9, RTC-10, and RTC-11.

3.5.4 Internal Programmer

The operation of the internal programmer (Figure 3-25) is the same as that for F-2 (flts 1, 2) payloads as described in paragraph 2.5.2.4.

3.5.5 Redundant Band Switching

Two methods of band switching are used in F-2 (flts 3, 4) payloads. In the primary method (Figure 3-26), the motors themselves via the encoders start and stop each other in rotation. The end of the scan of one band will start the scanning of the next. In the secondary (redundant) method, initiate pulses are generated by a 4-stage binary counter that is triggered by the 1-second satellite clock. The use of the 1-second clock for the redundant system requires that the time in each band be rounded off to the nearest second. The counters are updated once each cycle. This updating or reset comes from either the counter, the end-of-scan signal from the last band, or from the initial reset of the data handler. These inputs are OR gated, and trigger a monostable multivibrator that resets the counter.

The initiate signal normally comes from the end-of-scan signal of the previous band; however, this signal is OR gated with the initiate signal from the counter. The initiate signals from the counter always arrive after the initiate signals from the encoders, except when there has been a failure in one of the motors. In such cases the counter takes over for the band that is to begin scanning. Initiate pulses then start the band drive motor and apply power to the band. The end-of-scan signal of one band starts the next band and shuts off the power controller of the first band. The motor controller of the first band is turned off upon completion of one code wheel rotation (returning the motor to zero position). Stopping is aided by a solenoid-driven brake. If motor failure causes the repeat cycle timer to take over the initiate function for one or more bands, the total time required for a 4-band scan cycle is

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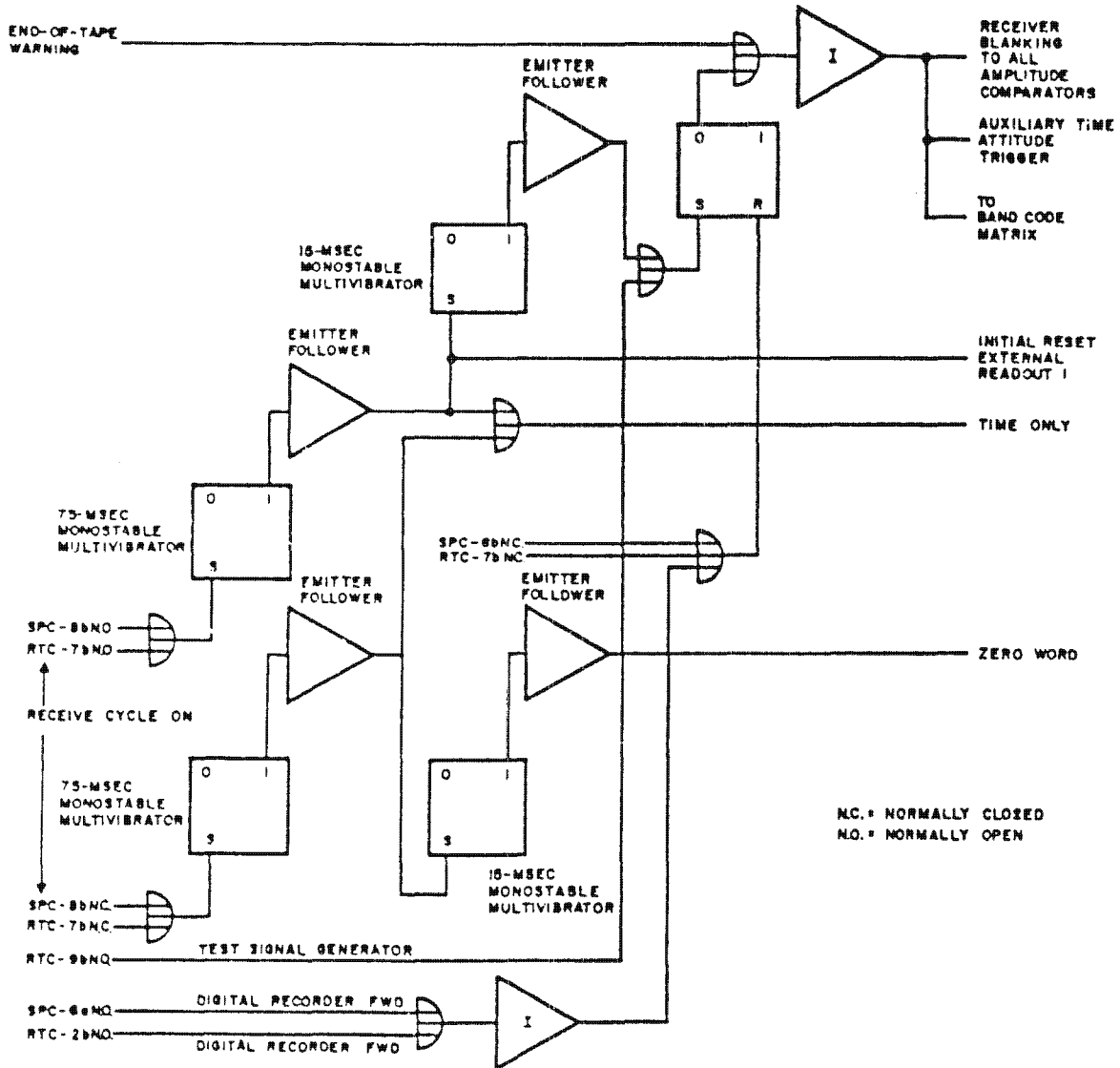
Figure 3-25 Block Diagram of Internal Programmer

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Volume I
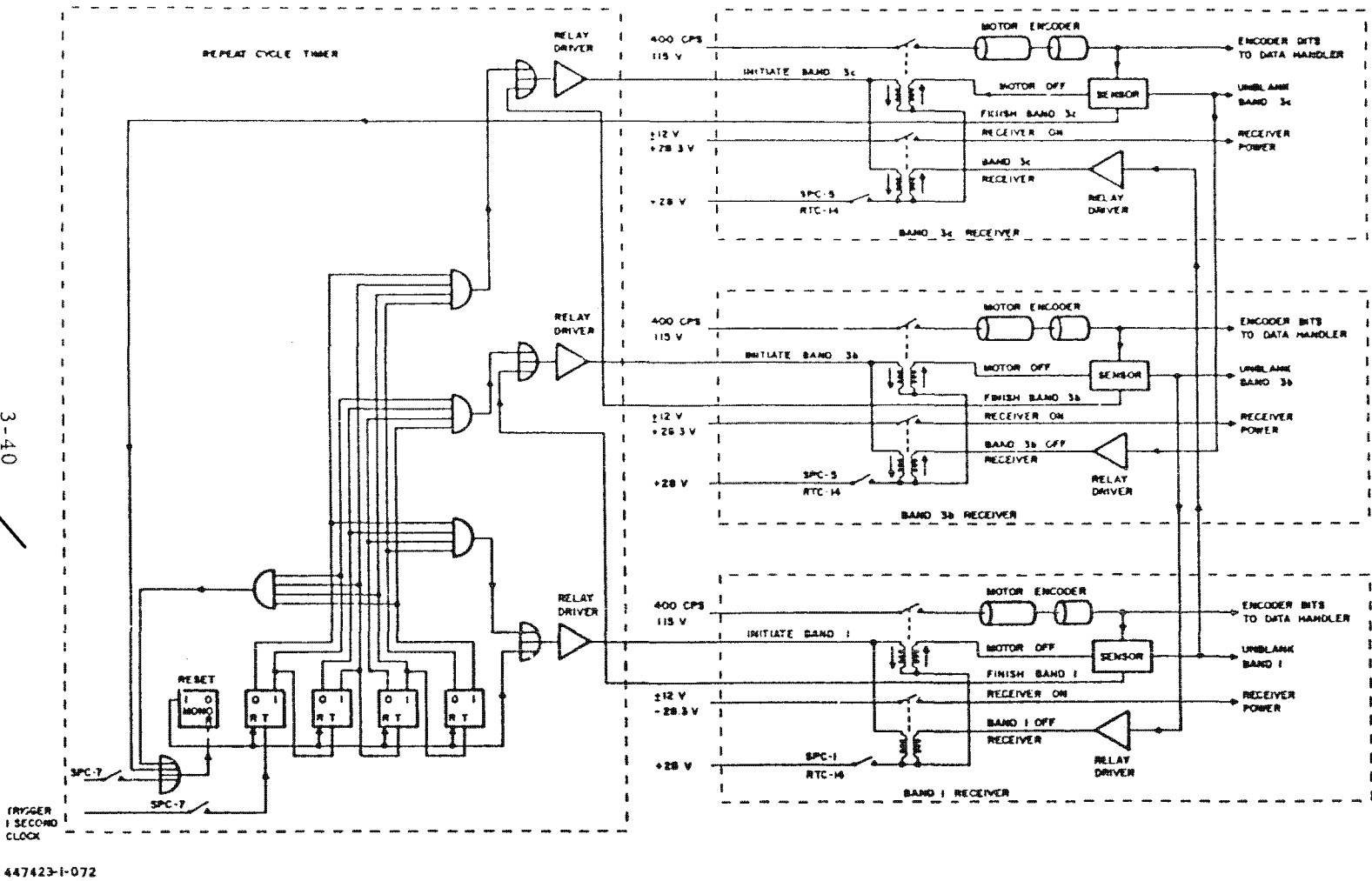
Figure 3-26 Block Diagram of Redundant Band Switching Unit

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somewhat increased, and the area of multiple intercepts and the transverse coverage are slightly reduced. Otherwise system capabilities are not affected.

3.5.6 Receiver Control Operation

This operation is for a typical receiver requiring a special power supply for the operation of a local oscillator. The initiate pulse from the SPC latches the power controller and motor controller. The power controller applies power to the local oscillators, I-F amplifiers, and amplitude comparator. The motor controller applies 400-cps power to the band scanning motor and disengages the brake from the motor shaft. The digitizer (shaft encoder) presents a continuous indication of the angular position of the motor shaft. The sensors send start and finish signals to the amplitude comparator unblanking circuit. The output of the amplitude comparator unblanking circuit is sent to the data handler to energize the proper verification circuit. The output of the amplitude comparator unblanking circuit is also sent to the band code matrix, through a transistor inverter.

The output of the digitizer is sent through a switching circuit that is activated by the amplitude comparator blanking circuit and the delay multivibrator. A 9-bit code is then sent to the data handler. In addition to the 9-bit code, which indicates a channel number, a band code matrix transmits a digital code to the data handler to indicate the receiver which is scanning. The code used is shown in Table 3-8.

3.5.7 Power Supplies

The power available from the auxiliary power supply does not fill all the needs of the ferret equipment. It is necessary, therefore, to provide low-voltage regulated power supplies for transistorized circuits, and a high voltage supply for vacuum tube local oscillators. The primary considerations in the design of these supplies are overall efficiency, minimum size and weight, and high reliability.

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Table 3-8

RECEIVER CONTROL CODE FOR F-2 (FLTS 3, 4) RECEIVERS

Band	Code
Receiver blanked by internal programmer	000
1	001
3b	011
3c	100
Between bands	111

The payload equipment will require the following voltages for proper operation.

   a.   115-v, 400-cps three-phase

   b.   115-v, 2-kc single-phase

   c.   +28.3 v regulated

   d.   -28.3 v regulated

   e.   +28 v unregulated

3.5.8 Attitude Converter

The digitization of attitude data is the same as for F-2 (flts 1, 2, see paragraph 2.5.4). Since the F-2 (flts 3, 4) payload uses a 68-bit word, the placement of the attitude data in the word is different.

The specifications for the attitude converter are as follows:

a.	Range of input level	-5 v to +5 v
b.	Digitization range (bits)	24 to 68 at 40 kc
c.	Accuracy	±0.25 v at 40 kc
d.	Sweep accuracy	±0.5 v

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3.5.9 Monitoring Control

The payload will provide, for transmission to the TAS via Subsystem C&C, various test data describing the operability of selected components of the ferret equipment.

The philosophy for selection of the monitoring points is a compromise between equipment complexity and monitoring sufficient to sense failures.

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SECTION 4

PAYLOAD CHECKOUT EQUIPMENT

4.1 GENERAL INFORMATION

The F-2 checkout equipment provides the means for easily evaluating the per-
formance of F-2 payload equipments as well as for calibrating and assisting
in their maintenance. The checkout equipment will be used for final inspec-
tion and acceptance tests of the F-2 payloads. After installation of the Sub-
system F payload equipment, the checkout equipment will be used for all tests
before system checkout. The operator of the checkout equipment will be able
to determine impending, as well as actual, failures by analyzing a permanent
recording of all measurements. For detailed examination of any particular
circuit in the payload, manual control is provided for both payload and check-
out equipments.

Subsystem F checkout is performed independently of all other subsystems
both before and after the Subsystem F payload is installed in the satellite.
The checkout equipment supplies all functions normally supplied to Subsystem
F by other subsystems. All cabling from Subsystem F to other subsystems
is connected to the checkout equipment for the tests.

The evaluation of the payload is performed through two sets of recorded
measurements called, respectively, static tests and dynamic tests.

The static tests consist of two groups. In group one, the checkout equipment
automatically monitors a large number of d-c or low-frequency a-c potentials
in the payload that are indicative of the performance of power supplies, mixer
crystals, digital circuits, and other like circuits. In group two, a pulsed
I-F signal generator located in the payload is activated, signals are fed to the
receivers, and selected d-c potentials are monitored. These potentials are
indicative of the performance of the preamplifiers and log I-F strips of the
receivers.

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For the d-c checkout voltages, go/no-go indications are provided. For voltages that vary as a function of time, such as crystal currents and band-switching signals, a pen recorder is used as the indicator. The go/no-go monitored voltages are recorded by the digital printer. Both records are available to the operator for analysis and for location of actual and impending failures.

During the dynamic test sequence, the checkout equipment automatically generates and injects radar-like R-F signals into the payload for a fixed number of test scans. The payload, when placed in the ferret mode of operation, processes these signals like an actual intercept. After the parameters (frequency, PW, pulse period, and time) of the signal are permanently stored on tape in the payload recorder, the data are read out into a data handler in the checkout equipment. The data (read out in a binary form) are converted to a decimal form, are appropriately scaled, and are then printed on a digital printer. An operator will therefore be able to evaluate the payload performance by a comparison of the printed data and the known input data. If desired, the automatic test can be followed by manual operation of the equipment for the purpose of localizing any fault to below-the-component level.

The four-cabinet assembly that comprises the checkout equipment is shown in Figure 4-1. The major units of this equipment and their general test functions are as follows:

Unit Name	General Use
Master Control	All Tests
Monitor 1	Static Test
Monitor 2	Static Test
Dual Pen Recorder	Static Tests
Digital Voltmeter	Static Tests
Dynamic Test-Control Unit (DTCU)	Dynamic Test Programmer
Signal Source Band 1	Dynamic Test
Modulator Band 1	Dynamic Test

4-2
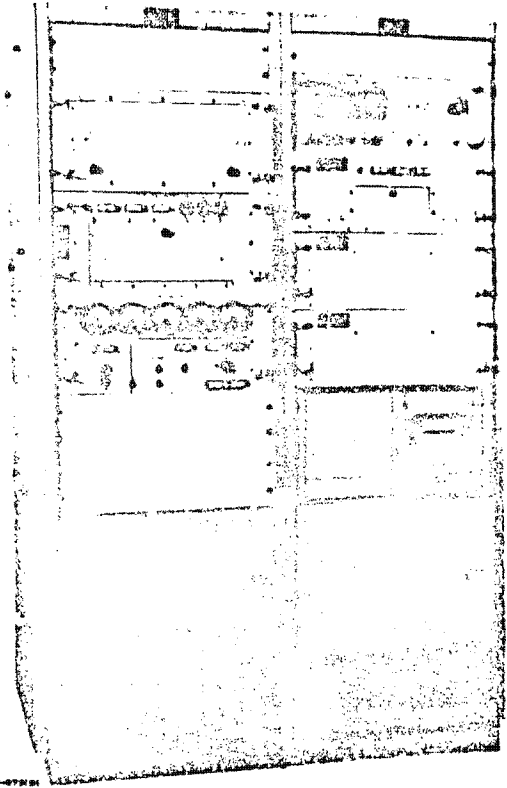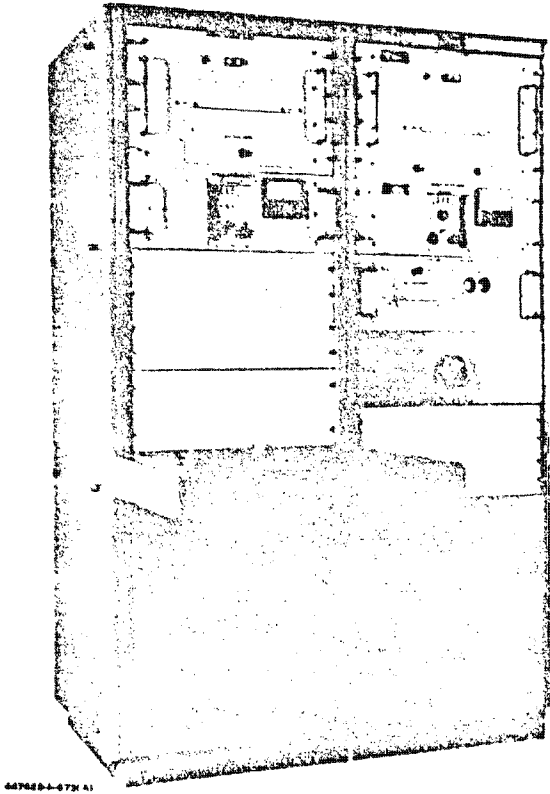
Figure 4-1 F2 Checkout Equipment

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Unit Name	General Use
Signal Source Band 2	Dynamic Test
Modulator Band 2	Dynamic Test
Data Handler 1, 2, 3	Dynamic Test
Programmable Power Supply	Dynamic Test
Signal Source and Modulators Bands 3b, 3c	Dynamic Test
Antenna Adapters	Dynamic Test
Manual Test Unit	Manual Test
Command Indicator Panel	Manual Test
Junction Box	Static and Dynamic Test
Digital Recorder	Static and Dynamic Test
Test Box and Dummy Load Unit (TBDLU)	Checkout Console Test

A block diagram of the F-2 checkout equipment is shown in Figure 4-2.

4.2 DESCRIPTION OF BLOCK DIAGRAM

By means of the TEST SELECTOR switch on the master control unit, the operator selects either STATIC or DYNAMIC and then presses the START TEST button to start the selected automatic test.

During the static test program the payload is commanded, through a programmed combination of RTC's or SPC's, into its TEST mode of operation. The band switching signals fed back from the payload through monitor 1 during the turn-on sequence automatically set the checkout equipment for operation with the particular group of bands present in the payload under test.

The monitored payload voltages are analyzed in the monitor unit and recorded by either the digital printer or pen recorder. The printed format (Figure 4-3) contains a set of designated test numbers that are indicative of various voltages measured and of no-go indications. Out-of-tolerance voltages (red NO-GO) that might damage the payload equipment or affect other measurements stop the static test and remove all power. No-go indications (amber NO-GO)
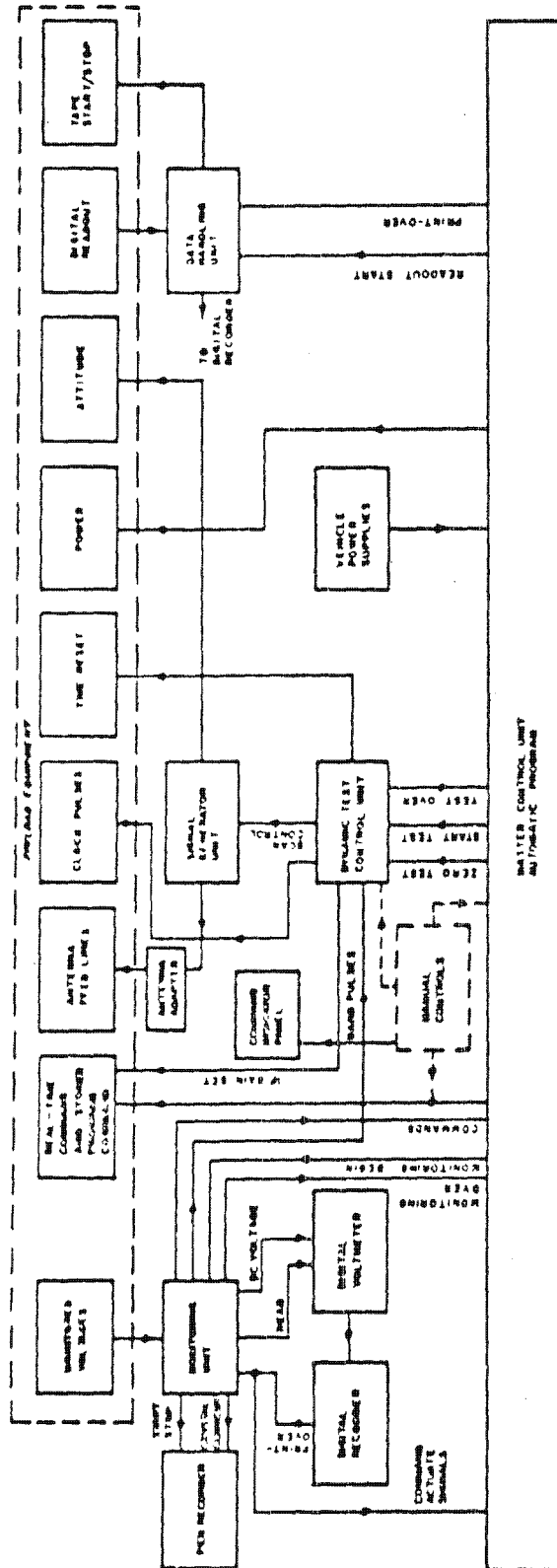
4-4

Figure 4-2   Block Diagram of F-2 Checkout Equipment

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PRINT WHEELS

```
  1  2  3   4   5  6  7   8  9  10  11
  |  |  |   |   |  |  |   |  |  |   |

  TEST NO.      VOLTS
  0  0  1   -   5  0  0   -  -  -   -
  {_____}      {____}

        -           -  -  -  -

  {_____}      {____}
  1  5  0   -   2  8  0   -  -  -   -
```
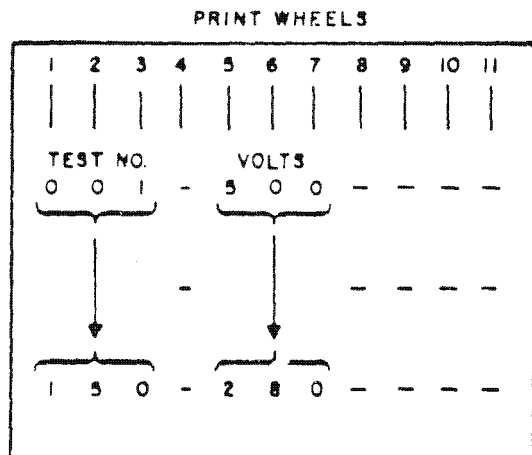
DASHED LINES INDICATE NO-GO

A. MONITORING FORMAT

```
  -  -  -  1      5  0  0  0    NUMBER OF BITS PER WORD
  -  -  -  2      7  1  2  5    TIME IN SECONDS
  -  -  -  3      2  5  0  0    PULSE REPETITION PERIOD 2 IN MILLISECONDS
  -  -  -  4      0  5  0  0    PULSE WIDTH IN MICROSECONDS
  -  -  -  5      2  5  0  0    PULSE REPETITION PERIOD I IN MILLISECONDS
  -  -  -  6      0  0  0  1    BAND NUMBER
  -  -  -  7      0  3  2  5    CHANNEL NUMBER

  -  -  -  1      4  9  0  0
  -  -  -  2      7  1  3  0          DASHED LINES INDICATE
  -  -  -  3      2  5  0  0          NON-PARITY CHECK
  -  -  -  4      0  5  0  0
```

CORRESPONDING PARTS   DATA
OF WORD INDICATOR

B. DATA FORMAT

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Figure 4-3 Digital Record Print Format for F-2 Checkout

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in any of the non-critical check points will not stop the test program. A single NO-GO indicator shows out-of-tolerance conditions for all amber NO-GO points. The point or points that show NO-GO are located by looking at the printed record.

After completion of the static test, a signal from the monitor unit through the master control unit turns off the payload equipment.

During the dynamic test program the payload is commanded into the RECEIVE mode of operation. After the warmup period, a signal to DTCU from the master control unit will permit the dynamic test to proceed. This will occur after the first complete band gate of a chosen sequence is received from a circuit located in the monitoring unit. The order of injection of signals into the payload is programmed to permit a definite order of processed output data for ease of operation analysis. During the warmup period, the DTCU also sets all preamplifiers in the payload to a preset gain. The DTCU controls all modulator units of the signal generator in the course of the dynamic test and commands the modulator units to change the modulation characteristics each time the control-band pulse is received. The modulation is changed for each of the 20 scans comprising this portion of the test. The simulated satellite clock pulses are also injected during this test, so that the time recorded for the first and succeeding intercepts is known. After the 20 scans, the ferret receivers are de-energized through the master control unit on a signal from the DTCU, and the payload is automatically commanded to read out on the printed record (Figure 4-3), seven numbers, corresponding to parts of the binary word and the number of bits in the word, are sequentially printed. Each print wheel has twelve positions: numerals 0 to 9, a blank, and a dash line. Dash lines in the columns used for the static test indicate no-go for the test voltages. Dash lines in the columns used for the intercept word indicate a non-parity check.

When all information is read out, the master control unit will be activated by a feedback payload signal to de-energize all power to the payload.

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Upon completion of the semiautomatic portion of the test, the recorded data of the dynamic test may be analyzed for determining the status of operation of payload functions. Should any questions exist as to the operation of any particular portion of the payload, the manually operated commands, in conjunction with the manual control of the checkout equipment, can be used for diagnostic purposes. In this mode of operation, the checkout equipment, in conjunction with external test equipment, will assist in locating faults in any component of the payload. The manual mode of operation may be used for additional application of the checkout equipment in fault location, maintenance, and adjustment of various payload functions.

4.3 MASTER CONTROL UNIT

The master control unit contains the payload power-distribution circuits, controls the test programs, and supplies the commands normally supplied via Subsystem C&C. All interconnections between units of the checkout equipment are made through the master control unit, except where physical limitations and circuit considerations dictate otherwise. A block diagram of the master control unit is shown in Figure 4-4.

4.3.1 Power Distribution

The primary power required to operate the checkout equipment is 2 kilowatts at 115 v ac, 60 cps, single phase. The checkout equipment supplies the following voltages to the payload:

> +28 v, unregulated
> $\pm$28.3 v, regulated
> 115 v, 400 cps, three phase
> 115 v, 2 kc, single phase

All power for the payload is applied through protective relay K1 of the master control unit (Figure 4-4). If any of the payload power supply voltages are out of tolerance, limit meters M1, M2, M3, M4, and M5 cause relay K2 to latch and prevent K1 from closing.

4-8
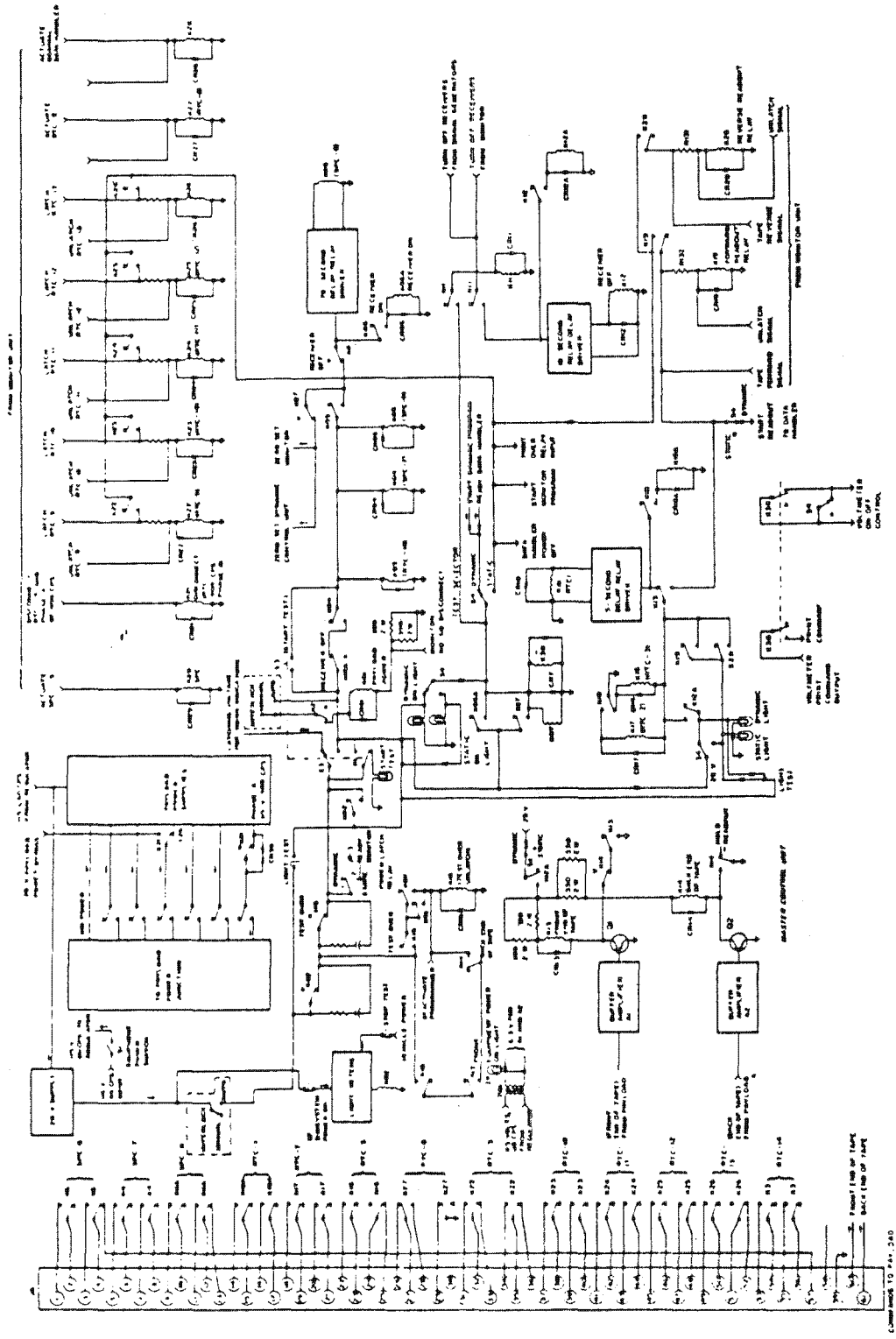
Figure 4-4 Block Diagram of Master Control Unit

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Relay K2 also latches when the main power is turned on, so that before K1 can be closed by closing the START TEST pushbutton switch, it is necessary to unlatch K2 by pressing the SUBSYSTEM POWER pushbutton switch. If any critical voltages fall out of limits in the static test program, K2 latches, thereby interrupting both the static test sequence and the payload power supply.

An interlock system prevents damage to the equipment due to accidental opera-tion of any of the manual switches during automatic operation and ensures that the automatic testing cannot be initiated when any of the manual switches are in use. When no manual command is activated, the interlock relay is ener-gized and the power circuit to the master control unit for the automatic test mode of operation is closed.

4.3.2   Test Selection

Selection of either the static or dynamic test program is made by setting the TEST SELECTOR switch (S4) in the DYNAMIC or STATIC position before pressing the START TEST button (S3). This selects the units in the checkout console to be activated during the test. Several internal changes in circuit logic are also accomplished through S4.

4.3.3   Simulated Commands

The master control unit contains relays that simulate the SPC's and RTC's, that are normally supplied to the payload by Subsystem C&C. These relays are interlocked to prevent improper sequencing of commands. Upon initia-tion of a static or dynamic test, the payload is activated in the desired mode of operation. A signal initiates either the monitor unit for the static tests or the signal generators for the dynamic test. During the course of either test there is a flow of signals from various units in the checkout equipment to the master control unit, which switches in appropriate payload commands. The various checkout units also send completion signals to the master control unit which switches both payload and checkout equipments to the next phase of the test.

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4.3.4 Description of Master Control Unit During Dynamic Test

Closure of S3 (START TEST button) latches K1, which applies power to the payload. K3, K4, and K5 are also activated, placing the receivers in the READY mode (RTC-14, SPC-6, and SPC-7). A signal is also generated to set the DTCU to the zero scan position. After a 70-second delay, K6 closes, activating the RECEIVER cycle (SPC-8) and latches K7 and K30. Signals sent through K7 to the DTCU permit the band gates fed back from the payload to control the generation of R-F signals and to remove the ZERO scan signal. A READY signal is also sent through K7 to the data handler, which disconnects calibration circuits and switches the payload digital output to the data handler input. Relay K30 turns off the digital voltmeter. Because the same digital recorder is used for both the static and dynamic tests, and the output of the digital voltmeter is permanently connected to the input of the recorder, it is necessary to disable the voltmeter. The band gates now step the R-F program through the appropriate test scans in the DTCU. Upon completion of the 20 R-F scans, a signal from the DTCU latches K11, which opens K6 and turns off the RECEIVE cycle (SPC-8 and RTC-14). K11 also activates a 10-second delay circuit, which energizes K12, removing SPC-6 and SPC-7, and completing the turnoff cycle.

With the TEST SELECTOR in the DYNAMIC position, closure of K12 performs two other functions. First, it applies power to the front end and back end of tape drivers Q1 and Q2, which activate K13 and K14 (front end and back end of tape relays) by signals from the payload. Second, it activates K16 (RTC-3 tape motor reverse) and after a five-second delay, it activates K18 (RTC-1 readout).

The payload is now in the NORMAL READOUT mode of operation. The tape runs to the front end, at which time the relay K13 closes and is latched. K13 removes RTC-1 (readout) and activates K19 (forward readout delay), which activates K17, RTC-2 (motor drive forward). The tape motor is now running in the forward direction with the capstan deactivated. K13 also sends a signal to the data handler unit; this starts the data processing cycle. During the

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processing, the capstan START and STOP signals are under the control of the checkout data handler.

After the last word on the tape is processed, the capstan START signal causes the tape to run to the back end, enabling the tape-end signal to latch K14 (back end of tape relay). Since the tape may come completely filled with a test word, the processing of the data will continue through the entire tape. The time of processing could last 2.5 hours with the same information being processed after the dynamic test information has been processed. To prevent excess time of processing, a timer in the data handler unit will hold the capstan start signal in after one-half hour of processing, again causing the tape to run to the end enabling the tape-end signal to latch K14. K13 is consequently unlatched and the payload again put into the first readout mode of operation (RTC-1 and RTC-3, activating K18 and K16). The tape runs to the front end, at which time K13 closes. Because K18 is closed, contacts of K13 in series with K14 energize K15, which is the TEST OVER relay. This relay is latched through its own contacts in series with K7 contacts (static and dynamic test power latch). This ensures the opening of K7 before K15 is de-energized, thus preventing a flip-flop action in the turnoff circuit. Power is removed from all previously self-latched relays, and K1 is de-energized, removing payload power.

4.3.5 Description of Master Control Unit During Static Test

When the START TEST switch (S3) is closed, with the TEST SELECTOR switch (S4) in the STATIC position, K1 latches and applies power to the payload. When K1 is activated, K3, K4, and K5 are also activated, placing the receivers in the READY mode (RTC-14, SPC-6, and SPC-7). After a 70-second delay, K6 closes, activating the RECEIVE cycle (SPC-8), and latches K7 and K30. Signals sent through K7 permit activation of K13 which switches the voltmeter and printer into the static test mode of operation. The voltmeter sampling circuit is connected externally to the monitor unit and the print command loop is closed.

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Closing S7 activates the monitor unit. During the progress of the static test, signals from the monitor unit latch and unlatch combinations of K21 through K26 (400-cps power on-off, RTC-9 through RTC-13) and activate K27 through K29 (RTC-8, RTC-15, SPC-1 through SPC-5). These switch the payload equipment to the mode of operation necessary for the particular test in progress. K21 stops the band motors by removing the 400-cps power and momentarily activating the motor brake by interrupting 28-volt power to the satellite. This procedure stops time-varying voltages and simplifies testing.

A signal from the monitor at the appropriate time activates K11 (SPC-8, off) to turn off the receivers. K12 closes through K11, completing the turnoff procedure. It is necessary to activate K19 and K20 from the monitor for forward or reverse readout. With S4 (TEST SELECTOR) in the static position, S4 also disconnects K13 and K14 (start of tape and tape end relays).

When K20 is activated by the monitor, for an activity test, K16 and K18 are activated, and the tape runs toward the front end. K19 is subsequently activated and switches to the second readout mode (RTC-1 and RTC-2 activated).

At the completion of the monitor test, a signal from the monitor actuates K15, unlatching all relays and turning off all power through K1.

4.4 MONITOR UNIT

4.4.1 General Description

The monitor unit has seven basic functions:

   a.   Provides the means for monitoring and recording the payload telemetered d-c and time-varying voltages

   b.   Incorporates a voltage comparator that makes comparisons of the monitored voltages on a go/no-go basis

   c.   Enables complete testing of all payload functions to determine the correctness of payload performance in all modes of operation

   d.   Determines from payload signals which bands are in operation and then automatically switches on the appropriate functions in the checkout equipment

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e.   Supplies signals for activation of payload commands through the
master control unit (dependent on the particular test in progress)

f.   Stops automatic test sequence when critical voltages are out of
tolerance.

g.   Provides a manual calibration mode of operation in which tests of
checkout equipment power supplies, reference voltages, and test
points from both payload and checkout equipment can be performed

A schematic diagram of the F-2 monitor unit is shown in Figure 4-5.   The
monitor unit is divided into two main subassemblies, monitor 1 and monitor
2.   Monitor 1 contains all calibration switches; one stepping relay switch; all
relays necessary to the performance of a test; and the voltage comparator.
Monitor 2 consists of eight stepping relays and about 200 potentiometers
which are used to set limit voltages for the comparison go/no-go tests.

A digital voltmeter, printer, and pen recorder are also used in the monitor-
ing system.

4.4.2 Stepping Relay Functions

Since the number of monitored voltages is approximately 220, nine stepping
switches are employed to form a 225-position, 12-pole switch.   Bank A of
each switch is used to sequence between switches.   Banks C, D, and E are
connected in a matrix, which denotes position of the switch in decimal form
by means of 10-wire-per-digit output.   The decimal position is displayed on
a visual readout and is printed by the digital recorder during test.

Banks K and M switch the voltages from the limit potentiometers to the com-
parator.   The test voltage is switched in by Bank L.   Banks F, G, H, and J
are used to activate switching functions necessary during the course of a
test.   This includes activation of combinations of payload commands through
the master control unit, and changes in internal programming necessary dur-
ing a test.

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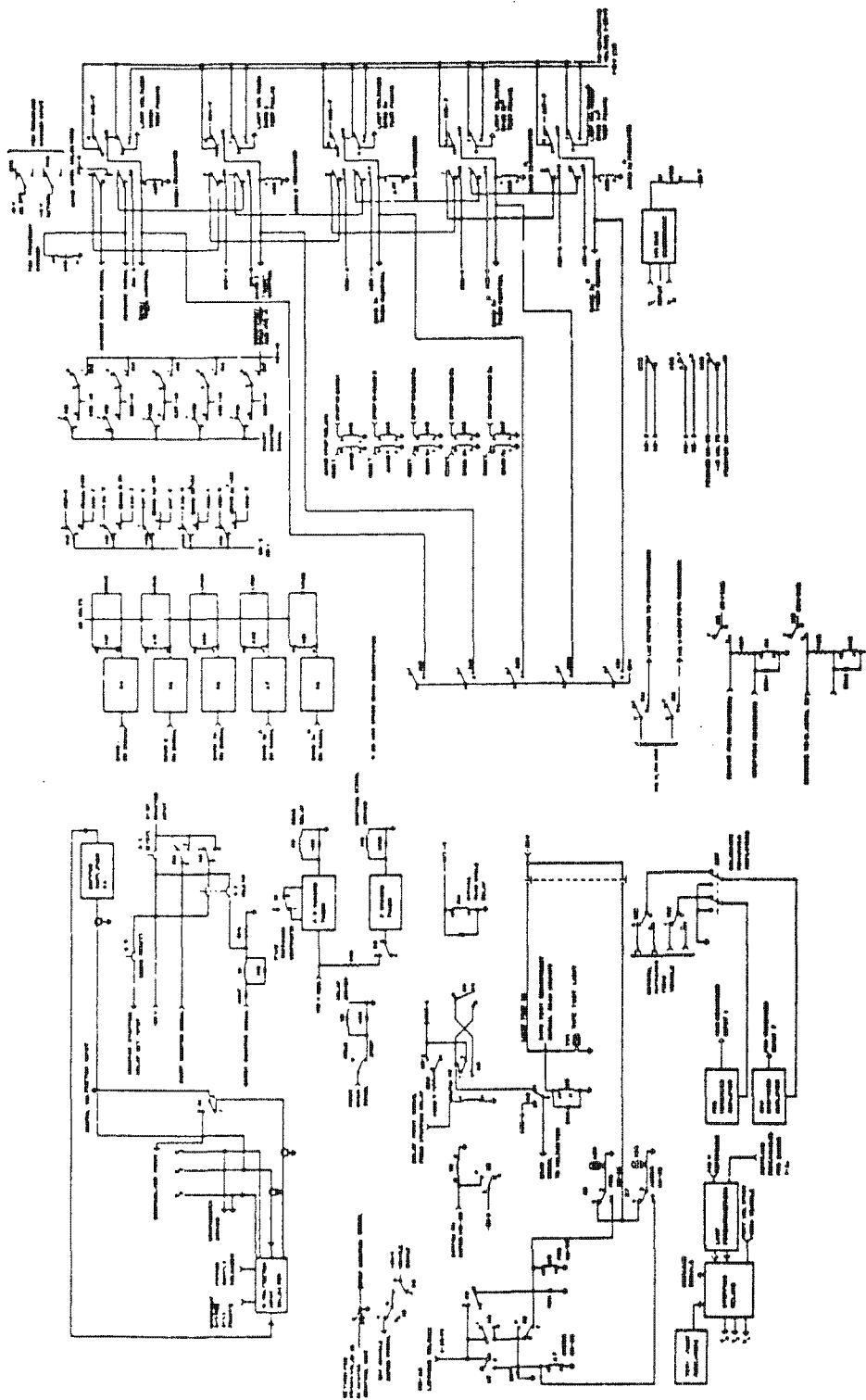
Figure 4-5   Schematic Diagram of F-2 Monitor Unit

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4.4.3 Presentation of Static Test Data

The test voltages from the payload are converted to 10-wire-per-digit decimal code by the digital voltmeter for presentation by the digital recorder. In addition to printing the test voltages, the number of the test is printed. A dash line is printed to denote any voltage that is outside of preset limits.

The dual-channel pen recorder is used to record receiver crystal currents. One channel monitors signal crystal currents, and the other monitors inhibit crystal currents. Since two separate crystal currents are monitored in each band, a signal from Bank H of the stepping switches from signal-and-inhibit A to signal-and-inhibit B through K12 after several sweeps have been recorded. Dual marker pens indicate the bands and crystal currents being monitored.

4.4.4 Voltage Comparator

The voltage comparator is used to determine whether a monitored voltage is within preset limits. The comparator amplifier is a dual-channel system fed by 60-cps square-wave voltages which are generated through the operating circuit of relay K32. One channel is used to provide ranges between the high limit and the monitored voltage and the other channel is used to provide ranges between the low limit and the monitored voltage. The 60-cps square waves are amplified and mixed, and the resultant voltage is applied to the contacts of the go/no-go relay (K33).

The first set of contacts of relay K33 is used to apply a ground to energize the blank print wheel or the dash print wheel on the digital recorder. A blank denotes GO and a dash denotes NO-GO.

In the case of a within-limits voltage (go), the two square waves are in phase, and K33 is energized. The first set of contacts thereof energizes the blank printing wheel, and the recorder prints a blank which indicates GO. The second set of contacts on K33 breaks the -28 v signal to K8, which disables the red and amber no-go lights. The third set of contacts on K33 is used to

monitor the TAPE END signal. In monitoring positions 220 and 221 a stepping switch energizes K5 which in turn interrupts the readout pulses and transfers them to the comparator switching contacts of the relay and, accordingly, no printing results during tape transit.

At either end of the tape, the go pulse from the tape, via the comparator, causes the monitoring to begin again in the normal sequencing procedure.

In case of an out-of-limits voltage, the two square waves are out of phase and a dash is printed on the recorder through the corresponding first set of K33 contacts. The corresponding second set of contacts puts a -28 v signal through the no-go actuator to the red-amber NO-GO selector. If the out-of-limits voltage is a critical voltage, the red light will go on indicating a NO-GO, K6 latches, and a signal is sent to the master control unit to disconnect all payload power. For a non-critical no-go condition, where continuation of the testing is desired, a BY-PASS NO-GO signal is fed to K2, removing the red NO-GO and the STOP MONITOR signal. The third set of K33 contacts is now open and the normal readout pulses appear at the voltmeter external read input.

4.4.5 Check of Payload Commands

The command switching for the static test program is shown in Table 4-1. During the progress of the static tests, it is necessary to activate particular combinations of RTC's and SPC's prior to actual test procedure. For example, the payload I-F test generator must be activated to check the I-F amplifiers.

Signals are sent from the stepping relay to the master control unit to excite the appropriate control circuits which activate the payload command relays. The telemetered point from the payload corresponding to each command is monitored after each command is activated. Go indications for the telemetered points effectively check the operation of all payload command functions with the exception of the gain adjustments and the readout controls.

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Table 4-1

STATIC TEST PROGRAM FOR F-2 CHECKOUT

Test Number	Payload Test Points	Commands or Switching Activated by Programmer Prior to Test Performance	Remarks
0		Latch RTC-14, SPC-6, SPC-7, and SPC-8. Step monitor stepping switch to zero position and activate monitor. Unlatch all latching relays in monitor.	Commands and zero set are actuated in control and programmer unit. This places receivers in the normal ferret mode of operation and initiates the static test.
	1, 3, 5, 9	Connect Signal A and Inhibit A crystal currents and Band ON markers to pen recorder	One crystal from each balanced mixer is monitored on a single wire designated "A" - the other as "B." "A" is continuously monitored for the first half of the static test. "B" is monitored after test "A."
1-8	122-127, 119-120		For tests numbered 1-24 sequencing will stop at a no-go, necessitating repair of faults before proceeding.
9	SPC-1A arm		
10, 11	60, 61		

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Table 4-1 (contd)

Test Number	Payload Test Points	Commands or Switching Activated by Programmer Prior to Test Performance	Remarks
12-21	133-135, 128-132		Test checks parallel connection of RTC and SPC and isolation diodes between SPC-1 to SPC-5 and RTC-14. For points 133-135, RTC-6A is normally open. For points 128-132, RTC-7A is normally open.
22	SPC-2A arm		
23, 24	144, 116	Latch RTC-9	
25	SPC-3B arm	Connect stepping switch to sequence through remainder of points indicating but not stopping at a no-go	
26, 27	RTC-6 & RTC-7 arm		
28-47	20-39		Preamplifier gain set to normal position in gain control unit before the test is initiated
48-49	139-140	Stop receivers in band 1 disconnect Signal A and Inhibit A crystal currents from pen recorder	Each time receivers are stopped in a band, BAND ON pulse is used to disconnect RTC-14 and the 400-cps power from the band sweep motor. This enables static testing of the time-varying voltages.

Table 4-1 (contd)

Test Number	Payload Test Points	Commands or Switching Activated by Programmer Prior to Test Performance	Remarks
51-70	40, 67-48, 89		
71	SPC-5B arm	Actuate RTC-3	
72	143		Redundant relay in payload should be latched.
73-91	67-80, 89, 104, 82-84		
92	SPC-1A normally open	Latch RTC-10	Allows test of I-F gain
93	145		
94-98	61, 10, 15, 45, 55		
99	SPC-2A normally open		
100	SPC-3B normally open	Latch RTC-11	
101	146		
102, 103	SPC-4B normally open		
104	45		
105	Spare		
106	147	Latch RTC-12	
107	45		Tests 81 and 107. Check inhibit function, band 1.
108	50		

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Table 4-1 (contd)

Test Number	Payload Test Points	Commands or Switching Activated by Programmer Prior to Test Performance	Remarks
109	SPC-1B arm	Start receivers sweeping	
110	SPC-1B normally open	Stop receivers in band 2	
111	46		Tests 111 and 114. Check inhibit function, band 2.
112	51		
113	75		Tests gating multivibrator in data handler B, band 2
114	46	Unlatch RTC-12	
115	SPC-2B arm		
116	SPC-2A normally open	Unlatch RTC-11	
117	Spare		
118-121	41, 62, 65, 66	Unlatch RTC-8 at test point 121	
122	75		Tests gating multivibrator in data handler A, band 2
123-126	11, 16, 46, 56		
127	RTC-6A arm		
128, 129	RTC-6B arm, RTC-6B normally open	Start receivers sweeping	
130	RTC-7A arm	Stop receivers in band 3a	

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Table 4-1 (contd)

Test Number	Payload Test Points	Commands or Switching Activated by Programmer Prior to Test Performance	Remarks
131-135	42, 12, 17, 47, 57		
136	Spare		
137	75		Check gating multivibrator in data handler A, band 3a
138	Spare	Latch RTC-8	
139	75	Latch RTC-11	Check gating multivibrator in data handler B, band 3a
140	47		Check inhibit function of comparator, band 3a
141	Spare	Latch RTC-12	
142	47		
143	52		
144	RTC-7B normally open	Start receivers sweeping	
145	RTC-7B normally open	Stop receivers in band 3b	
146	48		Tests 146 and 149. Check inhibit function, band 3a.
147	53		
148	75		Checks gating multivibrator in data handler B, band 3b

Table 4-1 (contd)

Test Number	Payload Test Points	Commands or Switching Activated by Programmer Prior to Test Performance	Remarks
149	48	Unlatch RTC-8 and RTC-12	
150	75	Unlatch RTC-11	Checks gating multivibrator in data handler A, band 3b
151	43		
152	75		
153-156	13, 18, 4%, 58		
157	Spare		
158-159	Spares	Start receivers sweeping	
160	Spare	Stop receivers in band 3c	
161	44		
162	75	Checks gating multivibrator in data handler A, band 3c	
163-166	14, 19, 49, 59		
167	Spare		
168	Spare	Latch RTC-8	
169	75	Latch RTC-11	Checks gating multivibrator in data handler B, band 3c
170	49		Tests 170 and 172 check inhibit function, band 3c
171	Spare	Latch RTC-12	
172	49		

Table 4-1 (contd)

Test Number	Payload Test Points	Commands or Switching Activated by Programmer Prior to Test Performance	Remarks
173	54		
174	Spare	Unlatch RTC-8	
175	Spare	Unlatch RTC-12; start receivers sweeping.	
	2, 4, 5-9	Connect Signal B and Inhibit B crystal currents & BAND ON markers to pen recorder	
176-198	152-153 154-159 160-173	Unlatch RTC-11 Unlatch RTC-10 at 177	
199	174	Disconnect Signal B and Inhibit B crystal currents from pen recorder	
200	175		
201	148	Latch RTC-13	
202	80	Turn off receivers	
203	138	Latch RTC-3 & RTC-1	
204	80		
205	136		
207-209	85-88		
210	Spare		
211-214	85-88	Latch RTC-8	
215	80	Unlatch RTC-3 and -1	

Table 4-I (contd)

Test Number	Payload Test Points	Commands or Switching Activated by Programmer Prior to Test Performance	Remarks
216	Spare		
217	Spare		
218	137		
219	80	Unlatch RTC-8	
220	114	Disconnect normal print circuit; allow go at back end of tape to print.	
221	113	Unlatch RTC-2 and -1; allow go at front end of tape to print.	
222, 223	Spares	Reconnect print command	
224	RTC-14A normally open	Activate SPC-1 to SPC-5	Checks that diodes isolating RTC-14 from SPC-1 to SPC-5 are not shorted
225	Internal +4 volt reference	Deactivate programmer; test over.	

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The gain adjust controls are checked during the dynamic test. The telemetered points corresponding to gain positions are monitored and recorded.

The readout control circuits are monitored for correct operation during tests numbered 220 and 221 of the static test program.

4.4.6 Tape End Signals

A signal from the stepping switch to K5 (tape test relay) changes the monitor readout circuit to read on a signal through K33 in the go position. The voltage monitored is the tape front-end or back-end signal. Since the comparator will be in a no-go state until the tape reaches the end, contacts of K5 are used to prevent activation of the no-go relay.

4.4.7 Band Gates

The band gates generated in the payload are the inputs to d-c amplifiers A4 through A8. These pulses drive BAND ON relays K18, K19, K20, K30, and K31 through transistors Q1, Q2, Q3, Q4, and Q5. Contacts on the BAND ON relays are used (a) to generate markers for the pen recorder, (b) to generate signals for controlling the sequencing of the DTCU, (c) to generate band stop signals, and (d) for switching the checkout equipment for operation with different combinations of bands.

4.4.8 Monitoring of Time Varying Voltages

The payload receiver scan motors are stopped in each band to monitor all of the test voltages that are on only with the band in operation. A signal from the stepping relays latches one of the BAND STOP relays, K13 through K17. K3, the DELAY PRINT RELAY, is also activated each time any of the BAND STOP relays is activated. This interrupts the test cycle. Contacts of the BAND STOP relays K13 through K17 are connected in series with contacts of the BAND ON relays K18, K19, K20, K30, and K31. The signal through the end gate of the BAND STOP and BAND ON contacts is fed to the master control unit to stop the receivers in a band. The delayed print relay

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K4 is also activated by this signal. This relay now bypasses K3 to apply a timing pulse to continue sampling of monitor points. After all time-varying voltages in a band have been recorded, K3 and one of the BAND STOP relays is unlatched, returning the payload equipment to normal ferret operation.

4.4.9 Switching of Checkout Equipment

The checkout equipment is designed for five-band operation. Several switching operations must be performed, therefore, to accommodate the particular combination of receivers in the payload under test.

The BAND-ON signal pulses indicate the combination of active receiver bands in the payload at a particular time. The pulses latch the band indicator relays (K35 through K39) which perform the required switching for adapting the checkout equipment for operation with the particular combination of bands in the payload.

Two sets of contacts on each of the indicator relays switch the ADVANCE and ADVANCE ENABLE signals to the DTCU.

The ADVANCE signal is generated by the BAND-ON pulse from the first receiver band active in the payload at the particular time. The ADVANCE ENABLE signal is generated as a result of the absence of the same BAND-ON pulse. A signal from relays K35 through K39 is also supplied to the DTCU to switch the timing circuits.

4.4.10 Manual Calibration of Monitor Unit

Prior to activation of the automatic test, the digital voltmeter input is connected through contacts on relay K1 to the arm of switch S1, the VOLTMETER INPUT selector. This enables selection and measurement of a number of critical voltages in the checkout system. In addition, one position of S1 allows selection of all power supply voltages for monitoring through another switch on the power supply unit. S2 and S3 (Step), in conjunction with the Nixie indicators, permit manual sequencing of the stepping relays to any test position. When the Nixie readout indicates proximity to the test point desired, S3 may be used to advance the stepping relays, a test position at a time. When in a test position,

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checking of low and high limits may be made by switching in the voltmeter
through S1; adjustment of limits, if required, can then be accomplished with
limit potentiometers accessible through the front panel. Switch S5 enables
manual resetting of all stepping relays to the 0 test position.

After stepping to a position in the manual mode of operation, a check of the
sampling loop can be accomplished by closing switch S4 (MANUAL PRINT).
This switch removes data handler power by grounding the data handler power
relay and sends a signal to the digital voltmeter to read.

4.4.11 Monitor Unit Test Sequence

When the START TEST button on the master control unit is pressed, -28 v
power is momentarily applied to all stepping relays for initial reset to posi-
tion 1. The programmer sends an initiate signal (-28 v) which activates K1
in the monitor unit. The initiate signal is also applied to the stepping relay
command, thereby sequencing and unlatching various relay banks.

K1 switches the digital voltmeter to the appropriate switch bank for reading
the various telemetered voltages. K1 also sets the repetition rate of the ex-
ternal voltmeter read circuit to 3 seconds. This read circuit activates K9 at
3-second intervals which initiates the sampling circuit in the digital voltmeter.

Upon completion of the sampling cycle, the digital voltmeter sends a print
command pulse which is routed through the master control unit (K30) and the
data handler to the input of the print command delay circuit in the printer.
After a 0.2-second delay the print cycle is initiated by this circuit. During
the print cycle -28 v power is switched from contacts of K6, which are used
to stop the test in the event of a no-go, to the coil of K8. Closure of K8 en-
ables no-go sampling and initially sets the stepping signal driver circuit. In
the event of a red no-go, the static test is deactivated by switching -28 v to
the input of the red no-go test stop contacts of K6 at the end of the print cycle.
K8 is simultaneously de-energized allowing a pulse delayed by 0.2 second
from the stepping signal delay circuit to energize K10 which advances the
stepping relays to the following test position.

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The test is thus sequenced through all 225 positions as shown in Table 4-1.
After test 225, a deactivate signal from the last stepping relay is sent to the
master control unit. S8 (HOLD switch) enables the sequence to be interrupted
at any step by opening the input to K8. All of the above sequence still occurs
except that no-go sampling and automatic advance of the stepping relays is
stopped.

4.5 MANUAL TEST UNIT

The manual test unit establishes the means for achieving manual control of
payload functions during diagnostic test procedures. Switches on the manual
control unit simulate all payload commands, thus enabling the operator to ex-
amine any component in the payload for troubleshooting, maintenance, cali-
bration, and adjustment. The switches simulate the relays of the automatic
mode of operation and are interlocked to prevent activation during the auto-
matic mode of operation.

The use of this manual control system enables troubleshooting of any compo-
nent of the payload without removing it from the assembly. If either the static
or the dynamic test indicates a malfunction, detailed investigation of the fault
can be made through the manual test unit in conjunction with either the internal
or external test signals. For example, malfunction of the payload data handler
may be localized with the aid of an oscilloscope and the internal video genera-
tor. Similarly, malfunctions in the I-F amplifiers can be localized through
the use of an oscilloscope and the I-F test generator. The receiver scan mo-
tors can be stopped through switches on the manual test unit for testing of the
receiver front ends. The normal gain settings of the preamplifiers can also
be determined in this mode of operation.

Figure 4-6 shows the schematic diagram of the manual test unit. With the
exception of the payload power switches, all switches are of the double-throw
three-position type. Two poles are used to simulate relay contacts, while the
third pole of each switch is used for the interlock function. For stopping the
scan motors, the brake switch on the manual test unit interrupts one phase
of the three-phase, 400-cps supply to the payload. This switch also interrupts

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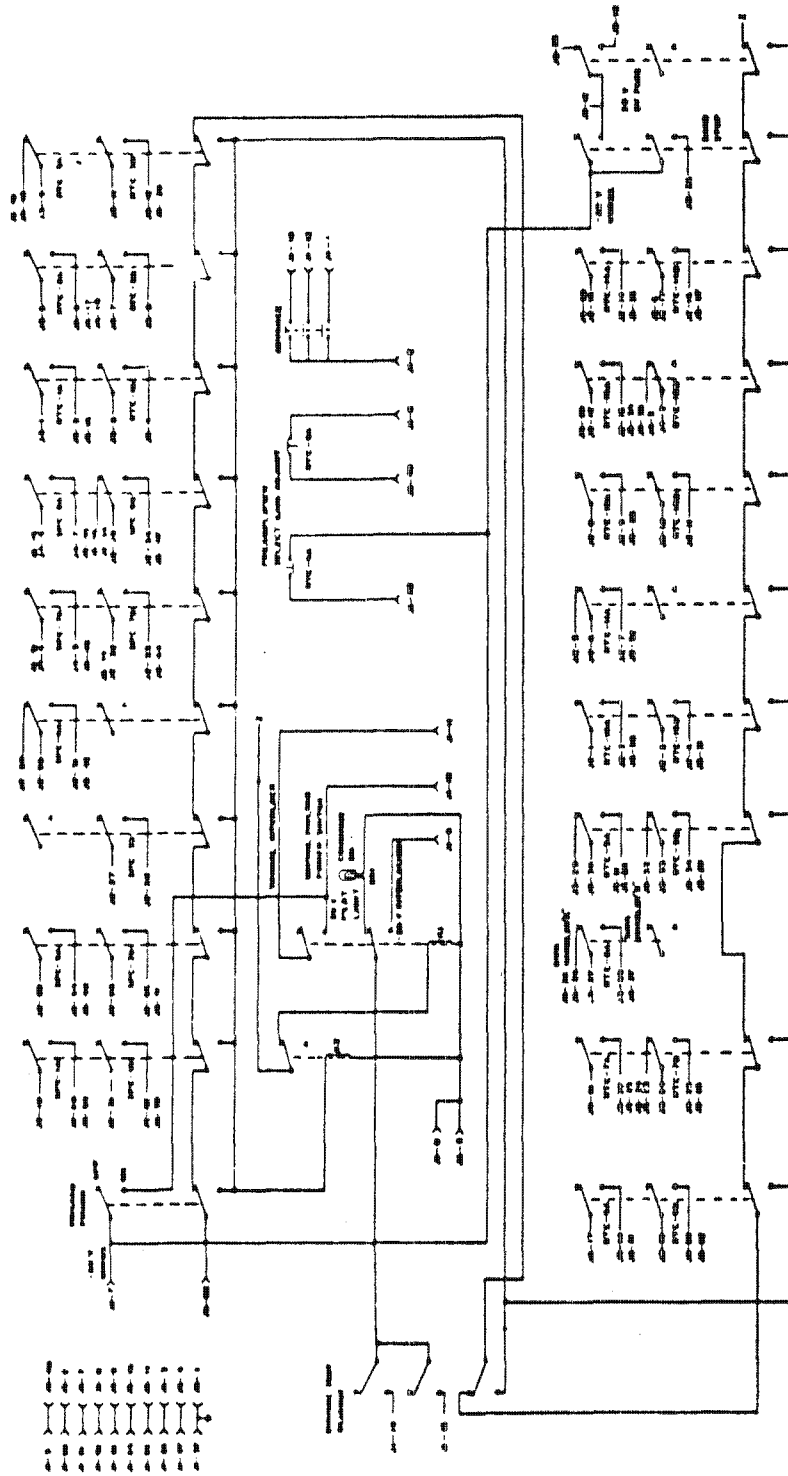
Figure 4-6 Schematic Diagram of Manual Test Unit

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the 28-v supply, thus causing the brake to take effect. A 28-v bypass switch enables restoration of the 28-v supply to the various units of the payload equipment without actuating the scan motors.

Manual advance of the DTCU is provided by a momentary switch located on the manual test unit. This enables the selection of the modulation characteristics of the signal source in manual operation for use in a diagnostic test.

RTC-4 (Preamp Select) has not been included as one of the commands on the manual test unit. This function has been incorporated in the band mode switch on the DTCU. When this switch is placed in any of the band positions, the signal preamplifier of that band is automatically selected for gain adjustment. A pushbutton on the manual test unit is provided to allow the preamplifier selected to be returned to the signal channel. Upon release of this button, the inhibit channel of the band selected is under control for gain adjustment. The payload telemetered voltages for RTC-4 and RTC-5 can be measured by the digital voltmeter through the voltmeter selector switch on the monitor I unit.

4.6 COMMAND INDICATOR PANEL

This panel, shown in Figure 4-7, is composed of indicators that display the status of payload commands during either manual or automatic checkout procedures. The purpose of this panel is to provide a means for locating interaction of payload commands. Where possible, indicators show OFF as well as ON positions of command relays and switches. Indicators are also provided to permit rapid determination of the preamplifier selected for control and its gain position. These indicators are controlled by payload telemetered voltages.

4.7 SIGNAL GENERATORS

The signal generators in the checkout equipment supply a specific prepared program of simulated radar signals that completely test and calibrate the payload. These programmed signals comprise the dynamic test and are defined with the following criteria.

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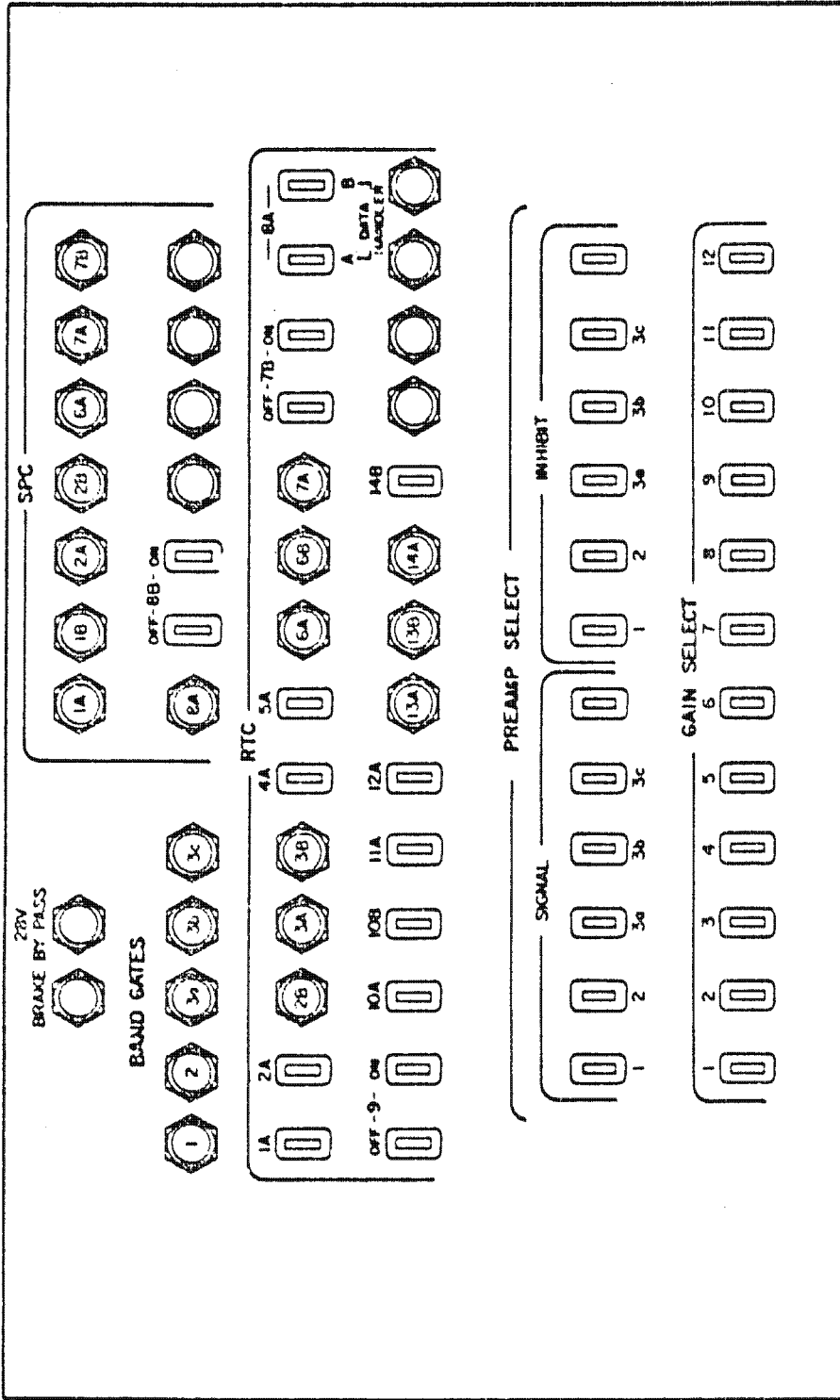
Figure 4-7 Command Indicator Panel

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a. Test signals are automatically selected for injection into the payload.

b. The test signals are selected to accurately determine performance and help locate faults in the payload.

c. The addition of other bands can be readily accommodated.

d. The accuracy of the test signal characteristics is at least an order of magnitude better than that specified for the payload.

e. The stability of the signal generators obviates frequent or repeated calibration.

The signal generators are capable of being programmed manually as well as automatically (as they are in the dynamic test mode). In the manual mode of operation the diagnostic tests for maintenance, reliability and detailed evaluation of the payload will be performed. The capability of manually controlling the payload with the manual test unit in conjunction with the manual functions of the generators lends the flexibility required for these tests. Tests not suitable for scheduling in the automatic test program are performed during the manual method of operation.

Figure 4-8 shows the functional block diagram of the signal generating equipment. The group consists of two signal source units (band 1 and band 2), two modulator units and the DTCU. All commands to the signal generator group are issued from the DTCU, via a modulator, to the signal sources and ultimately to the payload equipment.

4.8 DYNAMIC TEST CONTROL UNIT (DTCU)

The DTCU supplies:

a. Modulator units in the checkout equipment with control signals in the dynamic test and manual modes of operation

b. The payload with the command signals (RTC-5 Gain Adjust, RTC-4 Preamp Select, RTC-8 Standby Circuit Control)

c. Simulated time and attitude information for either the dynamic or manual mode of operation

d. Indication of the progress of the dynamic test

A schematic diagram of the DTCU is shown in Figure 4-9.

4-33
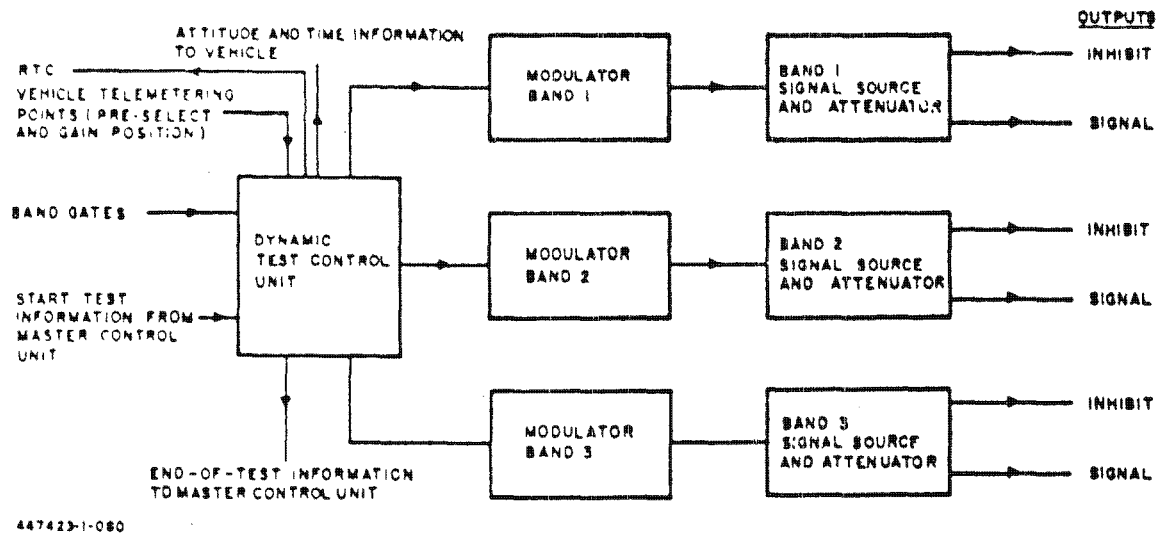
Figure 4-8   Functional Block Diagram of F-2 Signal Generators

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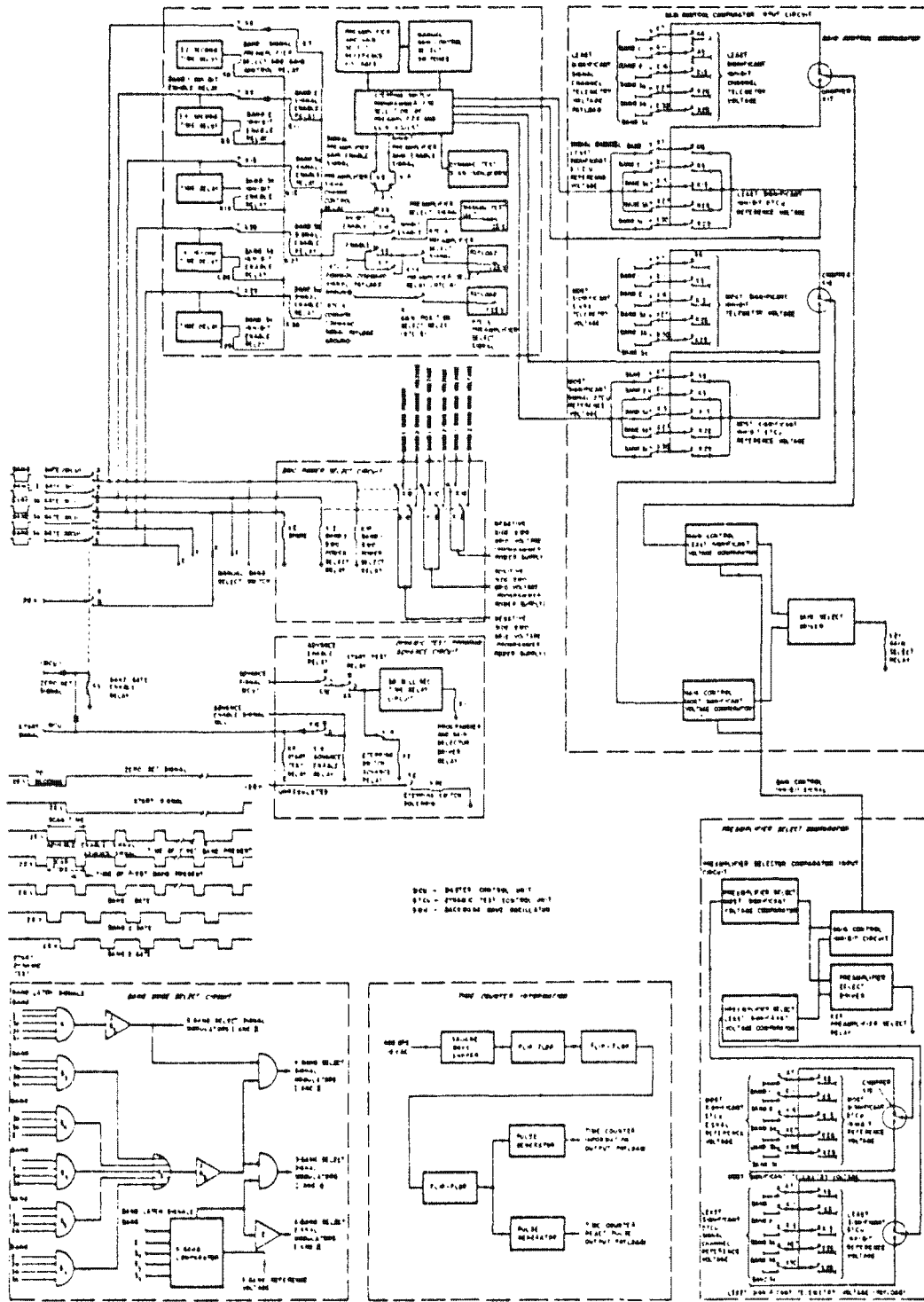
447423-1-081　　　　Figure 4-9　Schematic Diagram of DTCU

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The DTCU signals when manually controlled enable self-testing of the signal generators. Manual controls also provide for the initial selection of the receiver preamplifier gain position in the dynamic test mode. The dynamic test control signals sent to the modulators: (a) set pretest conditions for the dynamic test mode of operation; (b) allow frequency and power sequencing; and (c) program the dynamic test signals.

The pretest conditions determine proper frequency and power sequencing time. The DTCU band mode select signals (derived from the number of receiver band pulses present in one complete payload scan) select the correct time intervals in the modulator frequency and power sequencing circuits. The time intervals programmed for each changing of frequency of the BWO's will vary, depending upon the number of bands being tested. The band mode select circuit determines the correct timing information and sends it to the modulator units via the band mode select signals.

In the dynamic mode of operation, the test signals from the DTCU initiate and maintain the progress of the test. The test signals consists of modulator stepping switch advance signals, one to each modulator, which allow the dynamic test to progress from one scan position to another. There are 20 scan positions of the modulator stepping switches.

Two Nixie indicators on the front panel of the DTCU show the numerical scan position of the modulator units. Twenty-one stepping switch positions are required to complete the 20 scans.

The dynamic test programs for F-2 (flts 1, 2) are shown in Tables 4-2, 4-3, and 4-4.

The simulated command signals supplied to the payload are functions of the dynamic test scan positions. The simulated payload command signals consist of RTC-4, RTC-5, and RTC-8 and can be applied to the payload in either an automatic sequence, as in the dynamic test mode, or in a manual sequence, as is the case in the manual mode of operation.

The attitude information is injected into the payload at various points of the scan positions in the dynamic test program.

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Table 4-2

DYNAMIC TEST PROGRAM FOR BAND 1 OF F-2 (FLTS 1, 2)

Test Frequencies: 2.8 kmc or 2.6, 2.85 and 3.1 kmc

Scan Number	PRF (cps)	PW (μsec)	Signal Channel Amplitude (dbm)	Inhibit Channel Amplitude (dbm)	Payload Data Handler	Gain-Settings Signal Channel Preamplifiers Set to---Position	Gain-Settings Inhibit Channel Preamplifiers Set to---Position
0	-	-	-	-	Normal	Normal	Normal
1	258	21.0	-77	-85.5	Normal		
2	258	21.0	-52	-60.5	Normal		
3	400	10.5	-27	-35.5	Normal		
4	400	10.5	-77	-77.5	Normal		Off
5	400	10.5	-52	-52.5	Normal		Normal
6	400	10.5	-27	-27.5	Normal		Off
7	400	10.5	-52	-60.5	Normal	Minimum	Maximum
8	400	1.0	-77	-85.5	Normal	Normal	Normal
9	400	1.0	-77	-85.5	Normal	Normal	
10	400	30.0	-52	-60.5	Normal	Minimum	Minimum
11	24 kc	1.0	-27	No signal	Normal	Minimum	Minimum
12	34 kc	1.0	-27	No signal	Normal	Minimum	Minimum
13	120	21.0	-52	-60.5	Normal	Minimum	Minimum
14	129	21.0	-52	-60.5	Normal	Minimum	Minimum
15	258	21.0	-52	-60.5	Redundant	Minimum	Minimum
16	400	10.5	-52	-60.5	Redundant	Minimum	Minimum

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Table 4-2 (contd)

Scan Number	PRF (cps)	PW (μsec)	Signal Channel Amplitude (dbm)	Inhibit Channel Amplitude (dbm)	Payload Data Handler	Gain-Settings Signal Channel Preamplifiers Set to---Position	Gain-Settings Inhibit Channel Preamplifiers Set to---Position
17	120	28.0	-52	-60.5	Redundant	Minimum	Minimum
18	129	28.0	-52	-60.5	Redundant	Minimum	Minimum
19	24 kc	1.0	-27	No signal	Redundant	Minimum	Normal
20	34 kc	1.0	-27	No signal	Redundant	Normal	

Table 4-3

DYNAMIC TEST PROGRAM FOR BAND 2 OF F-2 (FLTS 1, 2)

Test Frequencies: 9.5 kmc or 9.1, 9.5 and 9.9 kms

Scan Number	PRF (cps)	PW (μsec)	Signal Channel Amplitude (dbm)	Frequency (kmc)	Inhibit Channel Amplitude (dbm)	Payload Data Handler	Gain-Settings Signal Channel Preamplifiers Set to---Position	Gain-Settings Inhibit Channel Preamplifiers Set to---Position
0	-	-	-	9.1 9.5 9.9	- - -	Normal	Normal	Normal
1	258	21.0	-77	9.1 9.5 9.9	-84.0 -85.0 -87.5	Normal		
2	258	21.0	-52	9.1 9.5 9.9	-59.0 -60.0 -62.5	Normal		
3	400	10.5	-27	9.1 9.5 9.9	-34.0 -35.0 -37.5	Normal		
4	400	10.5	-77	9.1 9.5 9.9	-84.0 -85.0 -87.5	Normal		Off
5	400	10.5	-52	9.1 9.5 9.9	-53.0 -53.0 -53.0	Normal		Normal
6	400	10.5	-27	9.1 9.5 9.9	-28.0 -28.0 -28.0	Normal		Off
7	400	10.5	-52	9.1 9.5 9.9	-59.0 -60.0 -62.5	Normal	Minimum	Maximum

Table 4-3 (contd)

Scan Number	PRF (cps)	PW (μsec)	Signal Channel Amplitude (dbm)	Frequency (kmc)	Inhibit Channel Amplitude (dbm)	Payload Data Handler	Gain-Settings Signal Channel Preamplifiers Set to---Position	Gain-Settings Inhibit Channel Preamplifiers Set to---Position
8	400	1.0	-77	9.1 9.5 9.9	-84.0 -85.0 -87.5	Normal	Normal	Normal
9	400	1.0	-77	9.1 9.5 9.9	-84.0 -85.0 -87.5	Normal	Normal	
10	400	30.0	-52	9.1 9.5 9.9	-59.0 -60.0 -62.5	Normal	Minimum	Minimum
11	24 kc	1.0	-27	9.1 9.5 9.9	-34.0 -35.0 -37.5	Normal	Minimum	Minimum
12	34 kc	1.0	-27	9.1 9.5 9.9	-34.0 -35.0 -37.5	Normal	Minimum	Minimum
13	120	21.0	-52	9.1 9.5 9.9	-59.0 -60.0 -62.5	Normal	Minimum	Minimum
14	129	21.0	-52	9.1 9.5 9.9	-59.0 -60.0 -62.5	Normal	Minimum	Minimum

Table 4-3 (contd)

Scan Number	PRF (cps)	PW (μsec)	Signal Channel Amplitude (dbm)	Frequency (kmc)	Inhibit Channel Amplitude (dbm)	Payload Data Handler	Gain-Settings Signal Channel Preamplifiers Set to---Position	Gain-Settings Inhibit Channel Preamplifiers Set to---Position
15	258	21.0	-52	9.1 9.5 9.9	-59.0 -60.0 -62.5	Redundant	Minimum	Minimum
16	400	10.5	-52	9.1 9.5 9.9	-59.0 -60.0 -62.5	Redundant	Minimum	Minimum
17	120	28.0	-52	9.1 9.5 9.9	-59.0 -60.0 -62.5	Redundant	Minimum	Minimum
18	129	28.0	-52	9.1 9.5 9.9	-59.0 -60.0 -62.5	Redundant	Minimum	Minimum
19	24 kc	1.0	-27	9.1 9.5 9.9	-34.0 -35.0 -37.5	Redundant	Minimum	Normal
20	34 kc	1.0	-27	9.1 9.5 9.9	-34.0 -35.0 -37.5	Redundant	Normal	

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Table 4-4

DESCRIPTION OF SCANS FOR DYNAMIC TEST PROGRAM

Scan 1   This is an overall receiver check. Three frequencies (low, medi-
um, and high) per band are selected to check the tracking of the
shaft encoder and preselector with the oscillator. An amplitude
of -77 dbm for the signal channel, and -85 dbm for the inhibit chan-
nel, tests the lowest acceptance level of the receivers.* Mistrack-
ing of the preselector may result in failure to obtain an intercept
due to increased insertion loss in the signal channel. A failure of
an intercept can therefore be due to bad sensitivity (noise figure),
receiver mistracking, a wrong threshold setting in the amplitude
comparator, a data handler failure, or a probability of occurrence.**

The PRF counter should read 155 counts (010011011) (258 cps) and
the PW counter should read 42 counts (101010) (21 μsec).

Scan 2   This scan, except for sensitivity, serves the same functions as
scan 1 except at a -52 dbm and -60 dbm power level for the two
channels. A lack of intercept at any frequency will be caused by
mistracking of the receivers, the data handler, or improper log
amplifier action as a function of signal level.

Scan 3   The third scan tests for a 50-db dynamic range of input power for
operation of the receivers. Inhibit action will occur if the signal
channel I-F amplifier limits the high input level.

The PRF counter should read 100 counts (001100100) (400 cps) and
the PW counter should read 21 counts (010101) (10.5 μsec), which
are complementary to the digital number of scans 1 and 2. The
PRF and PW counters are thus checked.

---

* The PRF and PW are selected to test the counters in the data
   handler.

** If evaluation of performance of the probability of occurrence ef-
   fect is desired, scan 1 shall be repeated as many times as
   necessary.

Table 4-4 (contd)

Scan 4   The fourth scan tests the inhibit channel sensitivity at a -79 dbm
power level, and the ability of the amplitude comparator to inhibit
with a 2-db signal-to-inhibit (S/I) amplitude ratio. Changing the
inhibit channel gain to OFF during the scan will result in no inter-
cept for the first two frequencies. The third frequency will pro-
duce an intercept, proving the ability to turn off the inhibit channel
preamplifiers and verifying that the inhibit channel was functioning
for scans 1, 2, and 3.

Scan 5   This scan continues to check the amplitude comparator inhibiting
function at -54 dbm power level. Frequencies 1 and 2 will be
intercepts, verifying the return to the normal gain setting of the
inhibit channel preamplifiers.

Scan 6   This scan tests the inhibit operation of the receiver at an input
power level of -29 dbm.

Scan 7   This scan checks receiver inhibit characteristics at minimum
signal channel and maximum inhibit channel gain. Frequencies 1
and 2 will be intercepts. Frequency 3 will be inhibited, verifying
ability to move signal channel gain to minimum and inhibit gain to
maximum.

Scan 8   This scan tests acceptance level for a 1-μsec pulse at -77 dbm
level with an 8-db S/I ratio. Both signal and inhibit channel gains
are set to normal, and the last 2 intercepts recorded. There is a
probability that the signal will be inhibited during this scan so that
it is repeated for scan 9.

Scan 9   This scan, repeated as many times as necessary, is used to de-
termine the probability of acceptance. This is done by stopping
the dynamic test in this scan.

Scan 10   This scan checks the S/I ratio at -50 dbm. With the signal channel
gain at minimum, frequency 1 will be an intercept and frequency 2

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Table 4-4 (contd)

might be inhibited. After setting the inhibit channel gain to mini-
mum, frequency 3 will be recorded as an intercept. The accept-
ance or rejection of frequency 2 gives an indication of actual S/I
ratio needed at -50 dbm power level and frequency 2.

Scan 11   The PRF of 24 kc is close to the maximum PRF that the data han-
dler will allow due to a blanking gate in the amplitude comparator.
Scan 11 tests that the gate is not too long. By removing the input
to the inhibit channel in band 1, the high amplitude signal tests
the skirt selectivity. The first intercept will be made as soon as
the S/I input ratio is greater than 8 db.* This will occur at the
bottom of the band pass characteristic curve. The inhibit channel
preamplifiers are turned off.
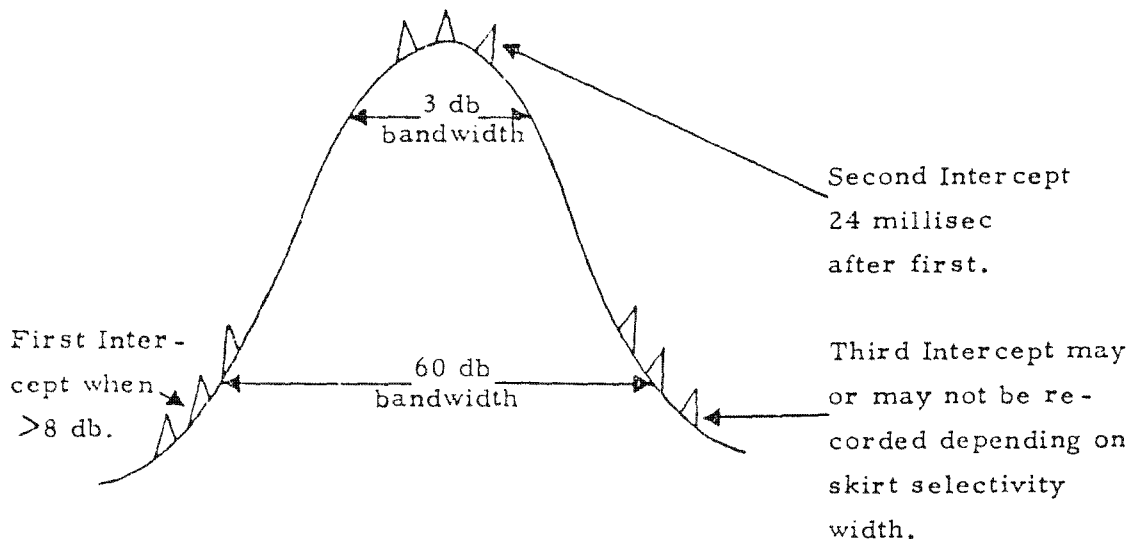
For   <2 intercepts: Selectivity is too narrow.
          2 to 3 intercepts: Selectivity is between 4 and 6 Mc.
             >3 intercepts: Selectivity is too wide.

* The S/I ratio needed for an intercept varies with frequency,
  power level, and PW.

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Table 4-4 (contd)

Explanation of Scan 11

Scan 11 also tests the readout circuit which allows one intercept
every 24 milliseconds. The 1-μsec output generally tests the
receiver's ability to handle this pulse.

Scan 12   Scan 12 in conjunction with scan 11 checks skirt selectivity. The
34-kc PRF tests that the amplitude comparator blanking pulse is
not too small. The 34-kc PRF should be counted every 35 μsec.
Since the pulse interval is less than the blanking pulse, every
other pulse will be recorded. The PRF counter should read 17 kc
due to the dividing action of the blanking pulse.

Scan 13   The purpose of scan 13 is to check the non-verification reset time
in the computer. If a second pulse is not received within 8 milli-
seconds of the first pulse, the intercept is considered non-verified
and the computer is reset for further intercepts.

Scan 14   The 129-cps PRF tests that the non-verified reset circuit is not
too short. Its pulse interval is 7.75 milliseconds.

Scan 15   This is the first test of the redundant data handler. Scan 15 is the
same as scan 2. The remaining scans test the redundant data han-
dler as in scans 1 to 14.

Scan 16   This is the same as scan 3 except the signal channel amplitude is
-52 dbm and the inhibit channel amplitude is -60 dbm. The redun-
dant data handler counters are checked.

Scan 17   Same as scan 13 with redundant data handler.

Scan 18   Same as scan 14 with redundant data handler.

Scan 19   Same as scan 11 with redundant data handler.

Scan 20   Same as scan 12 with redundant data handler.

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The time counters are reset in the pretest portion of the dynamic mode.

During the dynamic test portion, the dynamic test control unit injects a 50-cps clock pulse for 14 of the 20 receiver scans.

The redundant computer is then put into operation, reset, and then allowed to start counting the same DTCU clock pulse.

The gain settings of the preamplifiers in the payload are set to their normal position during the pretest period. The normal gain position setting is controlled by the GAIN SELECT switch on the DTCU. The gain positions can also be controlled in the manual mode. During the dynamic test the preamplifier gains are set to maximum and minimum and returned to normal gain settings.

4.9 MANUAL CALIBRATION OF SIGNAL GENERATORS

The manual calibration of the signal generators is accomplished, by means of the manual test unit, when the payload equipment is in the manual mode of operation. The MANUAL ADVANCE switch on the manual test unit steps the DTCU to any desired scan position and sets the modulation characteristics of the signal source by programming the modulators to the desired type of output signal. The manual CW-PULSE SELECT switch on the modulator unit enables power and frequency calibrations in either the CW or the pulse output type of operation. The BAND SELECT switch on the DTCU applies anode and grid voltages to the appropriate BWO and grid and anode remote control voltages to the corresponding modulator units.

4.10 BAND MODE SELECTION

After the payload receivers are turned on, through the master control unit, the monitor 1 unit supplies the DTCU with various band gates that are fed back from the payload as a control signal for the checkout equipment. This signal permits the DTCU to automatically select the correct combination of checkout equipment circuits for two-, three-, four-, or five-band operation. Logic adders, inverters, and AND gates allow the appropriate relays

to be energized, depending upon the number of bands in use. The energizing
of the relay selects the correct time-sequencing signal for the modulator unit,
and thus controls the time interval during which a particular frequency is in-
jected into the payload. One complete payload test scan is necessary to ener-
gize the proper relay.

4.11 PREAMPLIFIER GAIN ADJUSTMENT

A feedback system is used for automatically adjusting the gain of the payload
preamplifiers. A two-level telemetering code (provided in the payload for
monitoring preamplifier gain settings) is used for the feedback signal. Each
level of the telemetering code consists of a voltage that is part of a four-
voltage divider network. There is a set of levels for monitoring the correct-
ness of the PREAMPLIFIER SELECT position while other levels monitor the
preamplifier gain settings. The DTCU utilizes the telemetering outputs to
automatically select a preamplifier and change its gain setting. The change
of the gain setting is accomplished during the time when that particular band
gate is ON. This band gate energizes a six-pole relay that connects any one
of four reference voltages from the DTCU and the corresponding telemetered
voltage, to the voltage comparators.

The presence of an error signal in the output of the comparator is used to
trigger two monostable multivibrators. One of the multivibrators drives a
relay at a rate of 10 cps for 50 milliseconds. The contact closures of RTC-4
step the preamplifier select stepping switches in the payload until the com-
parator output error signal disappears, deactivating RTC-4. Upon the deac-
tivating of RTC-4, the gain select inhibit signal (derived from the preamplifier
select voltage comparator error signal) disappears and the gain select circuit
is allowed to send RTC-5 to the payload and to select the proper gain setting
in the same manner as the preamplifier select circuits. The reference volt-
ages will vary depending on the particular gain desired. Three different
gain positions are programmed during the dynamic test.

The three stepping switches in the DTCU impress the reference voltages upon
the relay contacts.

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In both the automatic test mode and the manual calibration mode, the preamplifiers are set to their normal gain positions when the stepping switches are in the zero scan position.

Twenty 4-position switch--- select the appropriate reference voltages for normal gain settings. (.ie switches are located on the rear panel of the DTCU.)

The preamplifier gains are changed to their maximum, minimum, and normal settings during the dynamic test. The stepping switch energizes an enabling relay in either the signal or inhibit channel each time the gain settings in that channel are altered. This relay permits gain control action when energized and inhibit action when de-energized.

4.12 DYNAMIC TEST SEQUENCE

Before the actual starting of the dynamic test, the payload receivers are turned on by a signal from the master control unit. A zero scan signal from the same unit sets the DTCU in the zero scan position. At the end of the 70-second warmup delay or pretest duration, during which time the receivers are set to their normal gain positions, the zero scan signal is removed, and the start dynamic test signal is sent by the master control unit to the DTCU. This signal latches relay K4, Figure 4-9, which in turn, permits the advance signal to pass through K16 and K4 to the stepping switch advance relay, K2. After 50 milliseconds K1 is energized, de-energizing K2 and allowing the program stepping switches to advance. The advance signal is a band gate, selected on the basis of the receiver bands in use at a particular time, and generated by the first receiver band of the group in use. The gate-actuated relay K2 makes it possible for the advance signal to activate the stepping switches in the DTCU. The stepping switches will proceed through the 20 scans of the dynamic test program.

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4.13 MODULATORS FOR BANDS 1 AND 2

The modulator unit (Figure 4-10) supplies modulation pulses of preprogrammed widths and repetition rates to the BWO. It also supplies programmer d-c voltages for varying the frequency and power output of the BWO. Programmed control voltages for the signal source attenuator setting are also contained in the modulator unit.

Different RF's (listed in Tables 4-2 and 4-3) are used for the various required modulation characteristics. These are: (a) 34 and 24 kc from Wien bridge oscillators, (b) 400 cps from the 400-cps power supply in the checkout equipment, (c) 258 cps and 129 cps through dividers from 516-cps tuning fork oscillator, and (d) 120 cps, a multiple of the 60-cps power line. A monostable multivibrator synchronized to the above signals will drive either of two pulse generators to produce any one of four PW's, namely, 1, 10.5, 21, or 28 μsec or the actual modulation signal.

Provisions are made in the DTCU for automatically selecting the correct timing of the frequency and power sequencing circuits. The band mode select signals, which are based on the specific group of frequency bands (two, three, etc.), energize one of four relays in the modulator unit. The contacts select the proper time constant of two time delay circuits. The time delay circuits sequentially energize a series of relays which change frequency and power output of the BWO during the ON time of the band gate sent from the DTCU. The anode and grid voltages of the BWO are programmed in three steps during the scan time of the particular band. The modulator units also program power output of the signal source units, with stepping switches in the modulator units. The modulators also include provisions for frequency and output power measurements.

The accuracies of the front-of-panel accessible frequency and power measuring facilities are ±0.1 percent and ±0.5 db respectively.

The measurements are used in the manual mode of operation for calibrating the signal sources. The front panel switch allows calibration at one of five different frequencies which can be injected into the payload. The modulators

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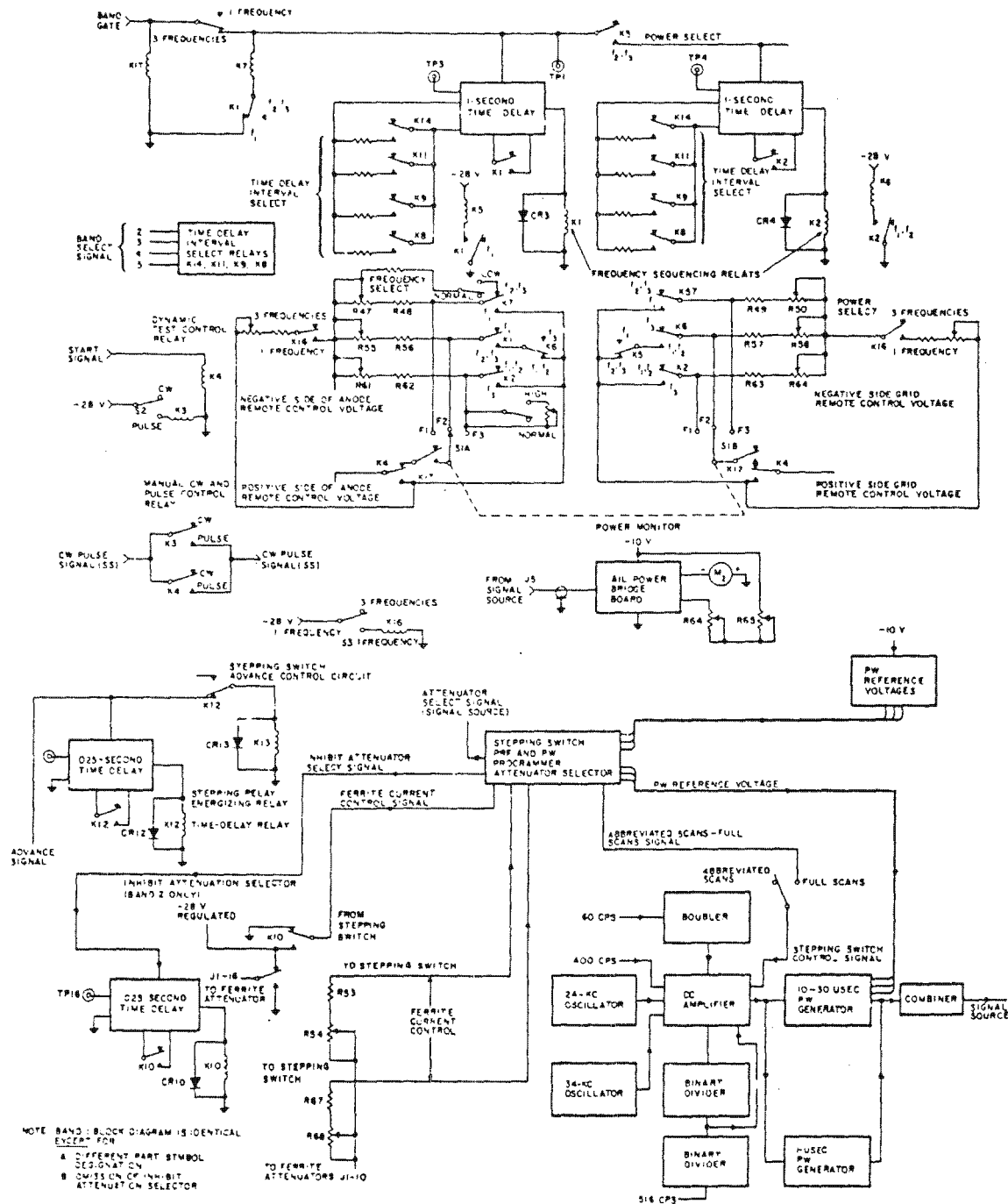
Figure 4-10 Block Diagram of Modulator Unit

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have the capability of injecting the end frequencies of the band or any of the three stepped frequencies into the payload in the manual mode of operation. In the dynamic mode, the modulators, by means of switches located on the rear panel, can inject into the payload only one frequency or the three step frequencies per scan. They can also eliminate modulation pulses after scan 14 of the dynamic test.

To calibrate the signal source parameters the checkout equipment is put in the manual mode of operation. The BAND SELECT switch in the DTCU is then set to the desired band, thereby activating that particular signal source unit. The FREQUENCY SELECT switch on the modulator front panel then selects one set of anode and grid voltages for the BWO for the particular frequency and power output desired. The frequency of the signal source is measured, using a calibrated wavemeter on the signal source unit tuned for a "dip" on a front panel power meter of the modulator unit. The power output of the BWO is also read on the same meter. The FREQUENCY ADJUST potentiometer provides a ±10 percent variation in frequency. Similarly, a ±10 percent variation of BWO output power is possible through adjustment of the POWER potentiometer. After calibration of the three frequencies and power levels within the particular band, the modulator unit is ready for test operation. The STATIC-DYNAMIC switch (S4) on the master control unit is then turned to the DYNAMIC position and the START TEST button (S3) is pressed, causing the stepping switch to move to its zero scan position. The modulator advance signal from the DTCU advances the modulator pulse and sets the correct attenuation for desired power-level outputs of both signal and inhibit channels. For programming the three frequencies within each band, the band-switching gate is applied to two time-delay circuits, which energize relays sequentially after specified time delays, depending upon the number of bands under test. The first test frequency signal is injected into the payload. At the end of the first time delay, the first relay is energized, and the frequency and power control voltages are programmed to inject the second test frequency signal. The second relay, energized by its time delay circuit, causes the third test frequency signal to be programmed and injected into the payload. This frequency sequencing takes place during every one of

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the 20 scan positions of the modulator 2 stepping switch. Tables 4-2, 4-3, and 4-4 give the detailed modulation and other characteristics for each of the 20 scans. Table 4-5 is a chart of intercepts provided for in each frequency in the 20 scans. At the end of the dynamic test, all the power is removed from the modulator unit, and the stepping switch is sequenced back to its zero position.

4.14 BAND 1 SIGNAL SOURCE UNIT

Figure 4-11 is a schematic diagram of the band 1 signal source unit, including the R-F oscillator, attenuators, R-F power distribution circuits, control circuits, and modulation circuits. A Raytheon type QK691 BWO (tunable from 2150 to 3150 Mc) is used as a grid-modulated signal source. Since the BWO is voltage tunable, the programmable anode supply voltage determines the frequency. A similarly programmable grid supply voltage controls the output power at each frequency. The direct-reading frequency meter, with an absolute accuracy of ±0.1 percent and a built-in thermistor for use in conjunction with an AIL power bridge, is included for frequency and output level adjustments. The coaxial switch-attenuator-pad combination, which is automatically programmed, obtains the required output signal amplitudes. A hybrid, used as a power splitter, provides dual channel output for signal and inhibit antenna feeding. Another programmable attenuator varies the output amplitude of the signal channel relative to the inhibit channel. A pad in the output of each channel assures a 50-ohm source impedance. A pulse amplifier is included for modulation of the BWO. A transistorized time delay and a BWO protection circuit are also incorporated.

The signal source unit for band 1 is capable of providing the following overall accuracies over its measuring band:

    a.   Frequency: ±0.2 percent

    b.   PRF: ±0.5 percent

    c.   PW: ±1.0 percent

    d.   R-F signal amplitude variation: 60 db

    e.   Output level for either one of the dual channels: variable from
        -20 db to -30 db ±2 db

Table 4-5

CHART OF INTERCEPTS

Number of Intercepts

Scan	Frequency 1	Frequency 2	Frequency 3
1	1	1	1
2	1	1	1
3	1	1	1
4	0	0	1
5	1	1	0
6	0	0	2
7	2	2	0
8	0	1 or 0	1
9	1	1	1
10	1	0 or 1	1
11	3	3	3
12	3	3	3
13	0	0	0
14	1	1	1
15	1	1	1
16	1	1	1
17	0	0	0
18	1	1	1
19	3	3	3
20	3	3	3

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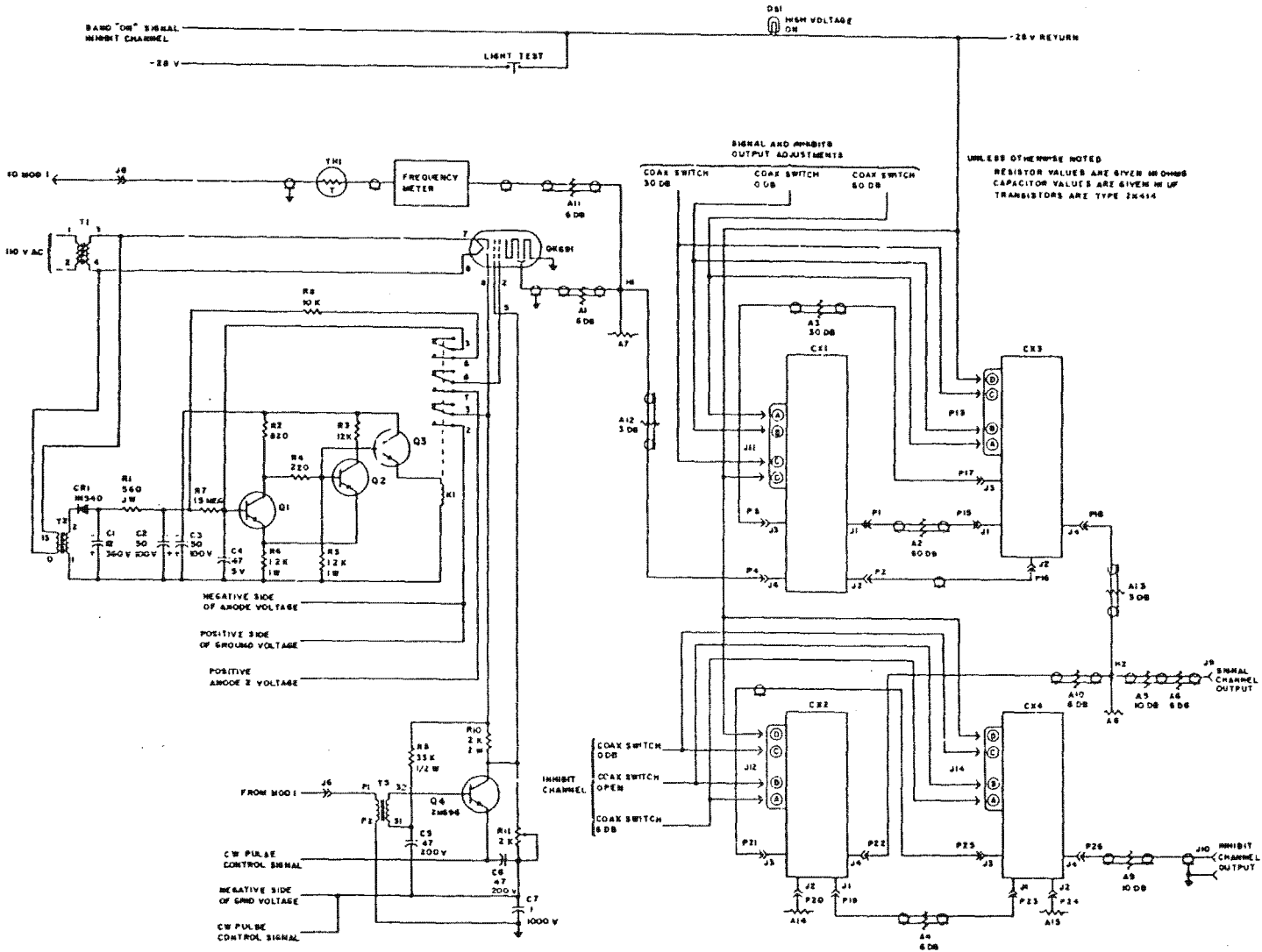
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Figure 4-11 Schematic Diagram of Band 1 Signal Source

4.15 BAND 2 SIGNAL SOURCE UNIT

The band 2 signal source unit is shown in Figure 4-12. A Varian VA-161 BWO is used as a grid-modulated signal source. A programmable anode supply varies frequency. Power output variations due to frequency sensitivity of the BWO, as well as due to differences between BWO tubes, are compensated for through a programmable grid supply. To prevent frequency pulling of the BWO, a ferrite isolator with a minimum isolation of 25 db over its band and a maximum insertion loss of 1 db is used at the output of the BWO. Two 25-db programmed step attenuators obtain the required signal output amplitudes. Dual channel output is provided by using a waveguide hybrid as a power splitter. Another ferrite attenuator varies the output of the inhibit channel relative to the signal channel. Output pads are used to assure a matched source impedance. A transistorized BWO protection circuit and a pulse amplifier for modulation are incorporated.

The signal source unit for band 2 is capable of providing the following over-all accuracy over the measuring band:

  a. Frequency: ±0.2 percent
  b. PRF: ±0.5 percent
  c. PW: ±1.0 percent
  d. R-F signal amplitude variation: 50 db
  e. Output level for either one of the dual channels: variable from -20 db to -80 db ±2 db

A direct-reading frequency meter and a built-in thermistor used in conjunction with an external power bridge provide frequency and power measurements during adjustments.

4.16 SIGNAL SOURCE AND MODULATOR FOR BANDS 3b AND 3c

A proposed block diagram of the R-F portion of the signal source for bands 3b and 3c is shown in Figure 4-13. Three spot frequencies are provided in each band. Frequency selection, output level adjustment as well as signal-to-inhibit relative power level adjustments are made through coaxial switches and suitable fixed and variable attenuators.

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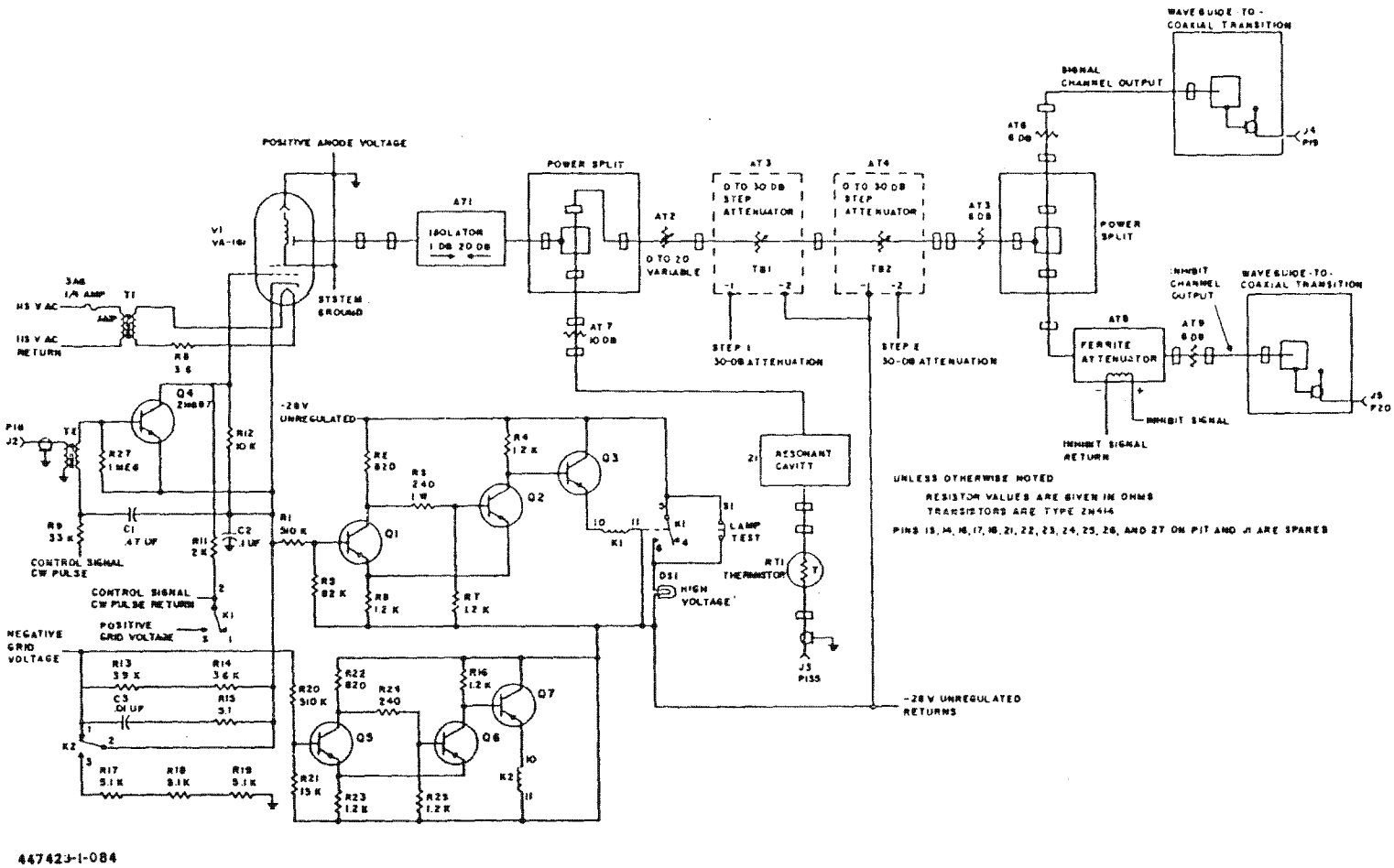
Figure 4-12 Schematic Diagram of Band 2 Signal Source

Consideration is being given to possible modification of the band 2 modulator for use in bands 3b and 3c, if it is feasible. Should this appear inadvisable, new modulators for bands 3b and 3c will be designed.

The initial F-2 checkout equipment is being designed for F-2 (flts 1, 2) payloads. Retrofit units will adapt it for the later F-2 (flts 3, 4) payloads.

4.17 ANTENNA ADAPTERS

4.17.1 General Description

The antenna adapters are devices used to inject R-F test signals into the payload antennas. The antenna adapters are fed from the signal source outputs by standard transmission line components and have output terminals suitable for direct coupling to the antenna under test.

To efficiently couple energy into a circularly polarized antenna, a circularly polarized adapter is required. In addition, such an adapter must be optimized over the frequency band with respect to ellipticity and transmission line discontinuities. The composite effect of these appears as an additional insertion loss of the adapter-antenna combination. Assuming a perfect adapter, the overall insertion loss versus frequency characteristic is then dependent upon the characteristics of the antenna.

4.17.2 Band 1 Antenna Adapter

The band 1 antenna adapter (Figure 4-14) is a coaxial device used to inject calibration signals from the checkout equipment signal source into the payload antenna. It consists of three coaxial hybrids and provides four outputs of equal amplitudes and with relative phases of 0°, 90°, 180°, and 270°. This combination will produce a circularly polarized wave when fed into the four terminals represented by the coaxial sleeves of the turnstile antenna. Connection is made by a special adapter which plugs into the sleeve dipole as an extension of the coaxial line with the sleeve. Interconnecting lines are coaxial cables.

COAXIAL COUPLING
MECHANISM WITH
TRANSFORMERS

TURNSTILE ANTENNA

COAXIAL OUTPUT CONNECTOR
OF CIRCULARLY POLARIZED
TURNSTILE ANTENNA

COAXIAL INPUT CONNECTOR
TO ANTENNA COUPLER
(FROM SIGNAL SOURCE)

447423-1-066

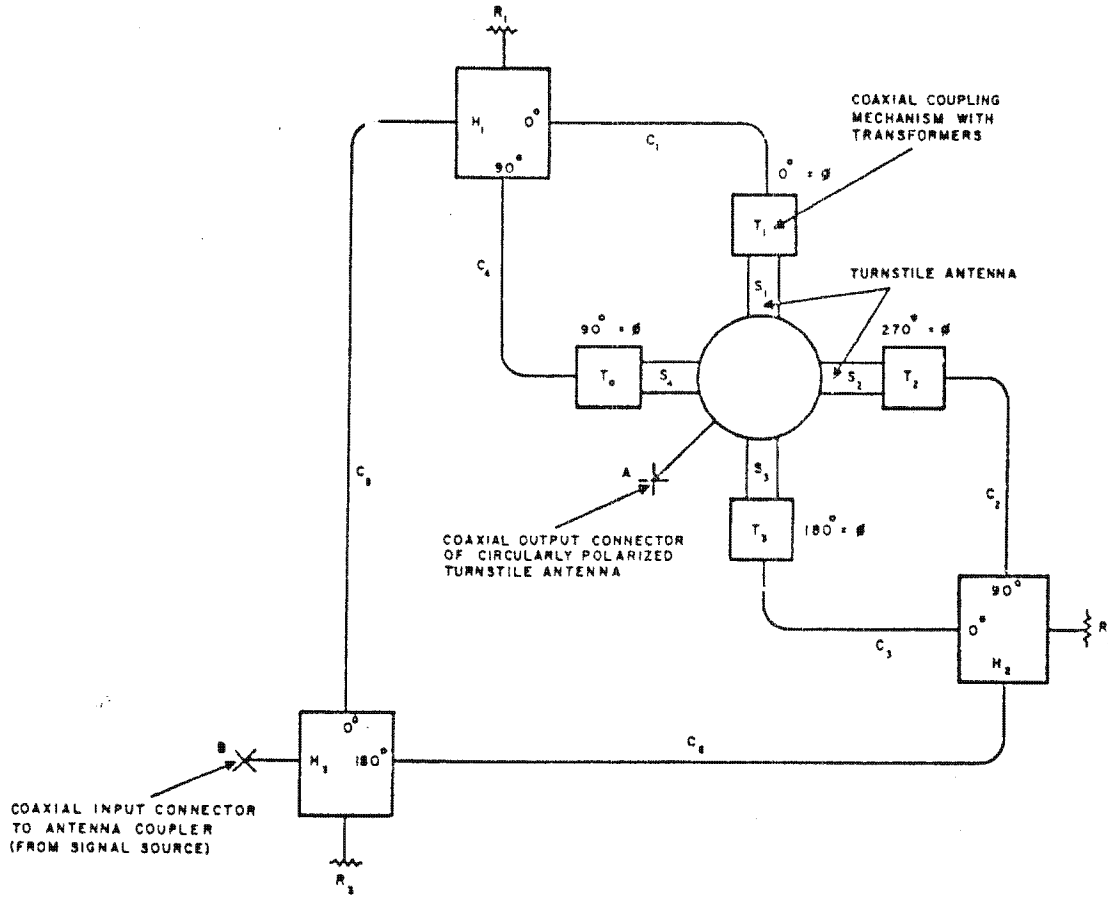Figure 4-14 Block Diagram of Band 1 Antenna Adapter

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Typical performance curves for several models of turnstile antennas exhibit periodic variation of overall insertion loss between 2 to 5 db. These variations are the cyclical effects of rotating polarization ellipses and discontinuities. It is felt that adapters should be mated to each antenna due to variations between antennas. SWR measured at the adapter input, when coupled to the antenna, will be less than 2:1.

4.17.3 Band 2 Antenna Adapter

The band 2 adapter (Figure 4-15 and 4-16) is a waveguide structure which couples calibration signals from the signal source into the payload antenna by direct contact with the antenna. The circular polarization is generated by a waveguide dielectric phase shifter and an inclined waveguide to generate the orthogonal components of the field.

Representative curves for this unit exhibit insertion loss variations of from 0.5 to 2.5 db. Each adapter and antenna combination will be matched. Internal reflective losses and polarization ellipse orientation account for the 2.5-db peak insertion loss for this device in combination with a typical antenna. SWR data at the input to the adapter, when coupled to the antenna, will be under 2:1.

4.18 F-2 TEST BOX AND DUMMY LOAD UNIT

4.18.1 General Description

The purpose of this unit is to verify the proper functioning capabilities of the F-2 checkout equipment. It accomplishes this in conjunction with various standard commercial equipments by injecting calibrated inputs, indicating the presence of required outputs and generally simulating payload signals under checkout conditions. The simulated Subsystem C power supplies provided by the checkout equipment are checked for compliance with the payload power supply specifications under peak loads normally imposed by the payload. The test box and dummy load unit is shown in Figure 4-17. A drawing of the panel is shown in Figure 4-18.

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FIXED DIELECTRIC
PHASE SHIFTER

TE_{10}

COAXIAL INPUT TO
WAVEGUIDE ADAPTER
(FROM SIGNAL SOURCE)

TE_{10}

$45°$

TE_{10}

$45°$

TE_{01}

TE_{01}

SQUARE WAVEGUIDE OUTPUT OF
ADAPTER ASSEMBLY
(CONTACTING MECHANISM FOR USE BETWEEN
ADAPTER AND ANTENNA - NOT SHOWN)
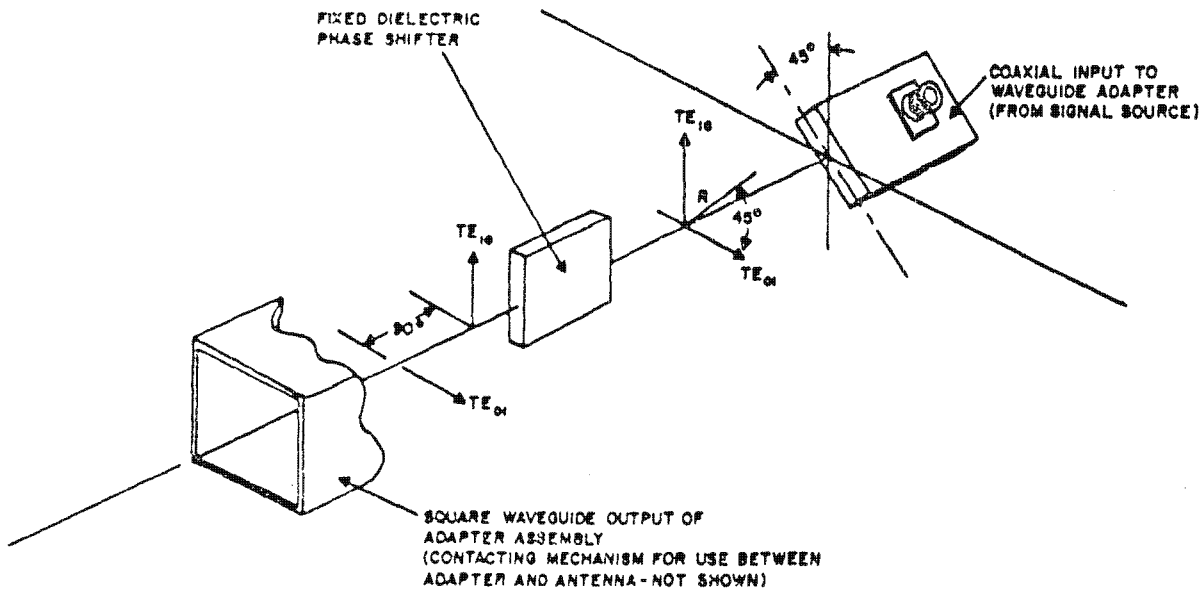
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Figure 4-15 Block Diagram of Band 2 Antenna Adapter

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Figure 4-16 Block Diagram of Band 2 Antenna and Adapter Assembly

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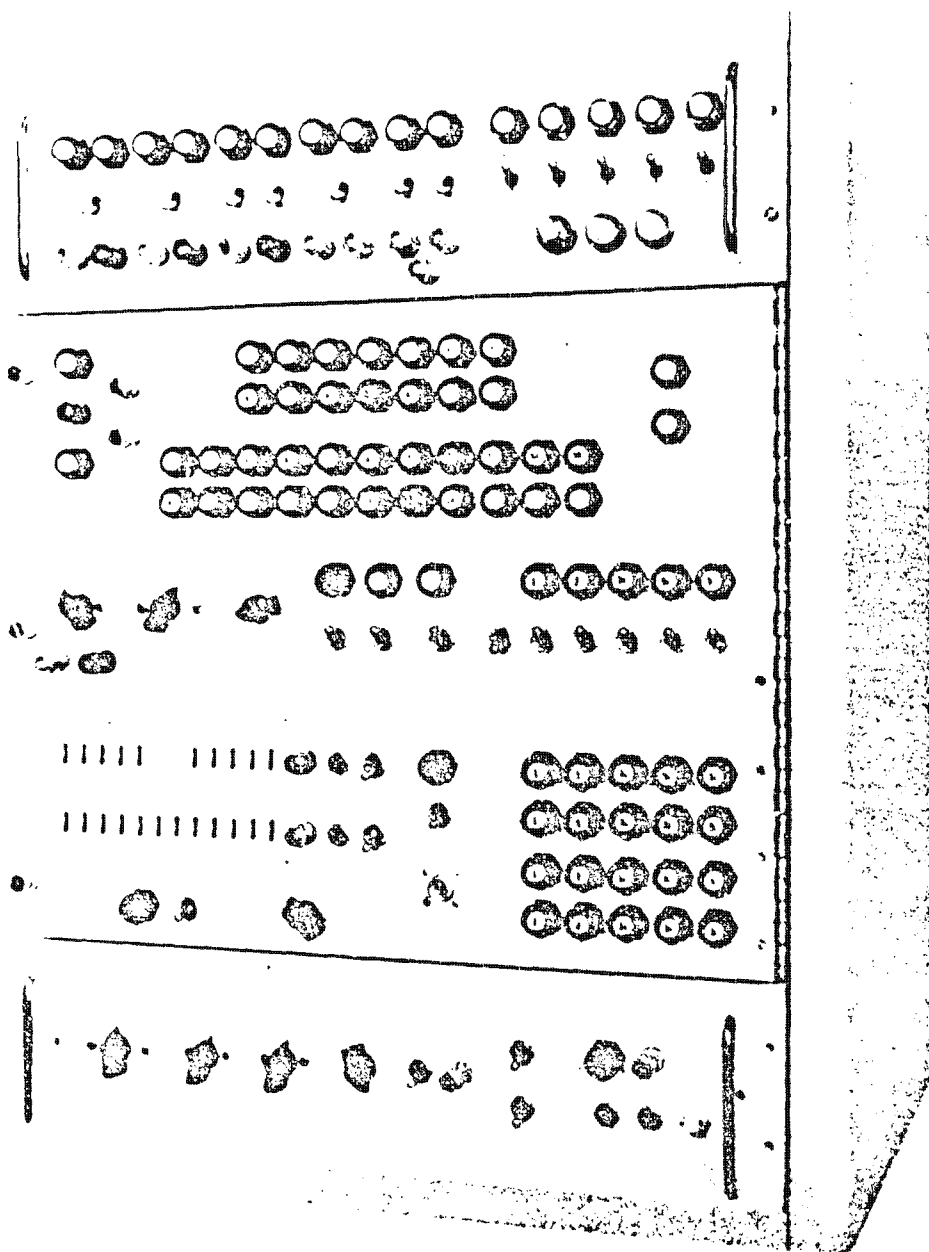
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Figure 4-17 Test Box and Dummy Load

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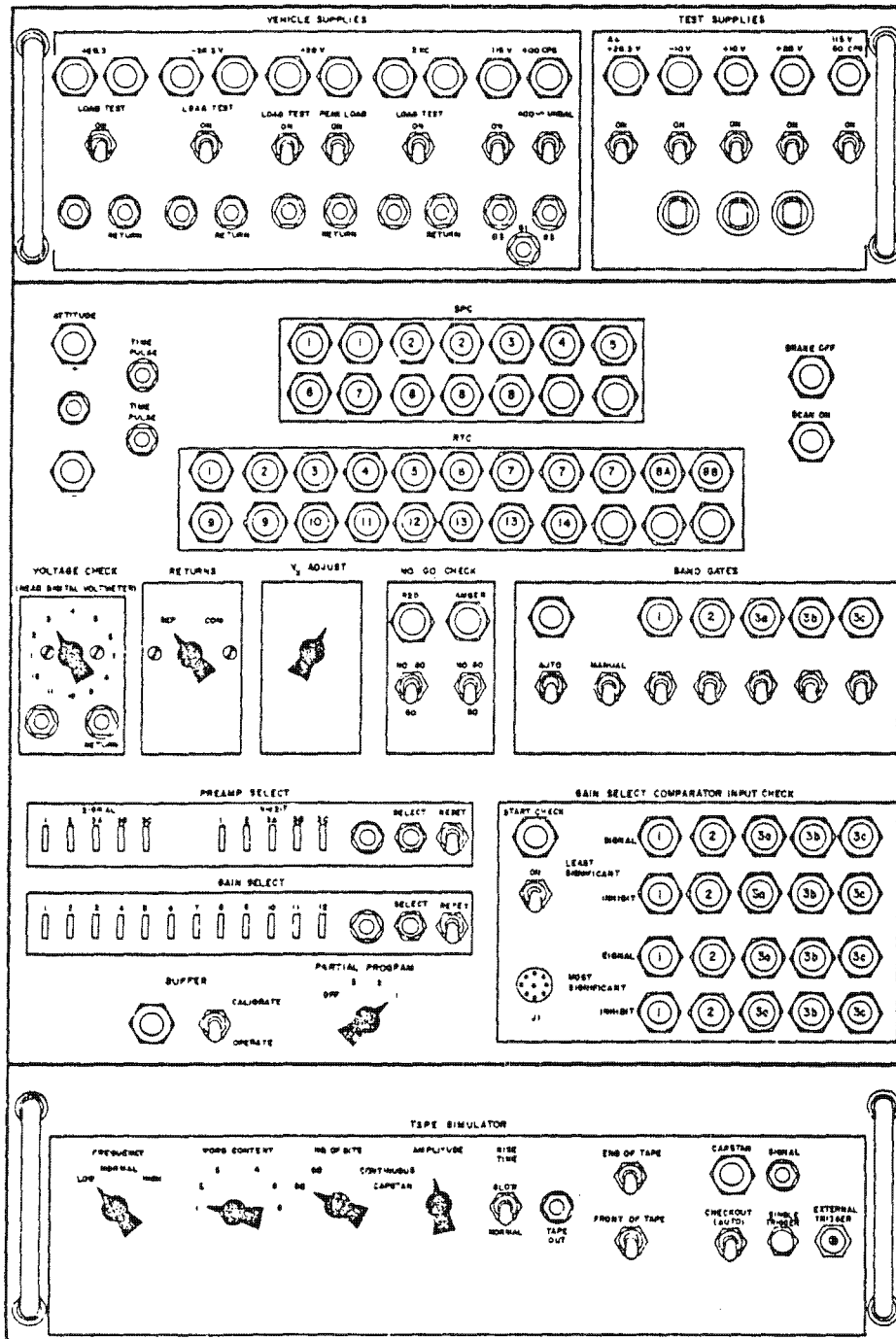
447423 1-089

Figure 4-18 Panel of Test Box

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Interconnection between the checkout equipment and the test box and dummy load unit (TBDLU) is made through the same cables and connectors used to mate the checkout equipment with the payload. The TBDLU incorporates the means for checking, testing, and verifying every input and output of the checkout equipment by simulation of payload circuit characteristics and/or functions. The condition of each command in the simulated Subsystem H portion of the checkout equipment is indicated by lights on the TBDLU front panel. Similar indicators are used for checking the presence and polarity of the attitude signal.

The monitor portion of the checkout equipment is tested with 48 different voltages derived from a precision divider located in the TBDLU. This includes both critical and non-critical no-go voltages introduced into the checkout equipment in the manner of voltages from payload monitor points.

Band gate voltages are provided by a repeat cycle timer located in the TBDLU controlled by logic in the checkout system. The presence of each band gate voltage is indicated by lights on the TBDLU front panel.

The gain and preamplifier selection circuits in the checkout equipment are checked by electronically closing the loop with circuits in the TBDLU. The four simulated telemeter code voltages are set up by means of potentiometers with emitter-follower outputs. The preamplifier sel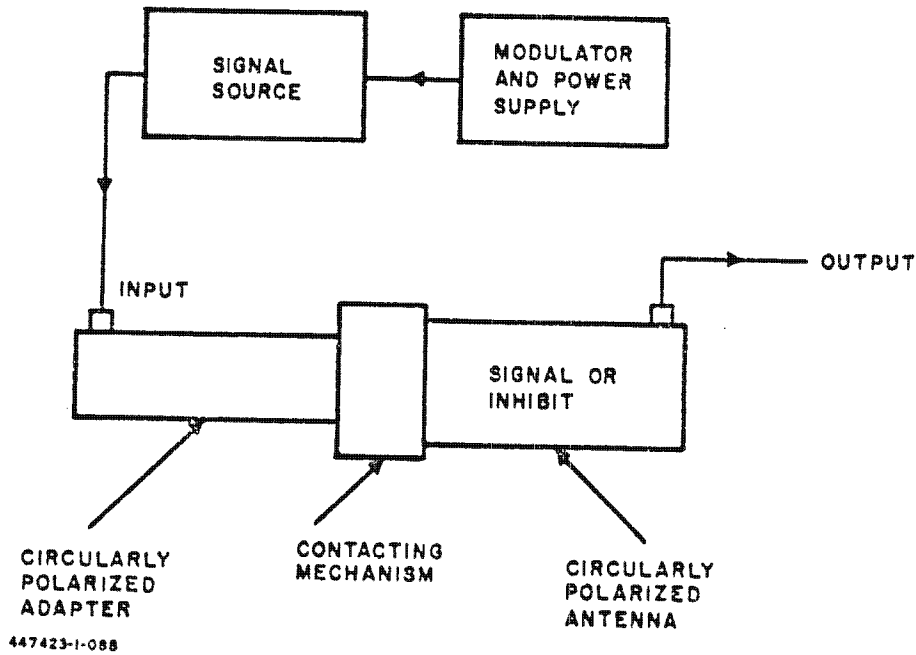ect and gain select functions in the checkout equipment are verified by simulation, in the TBDLU, of the corresponding payload telemeter code voltages. The TBDLU converts the error signal output from the gain and preamplifier comparators in the checkout equipment to step a binary counter in the TBDLU until the combination of code voltages selected is the same as the reference inputs to the comparators. Front panel indication of the chosen preamplifier and gain setting is provided on the TBDLU.

The tape simulator portion of the TBDLU contains a test word generator with the following capability:

    a.   PRF: 1.   20 kc

                                     2.   12 kc

                                     3.   4 kc

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b.	Word content selector:	1.	All 1's
		2.	All 0's
		3.	Alternate 0's and 1's
		4.	Alternate 1's and 0's
		5.	Two 0's, eight 1's repetitive
		6.	Two 1's, eight 0's repetitive
c.	Number of bits selector:	1.	50 bits
		2.	60 bits
		3.	Continuous (free running)
		4.	External (capstan) controlled
d.	Amplitude adjust potentiometer:		Continously variable from 20 v to 0 v.
e.	Rise-time switch:	1.	$2 \mu sec$
		2.	$4 \mu sec$

A block diagram of the tape simulator is shown in Figure 4-19 and the simulator waveforms are shown in Figure 4-20.

4.18.2 Test Word Generator

The test word generator uses a gated multivibrator to provide a burst of 50 astable pulses. One output is fed into the 1's generator, producing a burst of negative going pulses. These pulses are gated by the blanking signal of the scale-of-ten counter to give a proper pattern of 1's. The other output of the multivibrator is fed into the 0's generator and produces a burst of positive going pulses. These are gated by the blanking signal of the scale-of-ten counter to give a desired pattern of 0's. The blanking is arranged so that when a 1 is produced, a 0 is inhibited, and vice versa. The 1's and 0's signals are combined in the inverting combining gate to produce a burst of correct polarity 1's and 0's. An emitter follower generates a low impedance signal. When the scale-of-ten counter resets five times, the scale-of-five counter gives a signal which shuts off the oscillator at 50 counts. A reset pulse is used to restart the oscillator and repeat the sequence. By proper
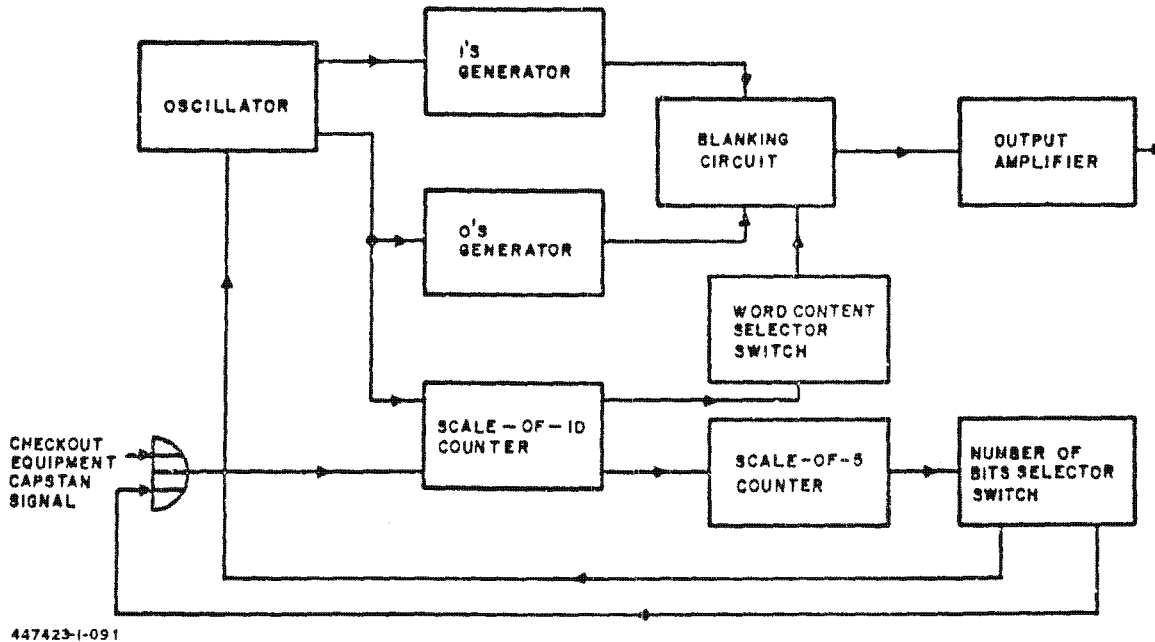
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Figure 4-19 Block Diagram of Tape Simulator

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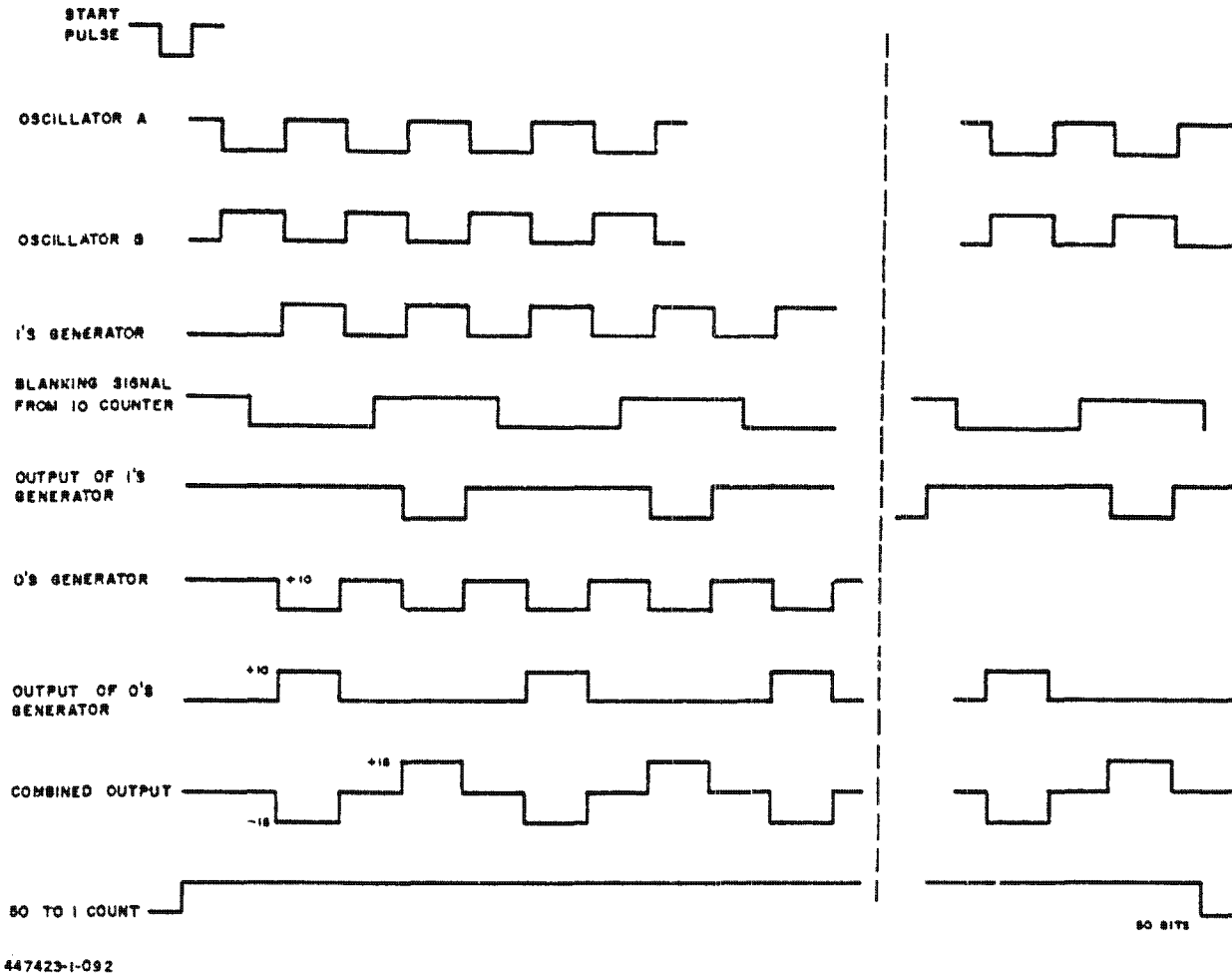
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Figure 4-20   Waveforms of Tape Simulator

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selection of the different outputs of the scale-of-ten counter, six different patterns of 1's and 0's can be produced. A switch on the front panel of the TBDLU provides for this selection.

Provision for frequency variation is made by r-c adjustment in the oscillator and the 1's and 0's generator. Similarly, flexibility is provided for signal amplitude variation, free-running multivibrator operation and word length increase to 60 bits through a change of the scale-of-five counter to a scale-of-six counter.

4.19 CHECKOUT DATA HANDLER

The general requirements for the data handler unit are as follows:

 a. The unit shall process digital information in an open loop fashion, printing correct as well as incorrect information.

 b. The 3-level return-to-zero binary code of the payload shall be converted to decimal form and recorded on a digital printer.

 c. The digital word shall be broken up into subwords; the information obtained from these shall be:

  1. Parity check

  2. Numbered bits in word

  3. Time of intercept (seconds)

  4. Pulse repetition period 2 (PRF-2) (milliseconds)

  5. Pulsewidth (microseconds)

  6. Pulse repetition period 1 (PRF-1) (milliseconds)

  7. Band number

  8. Channel number

 d. For PRF-1 and PRF-2, each count shall be converted to 0.025 millisecond for two-band operation and to 0.05 millisecond for three-band operation.

 e. For PW, each count shall be converted to 0.5 μsec.

 f. The channel number shall be converted from a 1's complement-gray code to binary code, and then to the final decimal code.

 g. A symbol shall be assigned and printed to indicate the subword processed.

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h.   A self-test capability shall be included. This shall make use of a
     test word generator, providing test words of alternate 1's and 0's,
     all 1's, or all 0's.

i.   A signal from the master control unit shall automatically stop the
     self-test function and permit the payload tape words to be entered.

j.   A second signal from the master control unit shall start the word
     processing. Automatic termination of the processing shall occur on
     a signal from a timer, which is reset at the beginning of the tape
     processing.

k.   The payload tape shall automatically be started and stopped for the
     processing of each word for thirty minutes, after which time the
     tape shall go to the end.

l.   Capability for changing the number of subwords being processed
     without equipment modification shall be included in the design.

m.   Capability of changing the scale factors for the processed data shall
     be included in the design of the equipment.

n.   Capability for expansion to a 60-bit word without modification to the
     equipment shall be included in the design.

The data handler unit contains about 250 plug-in cards, which are standard
AIL digital building blocks. Most of these cards consist of four standard
circuits; a few of the cards consist of nonstandard circuits for input and out-
put connections. The standard cards are arranged in what might again be
called standard circuits, such as binary counters, decimal counters, inhibit
gates, pulse generators, and a shift register. The arrangement of these
circuits into an overall logic diagram results in a system that meets the de-
sign requirements of the data handling functions. Figure 4-21 is a block
diagram of this system, showing the arrangements of the various circuits.

The AIL digital-handling blocks have four functional classifications: the flip-
flop unit, the logic unit, the driver unit, and the pulser unit. The flip-flop
unit is used for static storage, counting, shift register, etc. It has four in-
dependent pulse (clock) inputs and four d-c (logic) inputs. It acts in a logical
sense as a bistable device; it has two possible states. It always remains in
a given state until "flipped" into the opposite state by a suitable signal. This
placing of a flip-flop in a given state is called "setting the circuit." One state
is called the 0 state, the other is the 1 state.

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Figure 4-21   Block Diagram of Data Handler Unit

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The logic unit is a transistor amplifier. The input signal is inverted at the collector output. Depending on the input d-c signal level, the logic circuit is used as either an AND gate or an OR gate.

The driver unit is a two-stage power amplifier designed to furnish a large current.

The pulser unit produces an output pulse for a positive-going input signal. The duration of the output pulse is determined by an r-c time-constant network.

4.19.1 Description of Circuits

The data handler shown in Figure 4-21 is divided into sixteen sub-blocks, each containing groups of digital building blocks. These sub-blocks are described in succession. It is convenient to refer to these blocks by number; each number corresponds to that which appears on the block diagram and to the sequence in which they are described here. For example, 6 refers to the timing circuit sub-block and is the sixth circuit to be described.

1. Control Circuit--This circuit has the following functions:
   a. It resets the following circuits at the beginning of each word.
      1. Parity check
      2. Subword ring counter
      3. Timing
      4. Test word generator
      5. Readout signal generator
      6. Complements counter oscillator

      This reset circuit consists of a one-shot multivibrator driving a low-impedance transistor power amplifier. It is actuated by sig-nal 1 from the master control unit, or by the RESET switch, or by a feedback signal from the subword ring counter.

   b. It resets the following circuits at the beginning of each word and subword.
      1. Output ring counter
      2. Ratio counter
      3. Subword shift and binary complements counter

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This reset circuit is a low-impedance transistor power ampli-
fier. It is driven by pulses from the INITIAL RESET circuit
and the subword shift and the complements binary counter.

c. It contains the TEST WORD SELECTOR control that is a direct
manual selector of the desired test word from the test word
generator.

d. It contains the PRINT CYCLE SELECTOR control that deter-
mines whether the printer functions singly or repetitively during
the test phase with the test word generator. It also controls the
subword ring counter for a single subword printing.

e. It contains the PAYLOAD TAPE CONTROL circuit that is reset
at the end of each word.

The PAYLOAD TAPE CONTROL circuit consists of a single
switching transistor stage activated by a signal from the INITIAL
RESET. After the last subword has been processed, a signal
from the subword ring counter via this switching stage turns the
tape ON, and the processing cycle begins. On a signal from the
master control unit, relays contained in the control circuit re-
move the test-word generator output from the input to the data
handler and switch in the tape output. Another relay (actuated
from the master control unit by a signal corresponding to the
FRONT OF TAPE signal) starts the processing of the word in
the shift register. The RESET switch generates an INITIAL
RESET pulse to initiate the self-test.

f. It contains the relays for disconnecting manual operation circuits
and placing the equipment in automatic operation.

g. It contains the RESET control.

h. It contains a timer that is reset at the beginning of the tape
readout, and that determines how long the stop-start readout
of the tape shall continue.

i. It contains the relays for switching the printer control from the
data handler to the monitor unit.

2. Input and Parity Check Circuits--The input circuit converts the 3-
level return-to-zero binary input signal to a 2-level binary signal
with two separate outputs containing 0's and 1's on separate lines,
and a third output of combined 1's and 0's to form the read-in shift
pulses.

The parity check circuit is a flip-flop that is set to a particular state
before the word enters the input circuit. As the word enters, it is
flipped by the 1's in the word. Parity is correct if the flip-flop ends
up in its initial state.

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The input circuit is composed of a special digital board, standard logic boards, a driver amplifier, and a flip-flop acting as a buffer between the input circuit and the shift register.

3. Read-In Shift Drivers--The read-in shift drivers provide a high-current pulse derived from the incoming word information. This pulse shifts the incoming word information along in the shift register.

4. Output Ring Counter--The output ring counter performs the following functions.

   a. It counts the number of bits in a word entering the shift register.

   b. It performs the binary-to-decimal conversion in conjunction with the subword shift and complements binary counter.

   c. It drives the digital recorder.

   d. It provides the signal to turn on the timing circuit.

   The output ring counter consists of four ring-of-ten counters capable of counting up to 10,000. The bits of a word are counted directly from the input information, and the result is applied directly to the printer. The binary-to-decimal conversion is accomplished by counting (either directly or through a scale factor) the number of pulses required to set to zero the complements binary counter. Ten milliseconds after this counter reaches zero, a command is issued to print, and the output of the readout ring counter is printed by a digital recorder.

5. Shift Register--The purpose of the shift register is temporary storage of information. The means for storage of the binary information is the state of the flip-flop circuit. Digital data in serial form are fed to this unit. A control signal (shift pulse) advances the input information through the circuit. The shift register used in this system is wired for 60 plug-in flip-flop circuits. The circuit is arranged so that the shift pulse advances the incoming information from one flip-flop to the next in one direction, and shifts the word bits out of the register for decoding in the opposite direction. These decoding shift pulses are supplied from an internal clock pulse through the readout drivers.

   Thirteen of the flip-flops of the shift register form the readout section. These are also used to initially store the time subword that is processed first in the subword shift and complements binary counter and in the remainder of the data handler. All successive subwords are shifted into the readout section and handled in the same manner as the time subword.

6. Timing Circuit--The function of the timing circuit is to control the sequencing of the subwords processed in the subword ring counter. The timer consists of a Schmitt trigger driving a 15-μsec pulser, which in turn feeds the subword ring counter through a driver amplifier. For each count, a subword is processed. The timer period of 0.8 second is long enough to permit any one of the subwords to be processed and printed. The timer is reset at the end of each word and there is a 5-second delay between the time it is reset and the first output pulse.

7. Subword Ring Counter--The subword ring counter programs the processing of each subword. This programming consists of presetting the subword shift counter so that the 16-count output will occur when the proper number of bits has been shifted into the readout section of the shift register. In addition, the subword ring counter programs the ratio ring counter to give the appropriate scale factor changes in the binary-to-decimal conversion process.

    The subword ring counter consists of a ring counter in which all the flip-flops are initially 0-set. The first timing pulse sets the flip-flop 1 to a 1 state. The second timing pulse 0-sets flip-flop 1 and 1-sets flip-flop 2. A similar process occurs with timing pulses for the other flip-flops in the subword ring counter. A 15-μsec delay has been introduced between the 0-setting of flip-flop 2 and the 1-setting of flip-flop 3 and all following flip-flops in the ring counter. The purpose of the delay is to ensure that the outputs of the subword ring counter will have a definite change of state after each timing pulse.

8. Digital Recorder--Upon command, the Hewlett-Packard digital recorder prints the decimal number stored in the output ring counter. The print command consists of a relay contact closure that occurs 10 milliseconds after the binary-to-decimal conversion has been completed.

9. Subword Shift and Complements Binary Counter--The subword shift and complements binary counter performs three functions.

    a. It counts the number of readout shift pulses to shift the subwords into the readout section of the shift register and gives a 16-count output to turn off the readout signal generator.

    b. It counts the complement of the binary subword in the readout section of the shift register up to 0 for the binary-to-decimal conversion.

    c. It gives a print command 10 milliseconds after the binary-to-decimal conversion has been performed.

    The subword shift counter consists of an AND gate that is turned on by the counter set circuit and turned off by the 0-set pulse in the control circuit. This AND gate gives a 16-count output signal when 16 pulses have entered the subword shift counter from the readout

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drivers. To shift the proper number of bits of the subword into the shift register readout section, the subword shift counter is preset to a number so that when the number of pulses equal to the number of bits in the subword has entered the counter, there will be a 16-count output. For example, to shift a 6-bit word into the readout section, the subword shift counter is preset to 10, so that the additional six shift pulses will produce the 16-count output.

The binary-to-decimal conversion is performed by 0-setting the subword shift and complements counter and then inserting the complement of the subword stored in the shift register readout section. Pulses from the ratio ring counter increase the complements counter to all 0's. This counter now generates a 10-millisecond pulse, the trailing edge of which gives the PRINT command. The number of pulses required to increase the complements counter to all 0's is one more than the decimal value of the binary number stored in the shift register readout section. These pulses are counted in the output ring counter. To prevent the decimal number from always being greater by 1, an extra pulse from the complements count oscillator not counted on the output ring counter is put into the complements counter at the beginning of each binary to decimal conversion.

The PRINT command is achieved by a relay contact closure, the relay being activated by a driver amplifier operating on a signal from a PRINT COMMAND driver. The latter is 0-set after each subword is processed. The 10-millisecond delay after the complements binary counter has gone to 0 is obtained by using a pulser to drive the print command flip-flops.

10. Complements Count Oscillator--The complements count oscillator provides the pulses used to set the complements binary counter to 0 in the binary-to-decimal conversion. It uses the trailing edge of the shift register readout reset pulse to trigger the 15-μsec EXTRA pulse. The trailing edge of the EXTRA pulse turns on the oscillator after a 150-μsec delay.

The complements count oscillator consists of two pulser boards connected as a 25-kc oscillator, a switching circuit consisting of a flip-flop and logic boards, and a driver output stage.

11. Ratio Ring Counter--The ratio ring counter provides for various scale factors between 1 and 5 in the binary-to-decimal conversion. This is accomplished by dividing the input pulses by any factor from 1 to 5 for either or both of its outputs, depending on its programming from the subword ring counter.

One of the outputs goes to the complements binary counter, the other to the output ring counter.

The ratio ring counter consists of two scale-of-5 ring counters and associated logic circuits. The input pulses come from the complements count oscillator.

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12. <u>Counter Set Circuit</u>--The counter set circuit is used to preset the subword shift and complements binary counter for shifting the subword into the readout section of the shift register. The counter set circuit is programmed by the output of the subword ring counter. Each time a different subword is to be processed, one of the flip-flops in the subword ring counter goes to 0. Fifteen μsec later the next flip-flop goes to 1. The 15-μsec period during which all the flip-flops of the subword ring counter are in the 0 state permits a definite change of state to be noted by the input logic circuits of the counter set circuit. At the end of the 15-μsec period, the desired number is present in the subword shift counter, and an output pulse turns on the readout signal generator.

The counter set circuit consists of four logic OR gates, four pulsers on the output, and an OR gate to form the output pulse.

13. <u>Readout Signal Generator</u>--The readout signal generator provides the pulses that shift the subword into the readout section of the shift register. It is gated on by the output pulse from the counter set circuit and gated off in the 16-count output of the subword shift counter. The readout signal generator consists of two pulsers connected as a 20-kc oscillator and a switching circuit composed of a flip-flop and logic board.

14. <u>Readout Drivers</u>--The six readout driver amplifiers provide a high-current clock pulse used to shift the subwords into the readout section of the shift register. Input to the drivers comes from the readout signal generator. The outputs of the readout drivers go to the shift register clock inputs and the subword shift counter.

15. <u>Frequency 1's Complement Gray-to-Binary Converter</u>--The gray-to-binary converter transforms the complementary gray-coded channel information into binary form as the channel information is shifted into the readout section of the shift register. The converter is normally inhibited by a 10-volt signal from the subword ring counter until this channel information is ready to be shifted into the readout section. The gray-to-binary converter consists of logic circuits that compare the most significant bits with successive bits to perform the gray-to-binary conversion.

16. <u>Test-Word Generator</u>--The test-word generator is capable of producing three types of words--alternate 1's and 0's, all 0's, or all 1's. These words simulate the 3-level return-to-zero input from the tape for testing of the data handler.

4.19.2 <u>Sequence of Operations</u>

4.19.2.1 <u>Process of Typical Word.</u> Figure 4-22 shows the timing diagram for processing a typical word. In the following description, a number in

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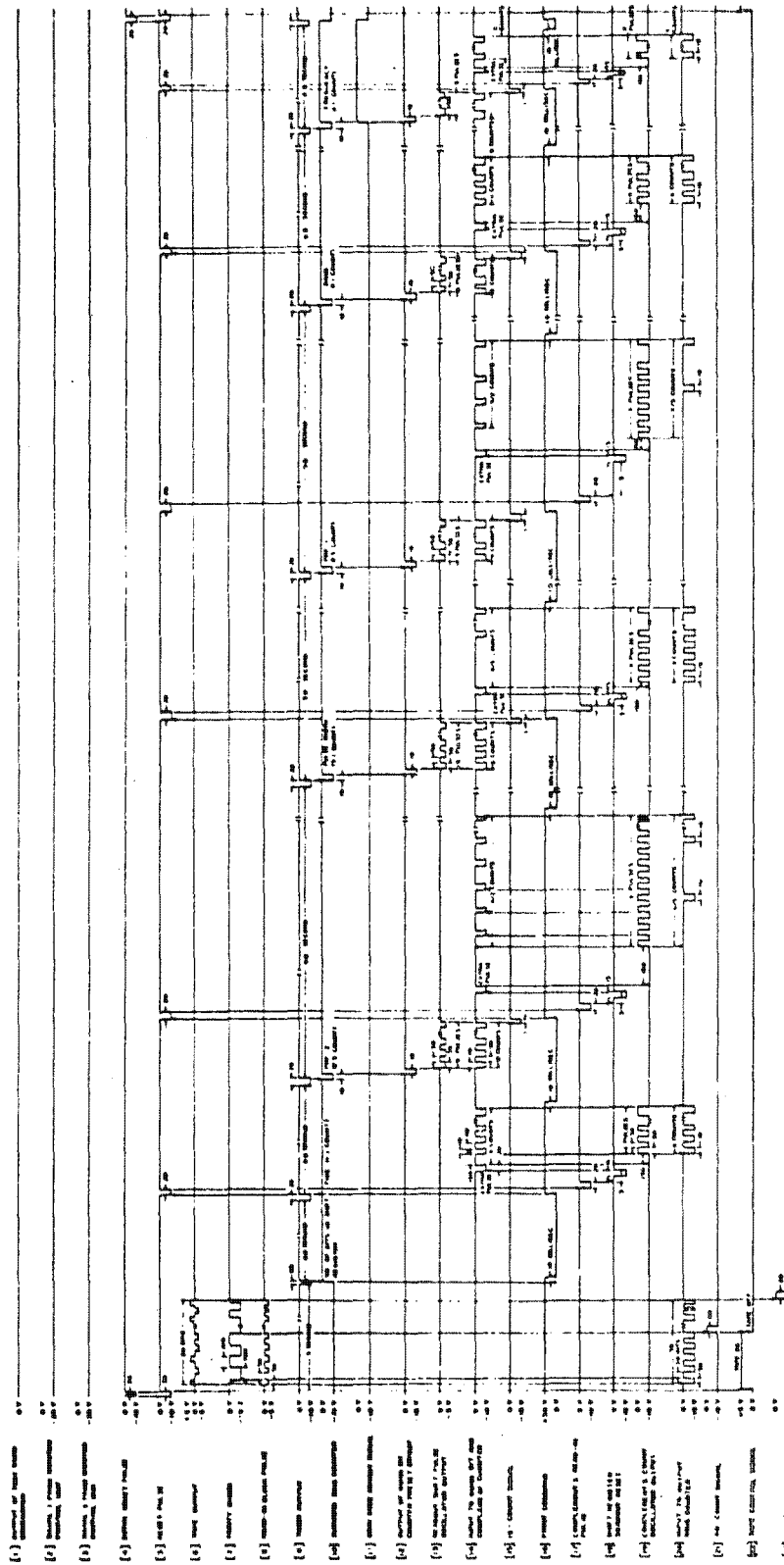Figure 4-22 Timing Diagram of Typical Word

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brackets [1], refers to lines on the timing diagram and a number in a circle (1) refers to the data handler circuits in Figure 4-21. Data processing is described in the following steps.

1. At the end of the previous word process, all circuits have been initially reset (1) [4].

2. A 3-level ±6 volt return-to-zero 19-kc word [6] enters the data handler via the control circuits (1); then it goes to the input and parity check (2).

3. In the input and parity check, the word is:

   a. Converted to a 2-level binary signal with 1's and 0's separated out of the word

   b. The 1's and 0's are combined in a single line to form read-in unidirectional clock pulses [8].

   c. The number of 1's in the word is counted by the parity check.

4. The read-in clock pulses [8] shift the 1's and 0's along the shift register (5) via the read-in drivers (3). The read-in clock pulses [8] are counted in the output ring counter (4) [20].

5. After 40 bits have entered the shift register (5), the output ring counter (4) gives a Tape Stop Count signal [21] (-10 to 0 volts, 80-μsec pulse), the leading edge of which gives the tape a command to stop [22]. As the tape coasts to a stop, the remaining bits enter the shift register.

6. Five seconds after the initial reset pulse, the timing circuit (6) gives its first pulse [9]. The timing pulses are 15-μsec wide and 0 to -10 volts in amplitude. There is an 0.8-second interval between successive timing pulses.

7. The first timing pulse 1 sets flip-flop 1 of the subword ring counter (7) [10].

8. Ten milliseconds after flip-flop 1 has been 1-set, a print command is issued 16, and the number of bits shifted into the shift register 5 as recorded on the output ring counter (4) [20] is printed by the Hewlett-Packard digital recorder (8).

9. The second timing pulse (9) 0-sets flip-flop 1 and 2-sets flip-flop 2 (7)

10. As flip-flop 2 is a 1-set, it triggers the reset pulse (1) [5] and programs the ratio ring counter (11) for a 1:1 count output.

11. The trailing edge of the reset pulse (1) [5] triggers the complements read-in pulse [17], which reads the complement of the time information (located in the shift register readout section (5)) into the subword shift and complements binary counter (9).

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12. The trailing edge of the complements read-in pulse [17], after a 30-μsec delay, triggers the shift register readout reset pulse [18], which 0-sets the readout section (5).

13. The trailing edge of the readout reset pulse [18] triggers the extra pulse [14] (9).

14. The trailing edge of the extra pulse [14], after a 150-μsec delay, turns on the complements counter oscillator (10) [19]. The output of this oscillator that is fed into the ratio ring counter (9) has programmed the ratio ring counter (11) to give a 1:1 count on its outputs--that is, one count in the subword shift and complements binary counter (9) [14] for one count in the output ring counter (4) [20].

15. The trailing edge of the last pulse required to count the complements binary counter (9) to 0 [14] turns off the complements count oscillator (10) [20], and after a 10-millisecond delay it gives a print command [16].

16. The print command [16] causes the printer (8) to print the number stored in the output ring counter (4) [20].

17. The third timing pulse 0-sets flip-flop 2 (7) [20]. Fifteen μsec after flip-flop 2 is 0-set, flip-flop 3 (7) is 1-set (10).

18. When flip-flop 3 (7) is 1-set (10), the ratio ring counter (11) is programmed to give a 2:5 count on its output--that is, two counts in the complements binary counter (9) [14] for five counts in the output ring counter (4) [20]. At the same time the subword shift counter is preset (12) to 7.

19. The counter set circuit (12) also gives a 15-μsec pulse [12], the trailing edge of which turns on the readout signal generator (13) [13].

20. The readout signal generator (13) shifts the nine bits of PRF-2 information into the shift register readout section (5) via the readout drivers [14]. The output of the readout drivers [14] is also fed into the subword shift counter (9) [14]. When nine pulses have been fed into the subword shift counter, the counter gives a 16-count output (9) [15].

21. The leading edge of the 16-count output (9) [15] turns off the readout signal generator (13), and the trailing edge triggers the reset pulse (1) [5].

22. The trailing edge of the reset pulse [5] initiates the complements read-in pulse [17] which reads the complement of the binary word in the shift register readout section (5) into the complements binary counter (9).

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23. After a 30-μsec delay, the trailing edge of the reset pulse [5] triggers the shift register readout reset pulse [18], which in turn 0-sets the shift register readout (5).

24. The trailing edge of the shift register readout reset [18] triggers the EXTRA pulse into the complements binary counter (9) [14].

25. After a 150-μsec delay, the trailing edge of the EXTRA pulse turns on the complements counter oscillator (10) [19], the output of which goes to the ratio ring counter (11) and then to the output ring counter (4) [20] and the complements binary counter (9) [14].

26. When the complements binary counter (9) [14] has been counted to all 0's, the complements count oscillator (10) [19] is turned off, and after a 10-millisecond delay a print command (9) [16] is issued. The counts registered in the output ring counter (4) are printed (8).

27. The data processing cycle is repetitive for the remaining parts of the word. The only variation is the number preset in the subword shift counter (9) and the ratio programmed on the ratio ring counter (11) (1:2 for pulse-width, 2:5 for PRF-2, 1:1 for all other parts of the word).

28. When the last subword (channel) has been processed and printed, the timing pulse (6) [9] 0-sets the last flip-flop in the subword ring counter (7) [10].

29. When this flip-flop (7) [10] is 0-set, it triggers the initial reset pulse (1) [4]. The trailing edge of the initial reset pulse (1) [4] triggers the tape command (1) [22], and the whole process begins again on the next word read in from the tape.

30. The data handler continues to process the words on the tape in stop-start operation until a signal from a variable time delay preset at the beginning of the tape readout stops the data handling process.

4.19.2.2 Self-Test Mode. In the self-test mode of operation, the word process is the same as that of a typical word except that the 68-count signal [23] from the output ring counter (4) turns off the test-word generator (16).

Processing the First Word--Figure 4-23 is the timing diagram for the processing of the first word. The data handler is normally in the self-test mode of operation. To begin processing words from the tape, signal 1 from the master control unit [2] to the control circuits (1) turns off the test-word generator (16) and connects the output of the tape to the input and parity check (2). Signal 1 from the master control unit [2] holds the data

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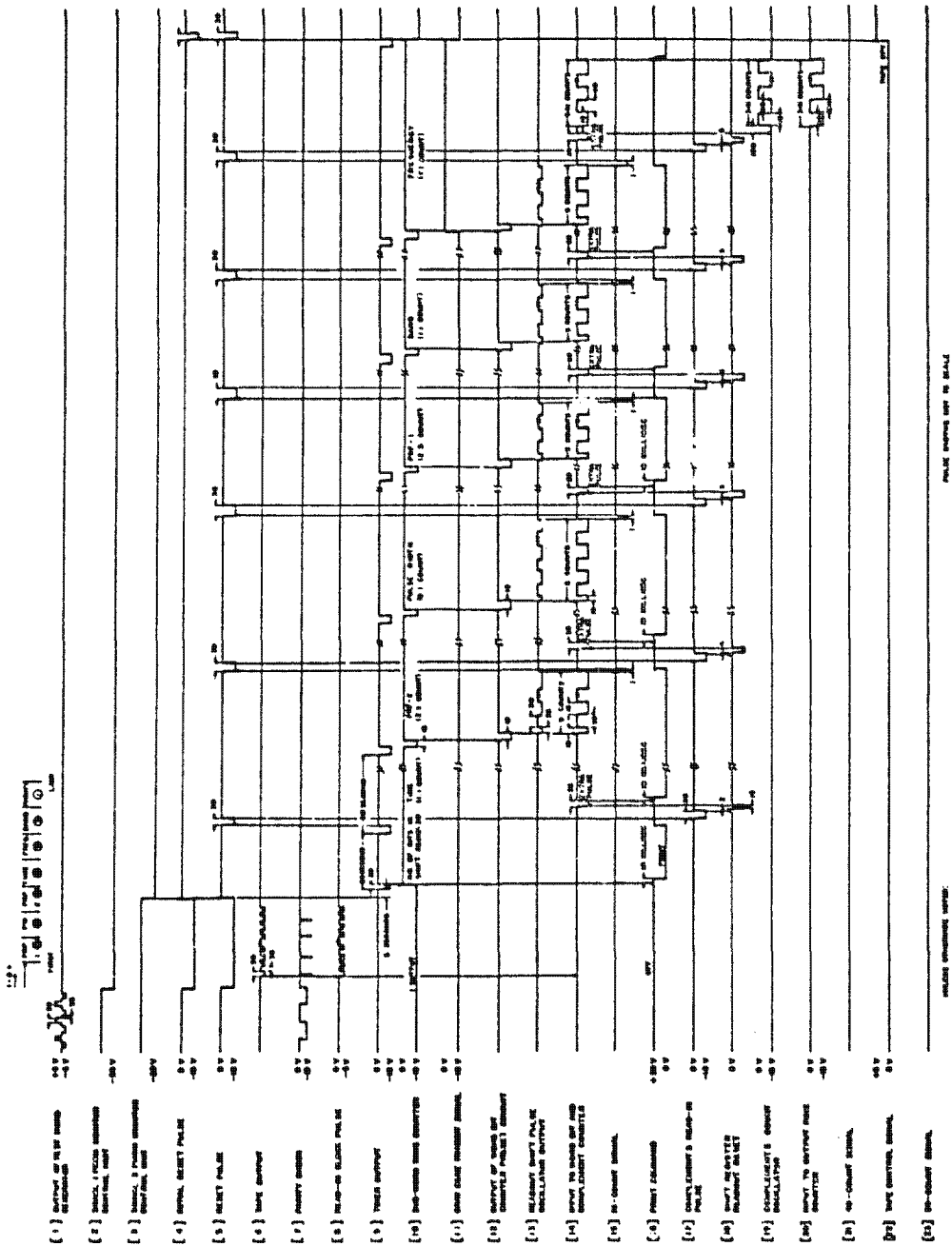
Figure 4-23 Timing Diagram of First Word

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handler in the initial reset condition [4], which permits the words from the tape to pass through the shift register (5) without being processed. When the forward end of the tape is reached, the first word on the tape (the all zero word) remains in the shift register (5); signal 2 from the master control unit [3] releases the initial reset and permits this word to be processed. From this point on, the all zero word is processed in the same manner as the typical word.

4.20 JUNCTION BOX

The junction box serves as an access facility to the various interconnecting cables between the checkout equipment and the payload equipment. All power and signal cables except for RF feeds are thus made accessible for measurement and monitoring when such is necessary. A number of test points are provided in addition to tie points thereby allowing access to many signal terminals without removing the junction box.

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Ltr, DDC(DDC-IR), 1 Jul 64, Clarification of Limited Access Reports

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3. This indorsement contains no classified information.

FOR THE COMMANDER

Kenneth D. Medlow, Jr., 2dLt, USAF

KENNETH E. INGRAM   7 Atch
Major, USAF   n/c
Chief, Systems Security
and Classification Division

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