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PHOTOGRAPHIC SYSTEM REFERENCE HANDBOOK FOR GAMBIT RECONNAISSANCE SYSTEM WITH EXTENDED ALTITUDE CAPABILITY (EAC)

VOLUME 5

Prepared by

BIF-008

Under Contract [redacted]

25X1

Approved by:

[redacted]

1 July 1980

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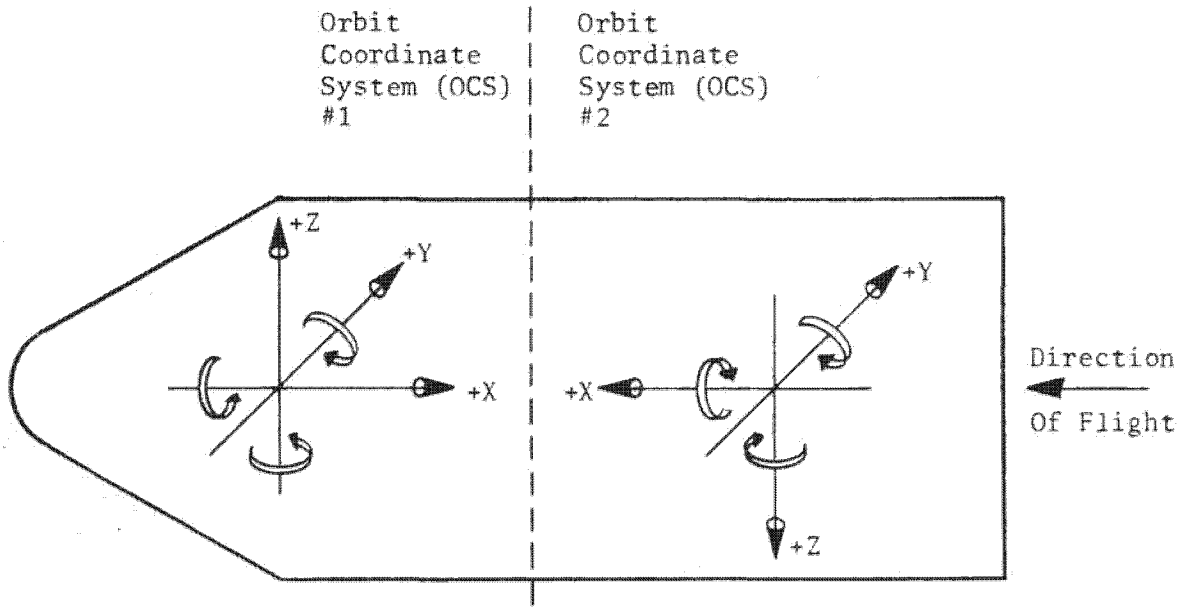

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9.0 COMMAND SUBSYSTEM

The command subsystem consists of two separate systems; the extended command subsystem (ECS)* and the minimal command subsystem (MCS)*. The ECS and MCS accept command messages from the remote tracking stations (RTS's) described in Part 4, Section 7, verify and decode the information, and either generate immediate commands, or store the data for later execution. Simply stated, command execution involves generation of a pulse on a single line (or pulses on several lines for certain types of commands) with controlled rise and fall times, pulse width, and amplitude.

Commands for the Photographic Payload Section/Dual Platen Extended Altitude Capability (PPS/DP EAC) are received either by the command processor (CP), or the initiator electronics unit (IEU) which perform the following functions:

a. Command Transfer

b. Logic Operations (if required)

c. Command Transfer Monitoring

The CP receives all non-pyrotechnic related commands while all commands which require actuation of pyrotechnic devices are handled by the IEU. The CP is described in Section 9.7. Further information concerning the IEU is provided in Part 3, Section 7.

*The ECS and MCS are located in the Satellite Control Section of the Photographic Satellite Vehicle and are manufactured by General Electric Aerospace Electronic Systems Division (GE AESD).

In normal operation, the ECS is treated as the primary subsystem for commanding. The MCS is used only as a backup for the ECS, to provide an additional means of commanding those functions critical to mission termination and recovery. The relationship of the ECS, MCS, the RTS communication links and the PPS/DP EAC units is shown in the block diagram of Figure 3.9-1.

9.1 Vehicle-Ground Communications Link

Communication with the vehicle is provided by two separate links. Link 1 consists of two redundant channels, space ground link system 1 (SGLS 1) and space ground link system 2 (SGLS 2). Link 2 is a backup command link employing an ultra high frequency (UHF) receiver in the SCS (see Figure 3.9-2).

The SGLS equipment in the vehicle provides the tracking, telemetry, and command capabilities for the vehicle. The SGLS transponder contains the radio frequency (RF) receiver [redacted] for tracking and command purposes, and the RF transmitter [redacted] for tracking and telemetry requirements. The UHF backup command link includes only a receiver, and therefore cannot serve for tracking or telemetry purposes. Each remote tracking station has both S-band (SGLS) and UHF communications equipment for support of the Gambit mission. 25X1

The telemetry portion of the vehicle communications is described in Part 3, Section 10. Tracking is the responsibility of the SCS associate contractor, Lockheed Missiles and Space Company (LMSC), and will not be discussed here.

9.2 Command Types

Two basic operational command types, real-time commands (RTC's) and stored program commands (SPC's), are available through the ECS and MCS. Real-time commands are executed upon receipt and verification, and are used to provide ECS/MCS control as well as commanding other vehicle functions. No RTCs are processed

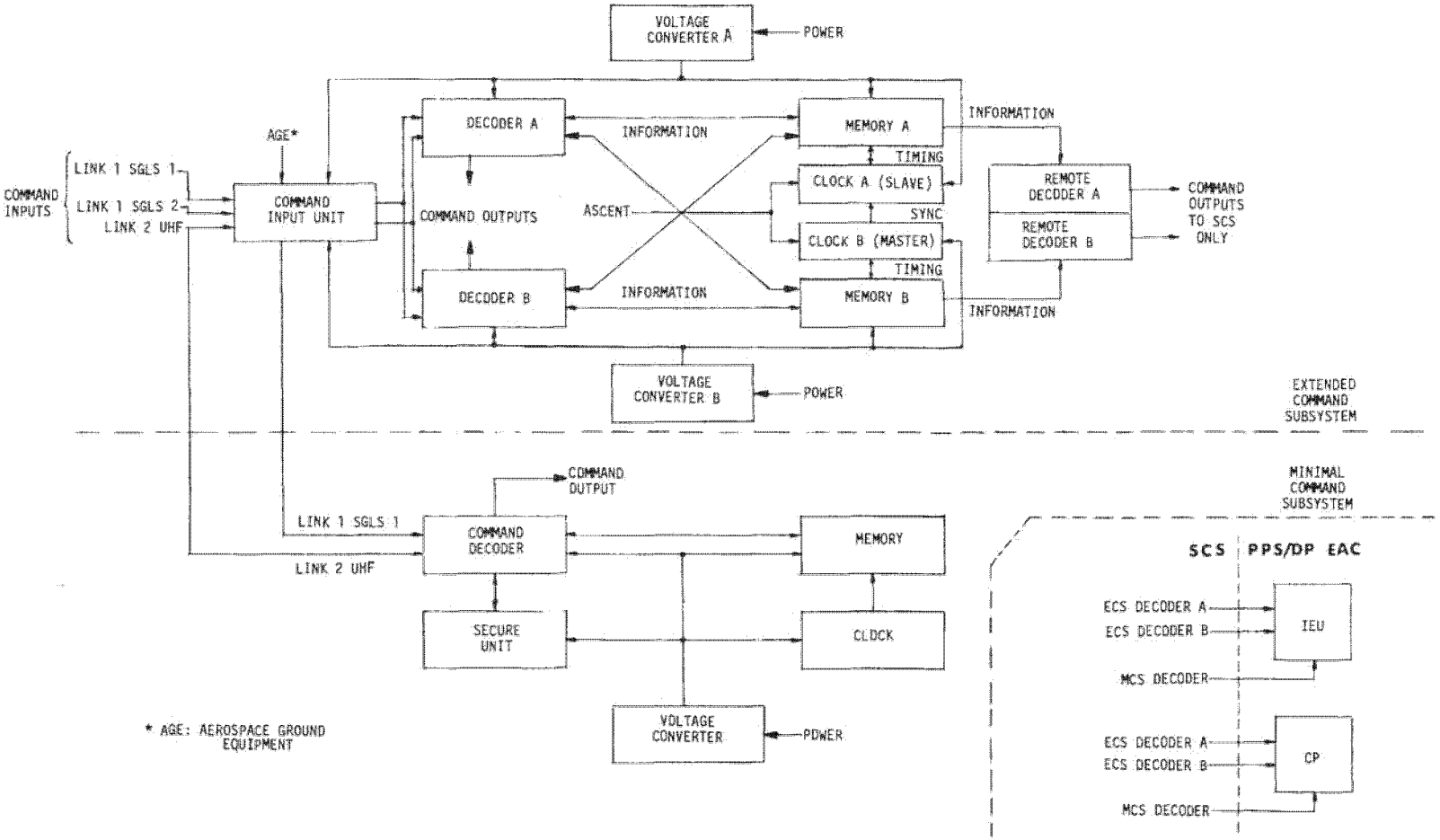


Figure 3.9-1. Command Subsystem Block Diagram

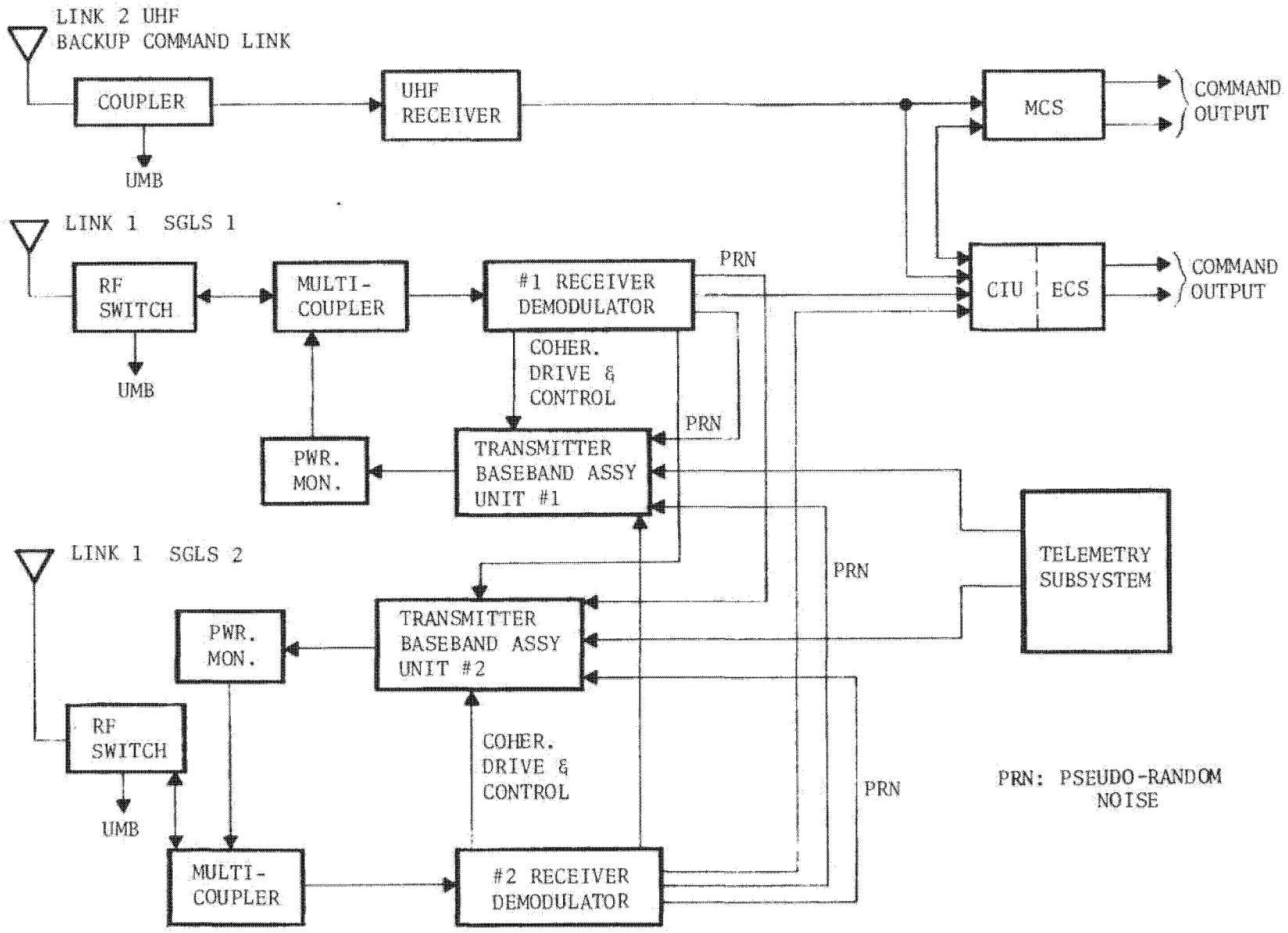


Figure 3.9-2. Vehicle Communications Block Diagram

by the PPS/DP EAC. Stored program commands are received and stored in memory upon verification and proper secure word* transmission procedures. These SPC's are read out of memory and executed 0.2 second after the command system clock matches the time code portion of the command. Thus, SPC commands can be given at a maximum rate of one every 0.2 second (the command system clock code increment).

Stored program commands are divided into three subgroups, each with distinct characteristics. Normal stored program commands (NSPC's) behave much as real-time commands in terms of command execution. Protected stored program commands (PSPC's) provide additional security in that they must be given in pairs for execution, the second following the first by 0.2 second. PSPC's are also protected against inadvertent commanding due to hardware failures by providing switched, isolated output and return lines for each command pulse.

Variable stored program commands (VSPC's), like NSPC's, occur singly. When executed in the command period following the time label match, they provide an output on one or the other of two discrete lines for each bit in the variable portion of the command word depending on the logic state of the bit. VSPC commands also provide one additional discrete output (the "implicit" bit) which indicates that the VSPC is being executed. This output is treated as a command input in the PPS/DP EAC.

Several other command types are used by the command subsystem to control the ECS and MCS and do not affect the PPS/DP EAC. However, two special commands, secure word real-time commands (SWRTC 1 and SWRTC 2), are available through the MCS which do control functions within the PPS/DP EAC. SWRTC 1 is used exclusively to enable the recovery of SRV 1, and SWRTC 2 to enable the recovery of SRV 1 and/or SRV 2 by MCS termination commands (ARM/TRANSFER/SEPARATE).

*Secure words are special command words used to gain access to the command subsystem, and to prevent unauthorized or accidental commands from being accepted.

The actual enabling circuitry is located in the initiator electronics unit. Execution of SWRTC 1 or 2 does not affect processing of termination commands from the ECS.

9.3 Command Bit Structure

Stored program commands transmitted to either the MCS or ECS consist of 39 bits, with bit 1 the least significant bit (LSB). For ECS command words, the first 22 bits represent a time tag; bit 23 is a time parity bit providing even parity for the time label (even number of 1's including parity); bits 24 through 38 are command and function identification bits; bit 39 is the even parity bit for the entire word (Figure 3.9-3).

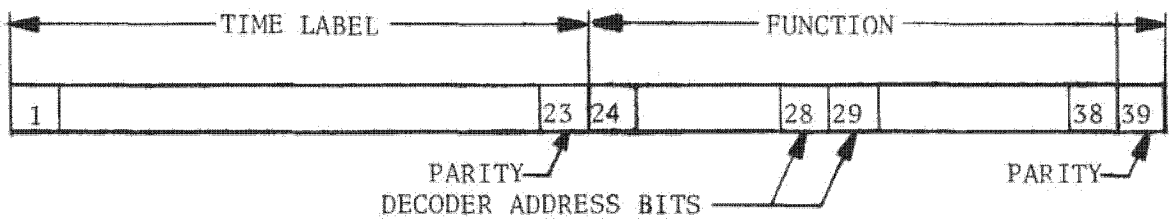


Figure 3.9-3. ECS Command Bit Structure

In the MCS command bit structure (Figure 3.9-4), bits 1 through 21 are the time code bits with bit 22 always set to 1; bit 23 is even parity for the time label; bits 24 through 28 are always zero and the command function is contained in bits 29 through 38; bit 39 is even parity for the entire command.

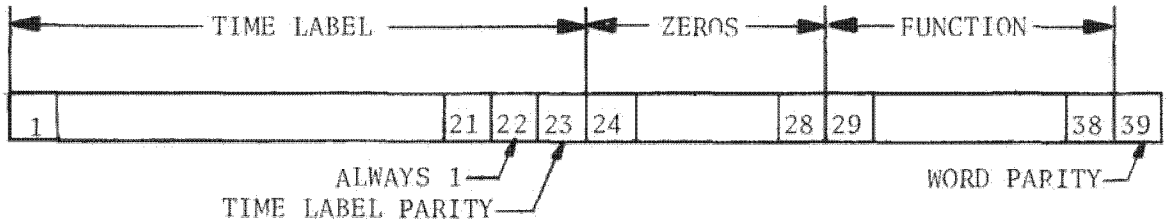


Figure 3.9-4. MCS Command Bit Structure

The command numbers assigned to stored program commands include a prefix to indicate the type of command; "N" for NSPC, "P" for PSPC, and "V" for VSPC. An "M" precedes the entire code for MCS commands. The octal representation of the function part of the command follows the prefix. This octal code consists of 5 digits which correspond to the conversion of bits 24 through 38 from left to right in groups of three. For example, a command expressed in octal as 01754 appears in binary as 000 001 111 101 100 (see Figure 3.9-5).

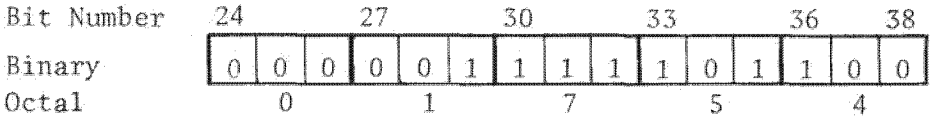


Figure 3.9-5. Binary-to-Octal Code Conversion

Each NSPC and PSPC has a unique octal code assigned to it. The command system identifies it by the bit pattern (bits 24-28) and produces outputs on the appropriate command lines.

VSPC's are different in that they are identified by a few of the 15 function bits and the remaining bits can each be used to provide one of two discrete outputs by assigning either a "1" or a "0" to each variable bit. The VSPC octal codes are identified by placing a "V" before the octal code. They are further identified by placing a decimal number ahead of the "V" to tell how many variable bits are available in the word. VSPC's available to the PPS/DP EAC from the ECS are 14V, 13V, 10V and 4V words. Only one variable command, a 6V word, is available to the PPS/DP EAC from the MCS.

To facilitate discussion of the VSPC formats, the letter b is used to represent a variable binary bit and the letters W, X, Y, and Z are used to represent the four variable octal code digits. This convention is shown in Figure 3.9-6.

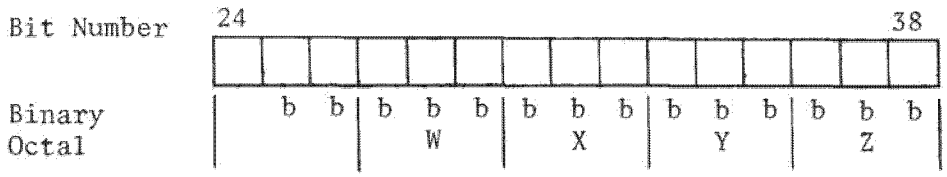


Figure 3.9-6. Variable Word Octal Representation

For octal positions where only one or two of the three bits are variable, an octal equivalent of the bit pattern resulting from placing the variable bit(s) in the 0 state expresses the fixed bit(s) and is followed by one or two b's depending on the number of variable bits in that octal position.

There are three large VSPC's available from the ECS. They are the 14V WORD, the 13V WORD and the 10V WORD. The bit patterns of the large VSPC's are shown in Figure 3.9-7.

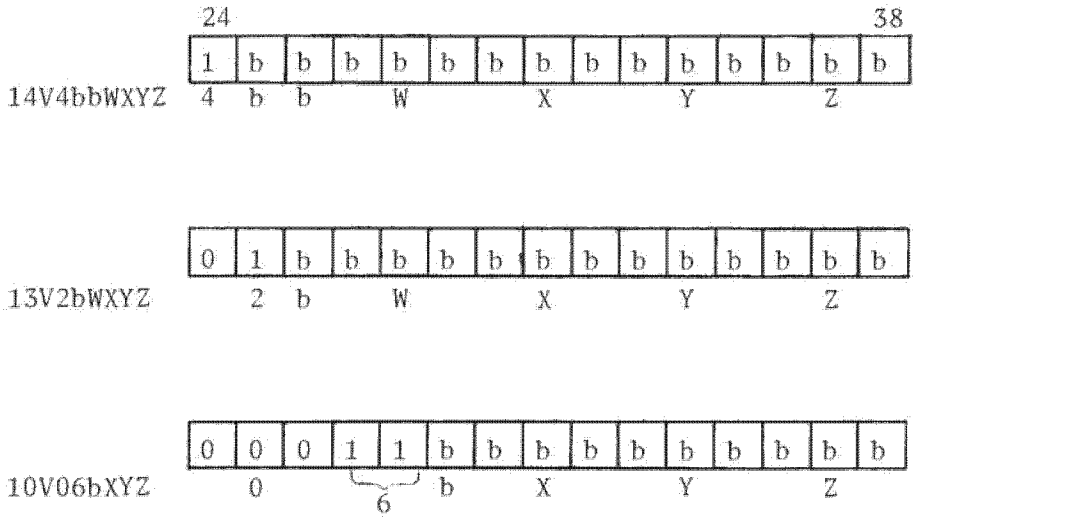


Figure 3.9-7. ECS 14V, 13V, and 10V VSPC Octal Codes

Examples of other variable words available to the PPS/DP EAC are 4V0172bZ, 4V0152bZ and M6V002YZ (MCS command). Additional VSPC's in the ECS and MCS are assigned to the satellite control section (SCS).

In addition to the two outputs available for each variable bit of a VSPC, there is the implicit bit which furnishes one additional output when the variable bit command is executed.

9.3.1 Decoder Selection

The stored program commands in the ECS are executed in either, or both, of the A and B decoders (except for those designated in the remote decoder*). The three large VSPC's (14V 13V, and 10V) are executed simultaneously from both decoders, unless a second SPC from the opposite memory is to be executed simultaneously, in which case each command will be executed by the decoder associated with its programmable memory unit (PMU).

All other stored program commands use bits 28 and 29 to designate the decoder(s) that will decode and execute the command according to Table 3.9-1.

*No PPS/DP EAC commands are executed in the remote decoder.

TABLE 3.9-1

ECS SPC DECODER SELECTION

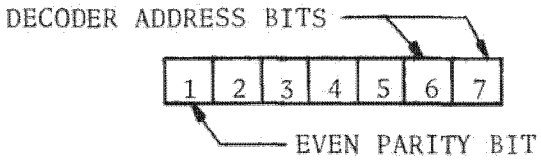
	Bit 28	Bit 29	Second Octal Digit
Decoder A	1	0	2
Decoder B	0	1	1
Both Decoders	1	1	3

Thus, N02754 will be executed by decoder A, N01754 will be executed by decoder B and N03754 will be executed by both decoders simultaneously.

The MCS includes only one decoder and therefore does not reserve bits for decoder selection.

9.3.2 RTC Bit Structure

Both ECS and MCS real-time commands consist of 7 bits: the first bit representing even parity, bits 2 through 5 for command identification and the last two bits (6 and 7) for the decoder address (ECS commands only). RTC's cannot be executed by both decoders simultaneously. Figure 3.9-8 illustrates the bit structure of all real-time commands.



	Bit 6	Bit 7
Decoder A	0	0
	1	0
Decoder B	0	1
	1	1

Figure 3.9-8. RTC Bit Structure

An octal code representing bits 2 through 7 is used to designate the RTC as was done for stored program commands. The codes are preceded by an "R" for ECS RTC's, and an "MR" for MCS RTC's. A second type of real-time command secure word real-time commands, exists only in the MCS. These have been described previously in Section 9.2.

9.4 ECS Simultaneous Commanding

Simultaneous commanding (executing a different command in each decoder during the same command time period) is possible with ECS stored program commands assigned to the PPS/DP EAC within certain guidelines:

a. A 14V, 13V or 10V command will be executed by both decoders at the same time unless the other programmable memory unit (PMU) supplies another VSPC or an NSPC to be executed at the same time. In such a case, each decoder will execute the command which came from its associated PMU.

b. One NSPC, 4V or 6V command can be executed individually out of one decoder, or out of both decoders simultaneously. Two different commands of the NSPC, 6V, or 4V type may be executed at the same time; one out of each decoder.

c. One PSPC can be executed individually by one decoder, or out of both decoders simultaneously. A different PSPC can be executed by each decoder simultaneously. However, a PSPC should not be executed by one decoder while the other decoder is executing a non PSPC type command.

d. Real-time commands may be executed out of only one decoder at a time and the other decoder cannot be used simultaneously. If the decoders are in the real-time state and a stored program command time label indicates an NSPC, PSPC, or VSPC is due for execution, the RTC will be inhibited and the SPC will be executed.

Table 3.9-2 summarizes the possible command combinations. Additional restrictions, imposed by the commanded hardware rather than limitations of the ECS, are listed below:

a. A function should not be commanded to two different states at the same time; i.e., DOOR OPEN from decoder A, and DOOR CLOSE from decoder B. The result of such commanding will be ambiguous.

b. Film drive ON/OFF commands and platen PLUS/MINUS/STOP commands should be issued from the same PMU to preclude an ECS clock separation situation from affecting the order of issuance; i.e., film motion which is started by a command from PMU A should also be stopped by a command from PMU A. Such a procedure will prevent film waste in the event of a problem with PMU B.

c. Termination sequence commands should be issued from both decoders simultaneously.

Many other conflicts and interlocks exist in the ECS, but are beyond the scope of this document.

9.5 Timing Signals and Command Pulse Characteristics

The ECS incorporates two independent clock circuits; the master clock (B), and the slave clock (A). In addition to internal ECS functions, these provide three timing signals (A, B, and C) to the SCS and PPS/DP EAC. Timing signal C from clock A is designated C1, and from clock B is designated C2. C1 and C2 are delivered on separate lines, only one of which is active at any given time.

The timing signals consist of a series of positive pulses having a peak amplitude between 4.7 volts and 7.35 volts and a quiescent level of 0.30 volt. The

TABLE 3.9-2

POSSIBLE SIMULTANEOUS DECODER EXECUTIONS IN THE ECS

DECODER A	DECODER B
14V-Identical-14V	
14V-Different-14V*	
14V	13V*
14V	10V*
14V	6V*
14V	4V*
14V	NSPC*

DECODER A	DECODER B
13V	14V*
13V-Identical-13V	
13V-Different-13V*	
13V	10V*
13V	6V*
13V	4V*
13V	NSPC*

DECODER A	DECODER B
10V	14V*
10V	13V*
10V-Identical-10V	
10V-Different-10V*	
10V	6V*
10V	4V*
10V	NSPC*

DECODER A	DECODER B
6V	14V*
6V	13V*
6V	10V*
6V-Identical-	6V
6V-Different-	6V
6V	4V
6V	NSPC
6V	Nothing

DECODER A	DECODER B
4V	14V*
4V	13V*
4V	10V*
4V	6V
4V-Identical-4V	
4V-Different-4V	
4V	NSPC
4V	Nothing

DECODER A	DECODER B
NSPC	14V*
NSPC	13V*
NSPC	10V*
NSPC	6V
NSPC	4V
NSPC-Identical-NSPC	
NSPC-Different-NSPC	
NSPC	Nothing

DECODER A	DECODER B
Nothing	6V
Nothing	4V
Nothing	NSPC
Nothing	PSPC
Nothing	RTC

DECODER A	DECODER B
PSPC-Identical-PSPC	
PSPC-Different-PSPC	
PSPC	Nothing

DECODER A	DECODER B
RTC	Nothing

*To get the combination shown, commands will have to be issued from the associated PMU.

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pulse duration is nominally 1.0 millisecond with rise and fall times less than 20 μsec. Since all three are derived from the basic ECS clock, they are synchronized to each other.

Figure 3.9-9 presents a timing diagram for signals A, B, and C. Timing signal A is a time label consisting of a synchronization pulse followed by a 24-bit time code representing the ECS clock time associated with that synchronization pulse.* The presence of a pulse represents a binary ONE and the absence of a pulse a binary ZERO. The code is presented every 0.2 second at the rate of 500 pps with the least significant bit first. The first 22 bits of the time code serve to accumulate time in 0.2-second increments to a maximum of 838,860.6 seconds and then reset (bits 23 and 24 are ignored within the PPS/DP EAC).

Timing signal B is a 500-pps wave train. Timing signal C is a 20-pps wave train. To prevent loading problems, the timing signal interfaces between the SCS and the PPS/DP EAC are controlled by interface agreements among the associate contractors. Each signal is transformer coupled to circuitry within the PPS/DP EAC (in the 9 and 5 camera electronics assemblies) to meet these requirements (see Figures 3.9-10 and 3.9-11).

9.5.1 Command Pulse Characteristics

Like timing signal characteristics, the command pulse characteristics at the PPS/SCS interface, and loading within the PPS/DP EAC, are also controlled by agreement among the various associates. The nominal command pulse amplitude is 31.5 volts with rise and fall times between 2 and 5 milliseconds. The pulse duration,

*Time relationship: The leading edge of the ECS command pulse lags the leading edge of the synchronization pulse of the associated time label by 190 to 210 milliseconds.

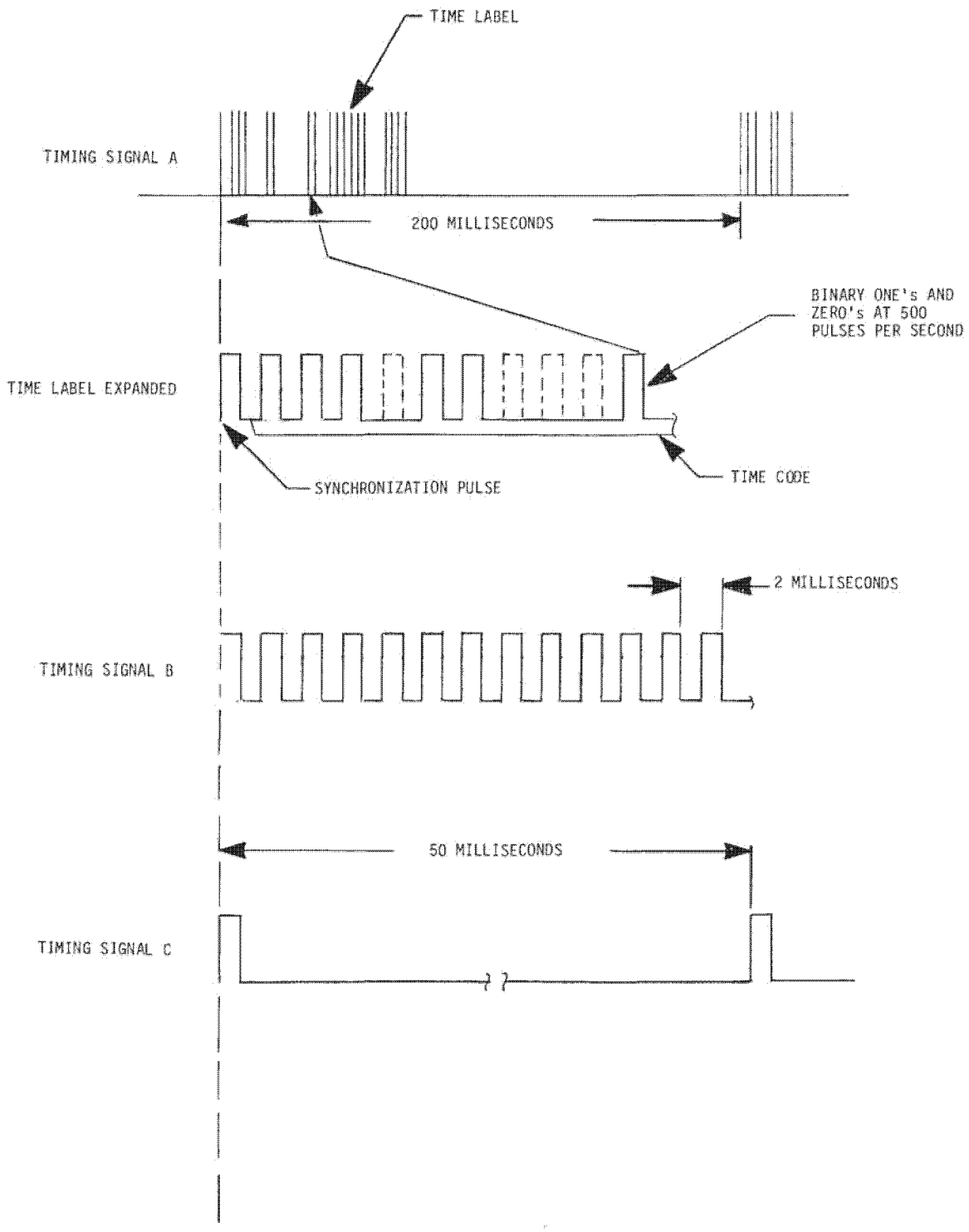

Figure 3.9-9. Timing Signals

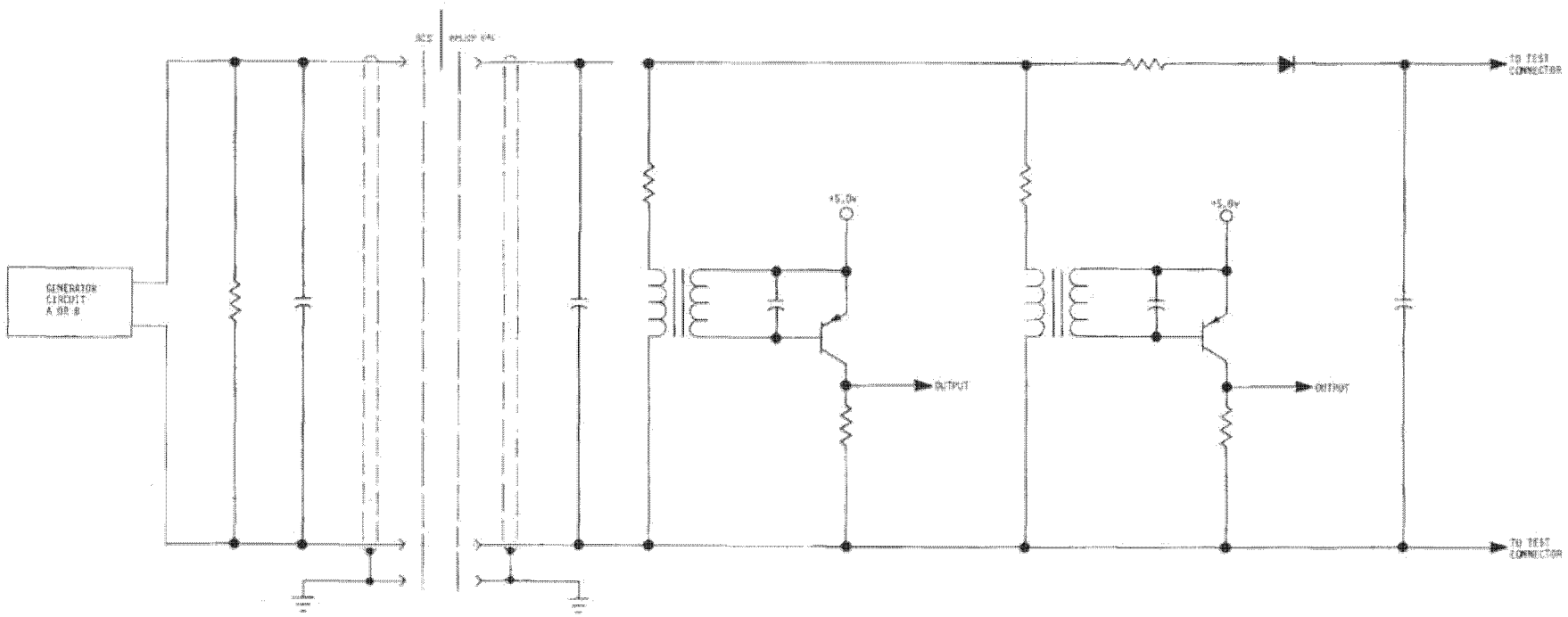

Figure 3.9-10. Timing Signal Circuit A or B Interface

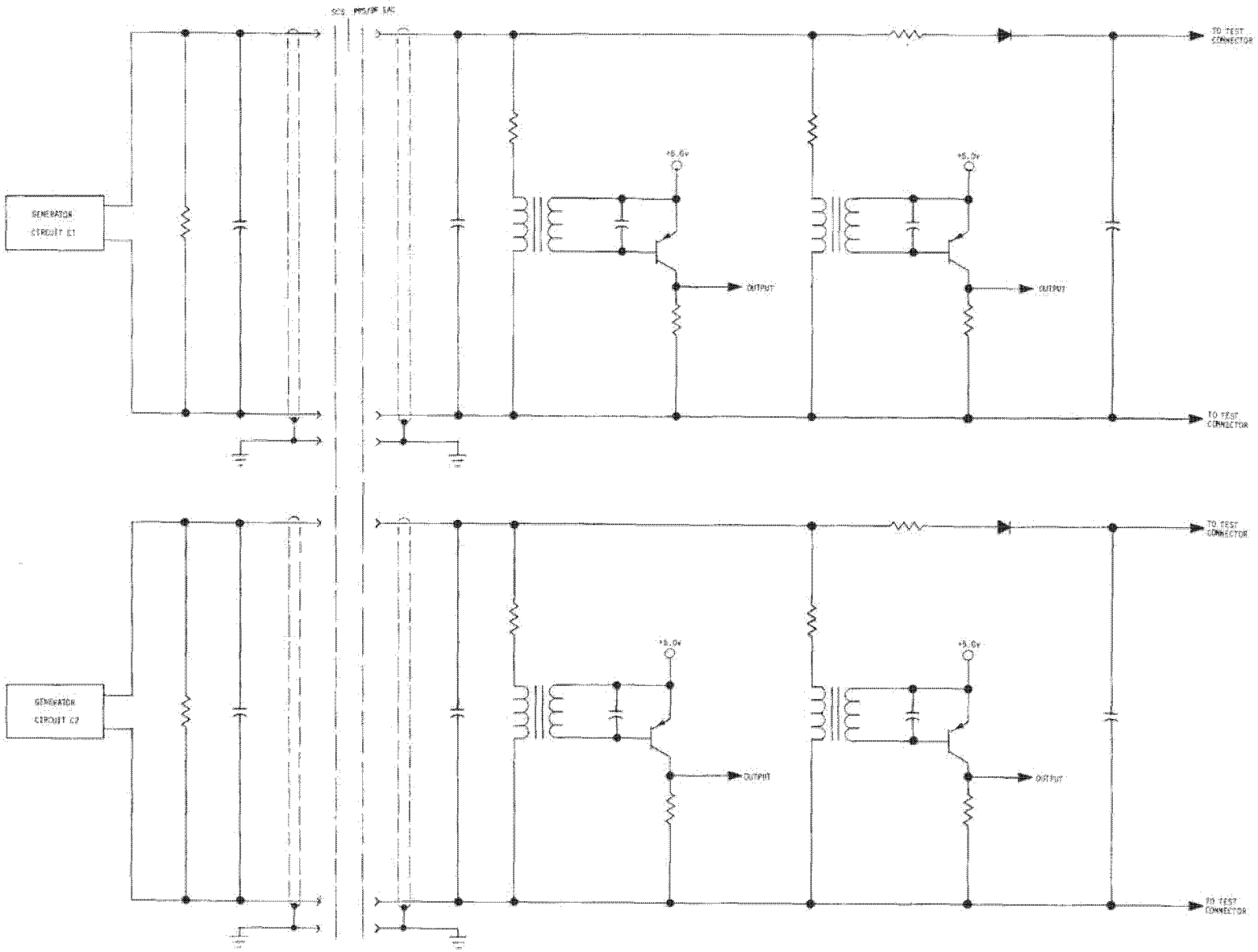

Figure 3.9-11. Timing Signal C Circuit Interface

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defined as the total time the pulse amplitude is above 50 percent of its peak level, is between 100 and 110 milliseconds for ECS commands, and 90 and 180 milliseconds for commands executed by the MCS.

Each decoder can execute one stored command every 0.2 second. Continuously transmitted real-time commands for focus adjustment have a maximum time between the trailing edge of one pulse and the leading edge of the following pulse of 100 ms when measured at the 50 percent level of peak amplitude.

When executing commands out of each ECS decoder during the same command period, or when executing a VSPC (several discrete outputs), the command pulses will be almost simultaneous. All VSPC pulses from one decoder occur within 1.5 ms of each other. Command pulses from opposite decoders, initiated by a single PMU readout, occur within 3.4 ms of each other. When the slave clock is synchronized to the master, command pulses from opposite decoders and PMU's are displaced in time no more than 7.3 ms. Tight control over the command timing ensures that the commanded functions will operate as expected when the orginal command message was assembled.

9.6 Extended Command Subsystem/Minimal Command Subsystem Overview

The ECS and MCS are manufactured by General Electric Aerospace Electronic Systems Division and are installed by LMSC in the satellite control section of the PSV. The following information is included for reference purposes only and is not guaranteed to be current. The source used is a training manual published by GE AESD.* Only those points considered pertinent to the understanding of PPS/DP EAC operation are discussed. For complete information, refer to publications from GE AESD and/or LMSC.

*Reference BIF-008-W-N-200061-IH-73: Training Manual for MOD IV Low Power Command System.

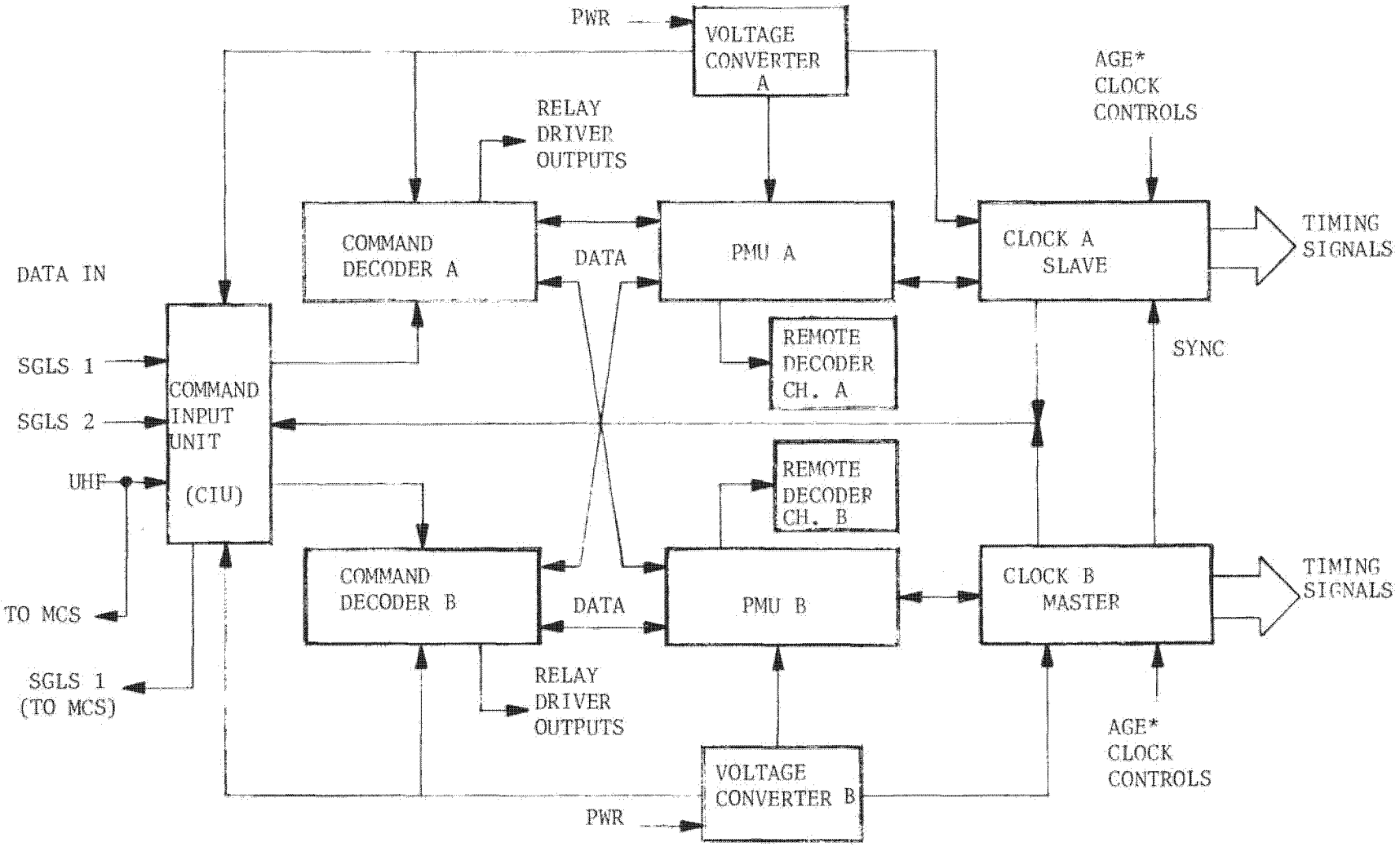
9.6.1 Extended Command Subsystem

The ECS, in response to signals from the ground communications link, accepts, verifies, and decodes information, and either generates immediate command outputs or stores the commands for later execution. The ECS is comprised of a single command input unit (CIU), and redundant voltage converters, clocks, programmable memory units, and synchronous decoders, and has an additional remote decoder (not employed for PPS/DP EAC functions) which processes PSPC's only (see Figure 3.9-12).

9.6.1.1 Command Input Unit. The command input unit gates data from link 1 (SGLS 1 and SGLS 2), or link 2 (UHF link), buffers the data and outputs it to the ECS decoders. SGLS 1 data is supplied to ECS decoders A and B, and also to the MCS. SGLS 2 data is provided to both ECS decoders only. Link 2 data (UHF) is fed to the CIU and also directly to the MCS. In addition to receiving the input data, the CIU also generates inhibit signals for the MCS to prevent simultaneous ECS/MCS processing on the same link.

9.6.1.2 Command Decoders. The two synchronous decoder units (A and B) in the ECS accept inputs from either the CIU or the programmable memory units. RTC inputs from the CIU are verified, decoded and executed. Stored program commands are sent to the PMU's. SPC's received from the PMU's are decoded and executed. The complete operation of a decoder can best be described by dividing it into RTC and SPC command operation.

9.6.1.2.1 Real-Time Command Decoder Operation. Command link data is supplied to both decoders in parallel by the CIU. The seven-bit RTC is preceded and followed by one or more S (synchronization) pulses. The first bit transmitted



3.9-20

Figure 3.9-12. Extended Command Subsystem

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to the ECS is the parity bit (bit 1). Bits 6 and 7 are the decoder address bits which determine whether decoder A or B executes the command. The addressed ECS decoder must be in a real-time state to accept an RTC.

The received command is checked to verify that it exhibits proper bit count, parity, and address. For valid RTC's, the receipt of the trailing S pulse(s) signals the start of execution, and the voltage converter generates a command pulse which is supplied to the selected output line. For internal RTC's (those controlling the ECS), the voltage converter output pulse is inhibited.

9.6.1.2.2 Stored Program Command Decoder Operation. The stored program command transmitted consists of 39 bits preceded and followed by one or more S pulses. The first 22 bits are the time label bits, with bit 1 (0.2 second) the least significant bit. Bits 24-38 are the function bits containing the command data that is transferred to the decoders from memory when the time label is matched.

An addressed memory may be loaded via either decoder. The command is transmitted to the memory and checked for proper bit count and parity. The command is rejected if one or both are incorrect.

Readout of the 15-bit function portion of a command from memory occurs 0.2 second after the time label of the command (NSPC, VSPC, or PSPC) matches the clock (vehicle) time. When a command is about to be read out, both decoders receive a signal which inhibits RTC operation, and, if necessary a signal to turn on decoder power. Should both memories read out simultaneously, each decoder accepts the command from its associated memory and executes the command if it is addressed to that decoder.

The decoder logic determines whether the SPC is an internal or external command, verifies the bit count, and determines whether it is a valid NSPC or VSPC, or is part of a PSPC pair. Execution of an NSPC results in one command

pulse output on the command line selected by the NSPC code. VSPC's require two output lines for each variable bit. An output pulse is supplied to one line if the bit is a logic 0, and to the other if the bit is a logic 1. In addition, there is one discrete output provided each time the VSPC is executed (the implicit bit).

PSPC decoding is accomplished differently in that two identical PSPC's exhibiting a difference in time labels of 0.2 second must be read out from memory. The first is treated like an ordinary NSPC or VSPC except that, upon identification as a PSPC, the output is inhibited. When the second half of the PSPC is read out 0.2 second later, a bit-by-bit comparision of the two commands occurs to verify that they are identical, and execution takes place. Any difference in the bit structure, or a difference of more than 0.2 second in the time labels, will prevent execution.

PSPC command pulse output requires two isolated wires for each command. Upon execution, one carries the command pulse, and the second is tied to ground during the command period, to provide an isolated return. As explained earlier, the use of switched output and return lines afford added protection against hardware failures such as short circuits.

9.6.1.3 ECS Clocks. The ECS contains two identical clock units. Each clock generates timing signals for its associated half of the ECS. Both, in conjunction with their associated PMU, generate timing signals A, B, and C for use external to the ECS. However, only one clock, as selected by command, outputs these signals at any given time.

The clock circuit contains a temperature-compensated crystal oscillator which provides a frequency of 4.096 MHz. Countdown circuitry provides the basic clock frequency of 1.024 MHz. Additional countdown circuits generate the timing signals for use by the ECS, and for external use.*

*The vehicle time code (signal A) is provided to the clock by its associated PMU.

In operation, the clocks are normally synchronous, with clock B the master and clock A the slave. Clock B provides a sync pulse to clock A every 0.2 second. A discriminator checks to see if the clocks agree within a specified tolerance. If so, clock A is synchronized to clock B. Otherwise the clocks are allowed to run asynchronously.

9.6.2 Minimal Command Subsystem

The minimal command subsystem is a backup system for the ECS, and is capable of performing the same functions except on a limited scale. The MCS processes the full range of stored program and real-time command types. In addition, the MCS also accepts the two secure word real-time commands (SWRTC 1 and SWRTC 2) which enable MCS termination events for SRV 1 and SRV 2.

9.6.2.1 MCS Components. The MCS consists of two sections, the minimal command unit (MCU) and the minimal voltage converter (MVC). The MCU receives command inputs from link 1 SGLS 1 (from the ECS command input unit) or from the UHF backup command link, link 2. Real-time commands are executed immediately. Stored program commands received by the MCS for later execution are stored in a non-programmable memory. The MCU also receives external inhibit signals from the ECS which prevent the MCS from responding to data on a link if the ECS is being addressed on that link.

The MVC acts as the power control for the MCS. The power is normally off when no information is transmitted to the ECS or MCS except if SPC's have previously been stored in the memory. Transmission of S pulses on link 1 SGLS 1 or link 2 will turn power on regardless of whether the subsystem is to respond to the following commands. The MVC will turn off when the S pulse transmission stops unless the proper sequence of secure real-time commands (SRTC's) and a secure word is received to put the subsystem in an

operate mode.

9.6.2.2 MCS Real-Time Command Execution. Each real-time command consists of a 7-bit word preceded and followed by an S pulse. The first bit provides even parity for the word, and bits 2-7 contain the command function. The subsystem checks the incoming command for the correct number of bits and parity. Proper bit count and parity enable execution of the RTC upon arrival of the trailing S pulse.

9.6.2.3 MCS Secure Real-Time Command Execution. A second type of RTC, secure real-time command (SRTC), is also accepted by the MCS. These are processed in essentially the same manner as normal RTC's, except all of the SRTC's must be followed by a secure word match operation before the subsystem will execute the commands.

9.6.2.4 Stored Program Command Execution. The time labels of SPC's are compared with the time word every 0.2 second for a possible readout to the decoder circuitry. When a match is obtained, the command will be read out and executed during the next 0.2 second interval (unless it is the first command of a PSPC pair).

When an NSPC is executed, a command output pulse is supplied on the appropriate line. Execution of a VSPC results in an output on one of two lines for each bit, depending on the bit state, plus an implicit output. Each PSPC output requires two lines, one carrying the command pulse, the second providing an isolated ground return when the command is being executed. As in the ECS, the MCS PSPC's require successive words stored in memory. The two are identical except for the time label portions which are one time interval (0.2 sec) apart.

9.6.2.5 Secure Word Operation. The secure words used for secure real-time command execution, and two special secure words for the execution of the two

39-bit secure word real-time commands (SWRTC) are stored in the MCS prior to launch.

The two SWRTC commands are, by themselves, the secure words to be matched. Unlike SRTC's, these commands stand on their own. Once received and matched to the appropriate stored secure word, an output pulse is provided on the command line.

9.7 ECS Real-Time Bias

Real-time bias (RTB) is a 6V word command which incorporates a fixed offset in SPC execution time. The magnitude of bias is chosen on the basis of differences between the vehicle ephemeris as verified at the remote tracking station and the predicted ephemeris used in assembling the command message. The major effect of small inaccuracies in the predicted ephemeris is to introduce error in the in-track acquisition times of photographic targets. By adjusting command times to the actual vehicle position, events such as photographic sequences will occur at the point (in terms of vehicle location) where they were originally intended.

In operation the RTB command subtracts the selected bias from the vehicle clock time before comparison is made with the SPC time label. The bias occurs in increments of 0.2 second up to a maximum of ±6.2 seconds. The time bias affects only the PMU in which it is loaded, and will remain in effect until the next bias command is executed. The actual vehicle clock time, which is recorded on the film as timing signal A, remains unaltered.

9.8 Command Processor

The PPS/DP EAC command processor serves as the primary interface between the SCS and PPS/DP EAC for non-pyrotechnic commands. All pyrotechnic related commands are received and processed by the initiator electronics unit which is described

in Part 3, Section 7. The CP provides electrical isolation between the SCS and PPS/DP EAC, and the command signal decoding and encoding logic required for PPS/DP EAC operation. Where a user unit (i.e., a unit receiving commands from the CP) has redundant circuits, the CP provides independent, parallel redundant command processing circuits to maintain the reliability. In addition, the CP provides instrumentation outputs which monitor the receipt of commands from the SCS.

9.8.1 Command Processor Physical Properties

The command processor is mounted to rails in the supply electronics module which run from the +Y film supply enclosure wall outboard to rings of the supply electronics structure (SES). To reduce vibration loading of the unit during launch, special vibration isolators are placed between the CP feet and mounting rails.

A metal strip on one foot provides the necessary electrical conduction between the CP and SES for electromagnetic interference control. For a more exact description of CP location within the SEM, refer to the figures of Part 3, Section 1.

Physically, the CP is approximately 6.5 inches x 10 inches x 12 inches excluding the 6 mounting feet, and weighs slightly less than 26 pounds. As shown in Figure 3.9-13, the CP consists of a black anodized aluminum base plate and cover, and two stacks of epoxy-fiberglass printed circuit boards (14 total) mounted to the base plate. Since the unit uses very little power, no special heat sinking is required. The bottom side of each board is conformal coated as is each integrated digital-to-analog converter used within the CP. The boards are then individually foam potted flush with the vibration damper strips which are attached to the two board edges that have no input/output connections.

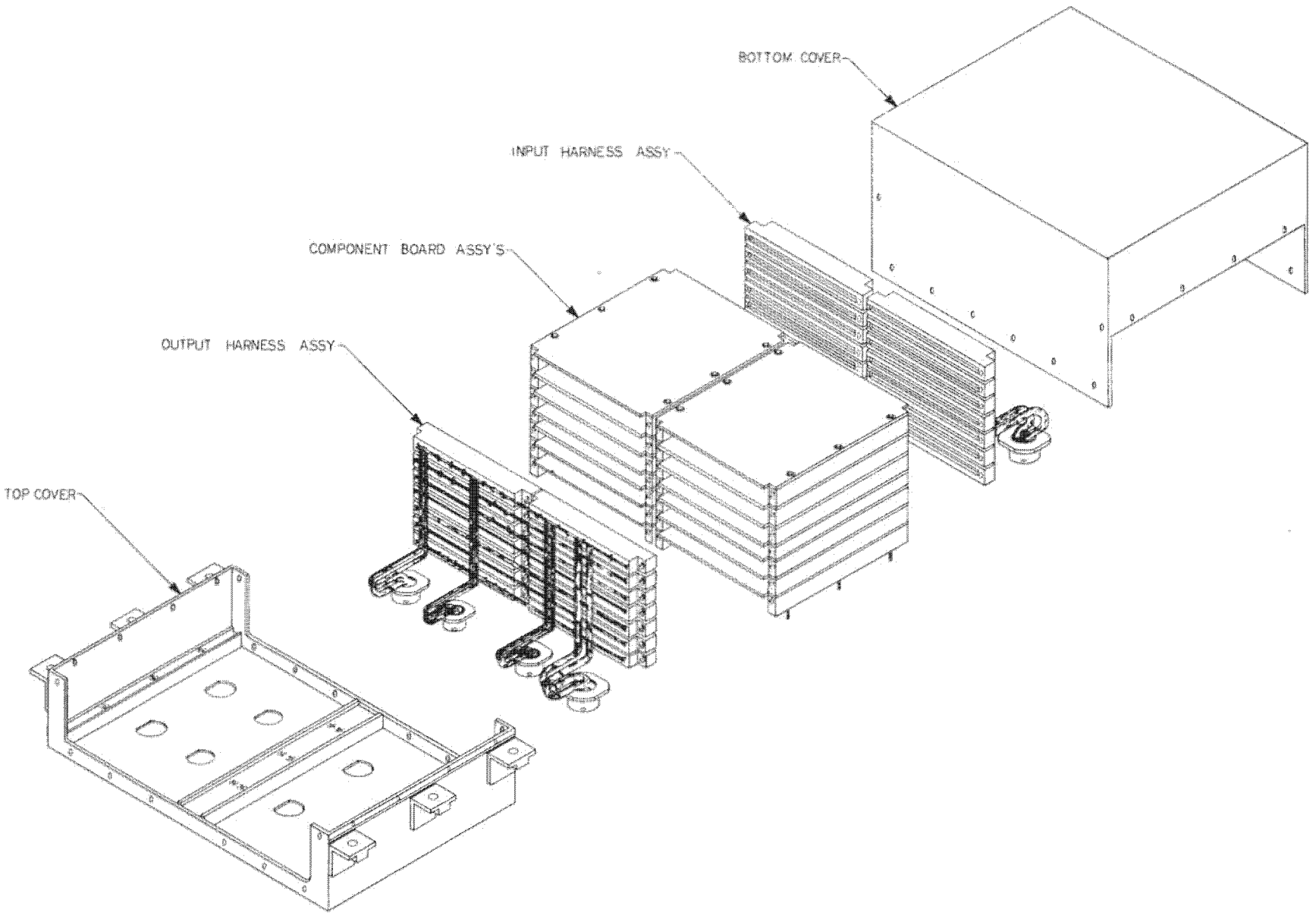


Figure 3.9-13. Command Processor Assembly

For purposes of isolation, input and output signals are carried by separate harnesses on opposite sides of the circuit boards. Power from the power monitor and control unit (PM&C) to the CP is carried by the output harness to maintain the isolation. Connections from the harnesses to the PPS/DP EAC and SCS are carried through eight electrical connectors mounted on the base plate. Connectors J1, J2, J3, and J5 carry output functions, and connectors J4, J6, J7, and J8 carry inputs from the SCS.

9.8.2 CP Operation

Command information is received as shaped electrical pulses on dedicated wires. CP outputs are either reproductions of the SCS command pulses or relay contact closures/openings. The shaped output pulses operate relays in the PM&C. This is the only case where CP power is used as a signal to another PPS/DP EAC electronics unit. CP relay contacts function as switches for their user units in the PPS/DP EAC. No connection is made between the CP power and instrumentation, and the user unit wires, or between wires provided by different user units.

A single case exists where a CP input and output are electrically continuous. The viewport door OPEN/CLOSE commands are hard wired through the CP to the viewport door electronics, with only command receipt monitoring performed in the CP. All processing of these commands is accomplished within the viewport door electronics. Proper isolation is maintained within that unit using latching relays.

9.8.2.1 SCS/PPS Command Isolation. Extremely high input (SCS) - output (PPS) isolation is provided by optically coupled isolators or latching relays used for the command interface. In addition, these circuits also maintain the proper load requirements for received commands as set by agreement among the associate contractors. The optical isolators are used where large fan-out requirements dictate parallel relay loads whose combined impedance falls below

the interface requirements, or where a shaped output pulse is to be provided to the PM&C.

All input command pulses are referenced to the command subsystem returns. Where incoming command lines are tied together, diode decoupling is used to prevent a pulse from being returned into the command subsystem. Within the CP, the command return wires for all normal and variable, ECS commands are connected together as are the returns for all normal and variable MCS commands, and all returns are isolated from the structure and the main power returns. For protected commands, separate isolated, switched returns are provided in both the ECS and MCS. Within the SCS, all command return wires used for the normal, variable, and real-time commands are tied together within the command subsystem and through the command subsystem to the vehicle structure.

Returns for PSPC commands maintain their isolation within the SCS. The only exceptions to this are where returns for redundant protected command loads may be tied together, or where a protected command is gated with a non-protected command load as shown in Figure 3.9-14.

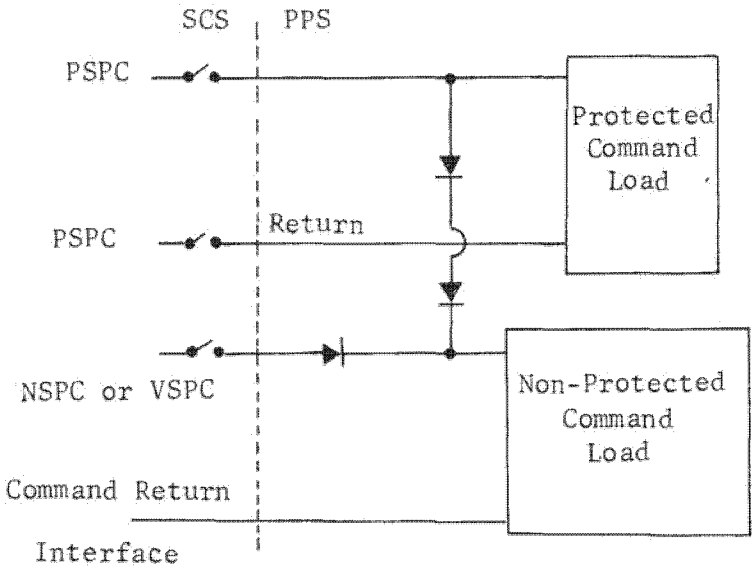


Figure 3.9-14. OR Gating Protected Commands with Non-Protected Commands

The isolation circuits in the CP provide several other benefits, the first of which is high noise immunity. The amount of energy required to operate relays makes them immune to narrow transient spikes. For optical isolators, zener diodes (15 volts) in series with the input provide this immunity.

Where latching relays are employed, they also serve as a nonvolatile memory. When used on primary outputs, or as instrumentation monitors on pulsed outputs, they enable command states to be retained during power-off periods.

Due to the relays and pulse circuits, the power consumption of the CP from the unregulated supply (24.5 vdc nominal) and from the instrumentation supplies (+5/±15 vdc) is extremely low. The unit draws less than 1 ma during quiescent periods, and less than 750 ma in a maximum of 100 msec surges from the unregulated supply, and typically 10 ma and 5 ma from the ±15-and +5-volt supplies respectively.

9.8.2.2 CP Standard Circuits. The CP contains several standard circuit designs, each of which is used for many different command functions. The descriptions for individual command functions following this section generally include only logic diagrams, and refer to the standard circuit type(s) as appropriate. The function CP A/B SELECT refers to the selection of redundant circuitry to process certain commands. Not all circuits within the CP are provided with this capability. However, completely redundant, but non-selectable circuitry is provided for all redundant PPS/DP EAC subsystems.

9.8.2.2.1 Command Input Diode "OR" Gate. The command input diode OR gate (Figure 3.9-15) is used to combine commands performing a single function but coming from different sources, and provides diode decoupling between incoming commands from the SCS.

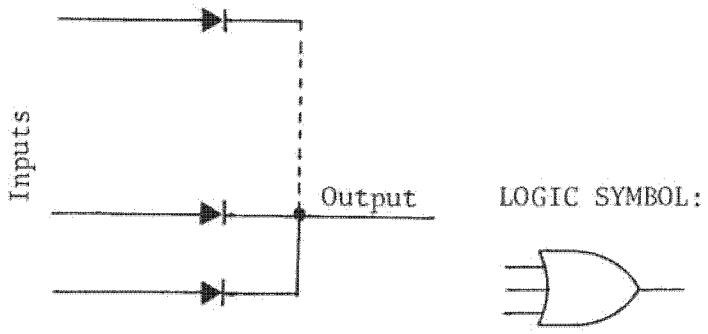


Figure 3.9-15. Command Input Diode OR Gate

9.8.2.2.2 Latching Relays. The latching relays contain two sets of contacts which operate together and can be set to either of two states by providing a pulse to the appropriate actuating coil. The logic representation of a latching relay is not direct. A set/reset flip-flop represents the relay state, with a high output indicating which direction the relay is commanded. The contacts are used as switches, and are represented by logical AND gates where appropriate (see Figure 3.9-16).

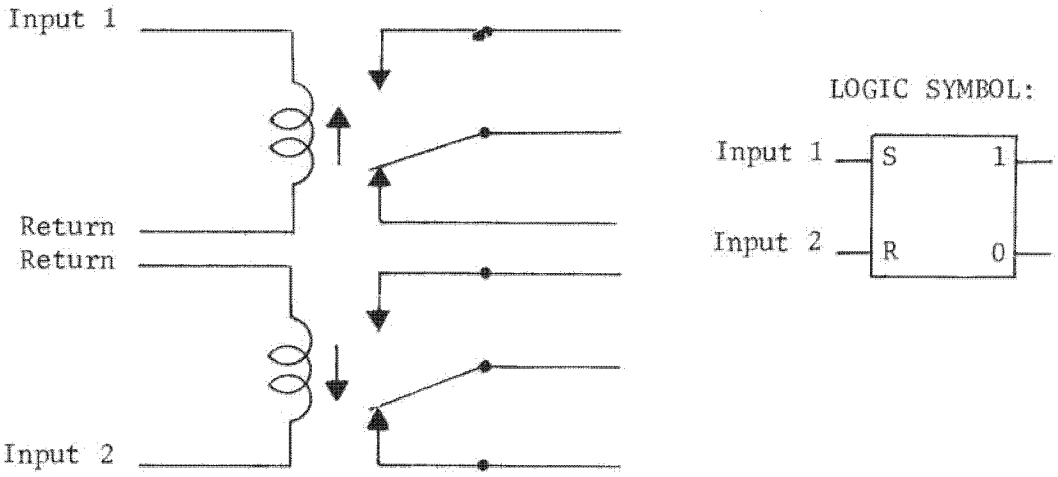


Figure 3.9-16. Latching Relay Logic Representation

As an example, the following circuit (Figure 3.9-17) is used as an ON/OFF control, connecting the output and return as commanded:

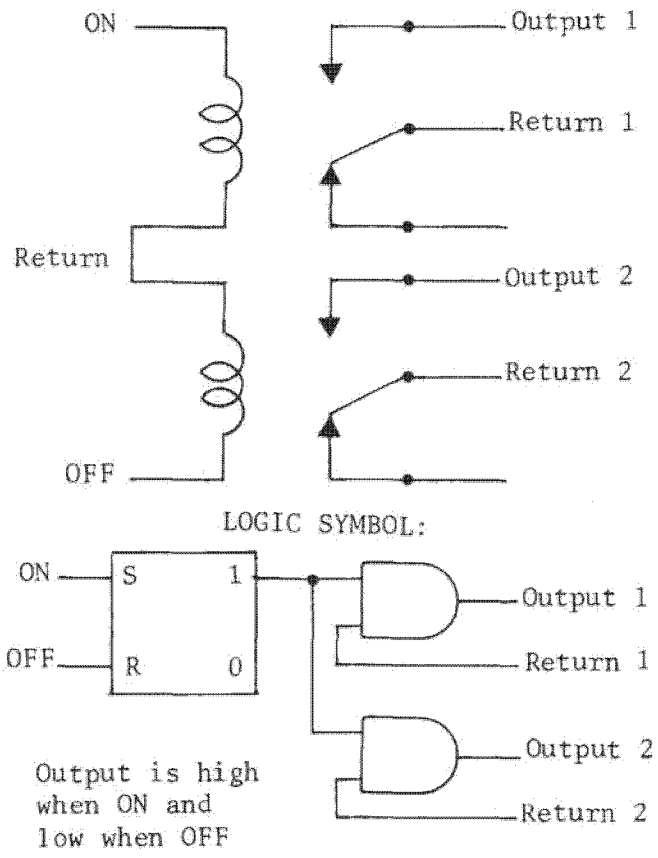


Figure 3.9-17. Latching Relay ON/OFF Control Circuit Logic Representation

Some simplification occurs in the function logic diagrams in the area of instrumentation outputs, but there is no misrepresentation of the manner in which the function operates.

9.8.2.2.3 Optical Isolator and CP Output Pulse Circuit. The optical isolator circuit is used to handle large relay loads within the CP, or to provide a shaped output pulse to the PM and C. Referring to Figure 3.9-18, the input diodes provide ECS/MCS decoder isolation and protect the photodiode in U1 from reverse bias. Resistor R1 is a ballast resistor which limits current to the photodiode. The zener diode (D2) provides noise immunity. U1 is an optically coupled isolator. Upon receipt of a command pulse, the current through the photodiode causes it to emit light, which turns on the phototransistor. The

phototransistor drives the final stage, Q1, which provides the output pulse in response to the input command pulse. The RC network formed by C1 and R2 is a rise time control network for Q1 and is used to shape the output pulse to meet EMI control requirements.

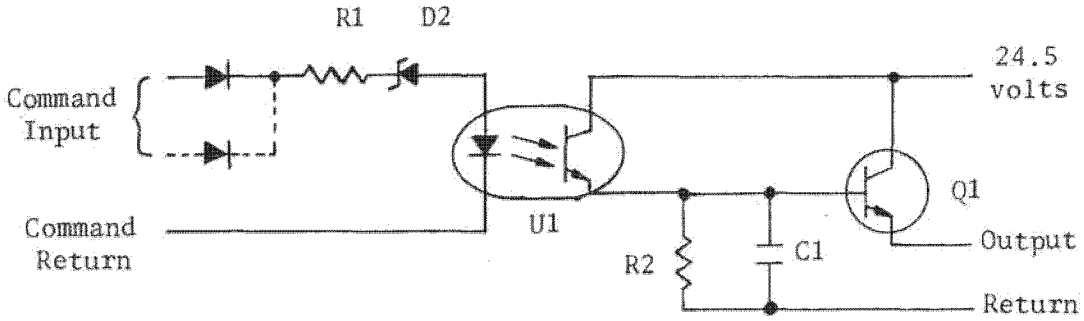
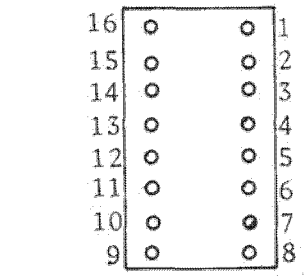


Figure 3.9-18. Basic Optical Isolator and Pulse Circuit

9.8.2.2.4 Instrumentation Circuit. Command receipt is monitored by a latching relay which feeds 5-volt instrumentation power to one input of a 4-bit digital-to-analog (D/A) converter through an isolation resistor. The converter (Figure 3.9-19) employs a 4-bit switched ladder to generate a 16-level analog output that can be used to indicate the state of each of 4 unique command inputs. The output voltage levels, shown in Table 3.9-3, and the output impedance characteristics of the device are compatible with the input requirements of the digital telemetry unit, and are not processed further.



MECHANICAL CONFIGURATION

PIN ASSIGNMENT

1	BIT ONE (LEAST SIGNIFICANT)
3	BIT TWO
5	BIT THREE
7	BIT FOUR
8	GND
9	-15V
13	OUTPUT
16	+15V
2, 4, 6, 10, 11, 12, 14, 15	NOT CONNECTED

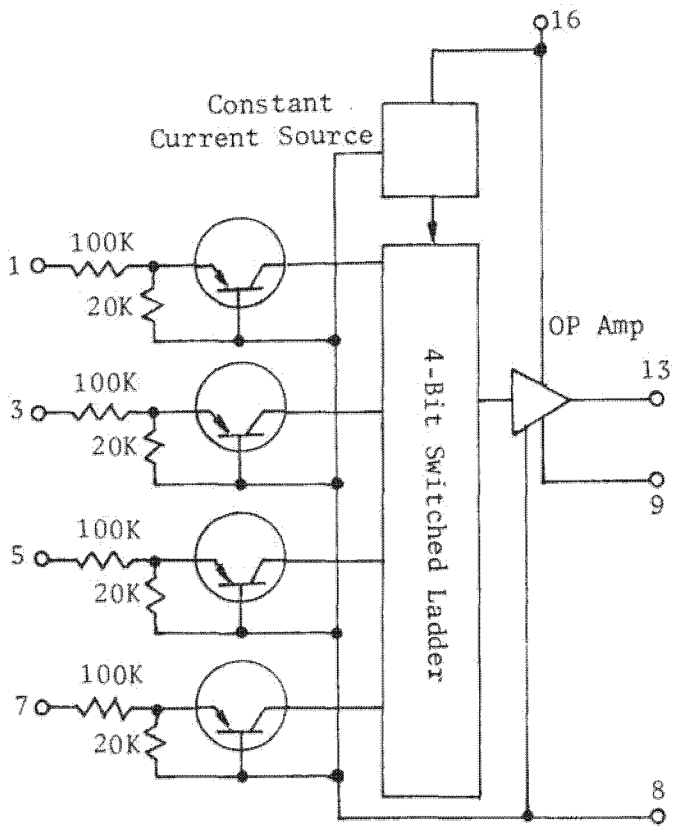


Figure 3.9-19. Instrumentation Digital-to-Analog Converter

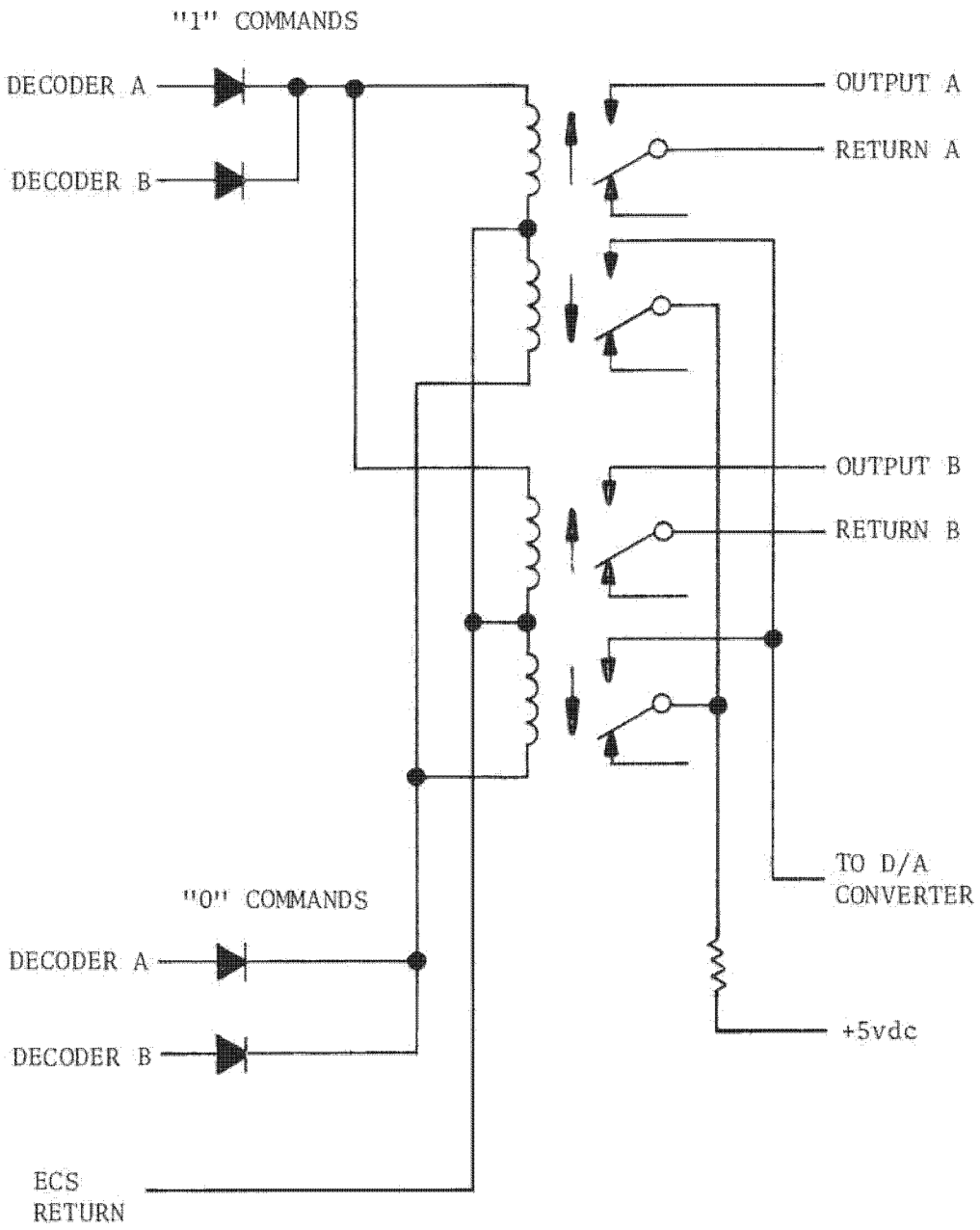
9.8.2.2.5 Basic Processing Circuits. Figure 3.9-20 through 3.9-22 represent the three most basic circuit designs used for processing. The commands from ECS decoders A and B are not shown for the CP SELECT inputs since these commands are coupled through optical isolator circuits and control several relays. All commands from ECS decoders A and B, and from the MCS decoder, are diode decoupled.

TABLE 3.9-3

INSTRUMENTATION VOLTAGE LEVELS

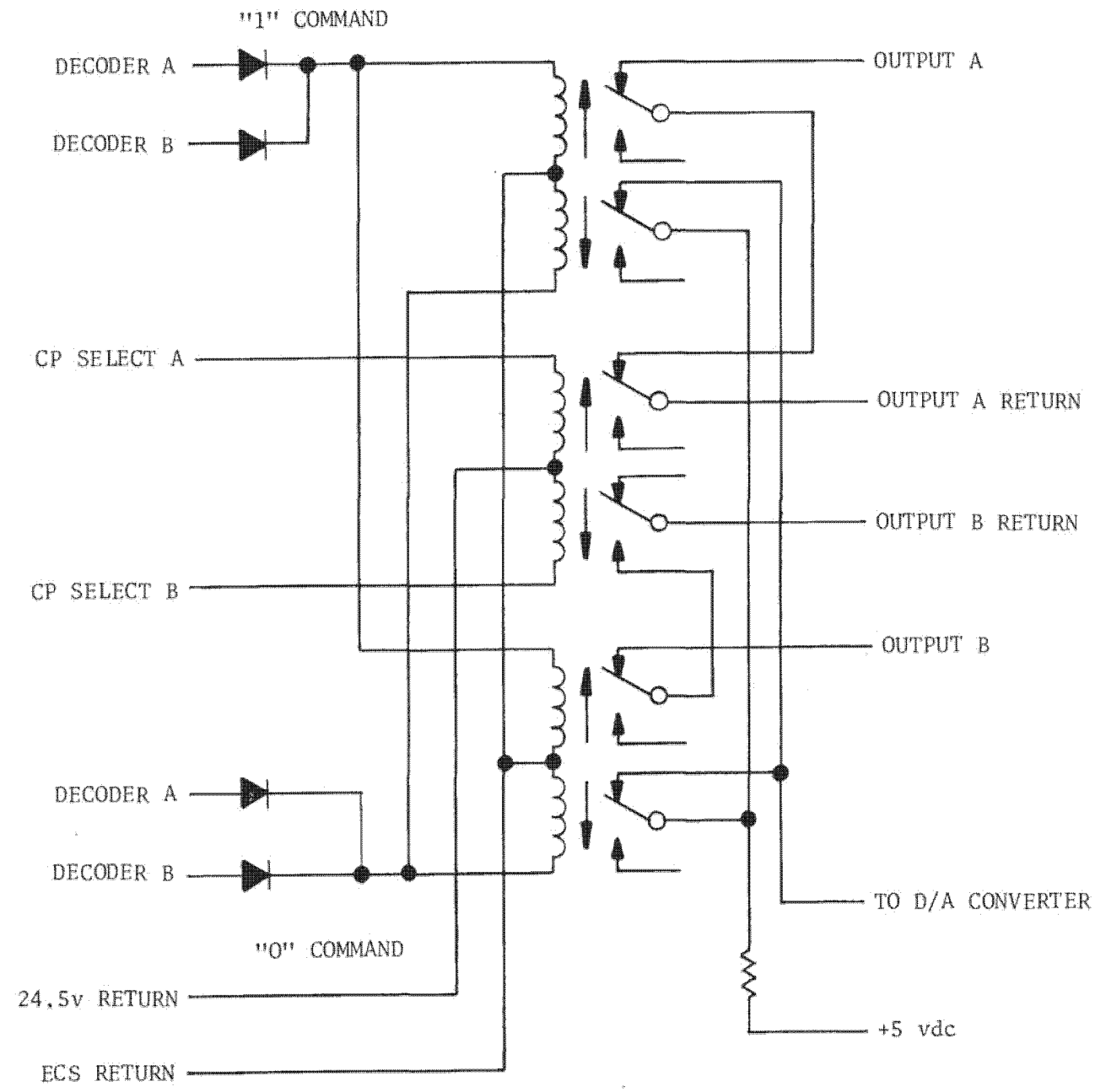
State of Command Switches*				Nominal Instrumentation Point Voltage Level
Bit 4 (MSB)	Bit 3	Bit 2	Bit 1 (LSB)	
0	0	0	0	0.25
0	0	0	1	0.55
0	0	1	0	0.85
0	0	1	1	1.15
0	1	0	0	1.45
0	1	0	1	1.75
0	1	1	0	2.05
0	1	1	1	2.35
1	0	0	0	2.65
1	0	0	1	2.95
1	0	1	0	3.25
1	0	1	1	3.55
1	1	0	0	3.85
1	1	0	1	4.15
1	1	1	0	4.45
1	1	1	1	4.75

* "1" represents switch closed (command received).



NOTE: Commands may also be coupled through optical isolators, in which case the return line will be the 24.5v power return.

Figure 3.9-20. Fully Redundant Processing and Outputs, Cross-strapped Inputs



NOTE: Commands may also be coupled through optical isolators, in which case the return will be the 24.5v power return. The basic logic remains unchanged.

Figure 3.9-21. Basic CP A/B Mode Switch Circuit

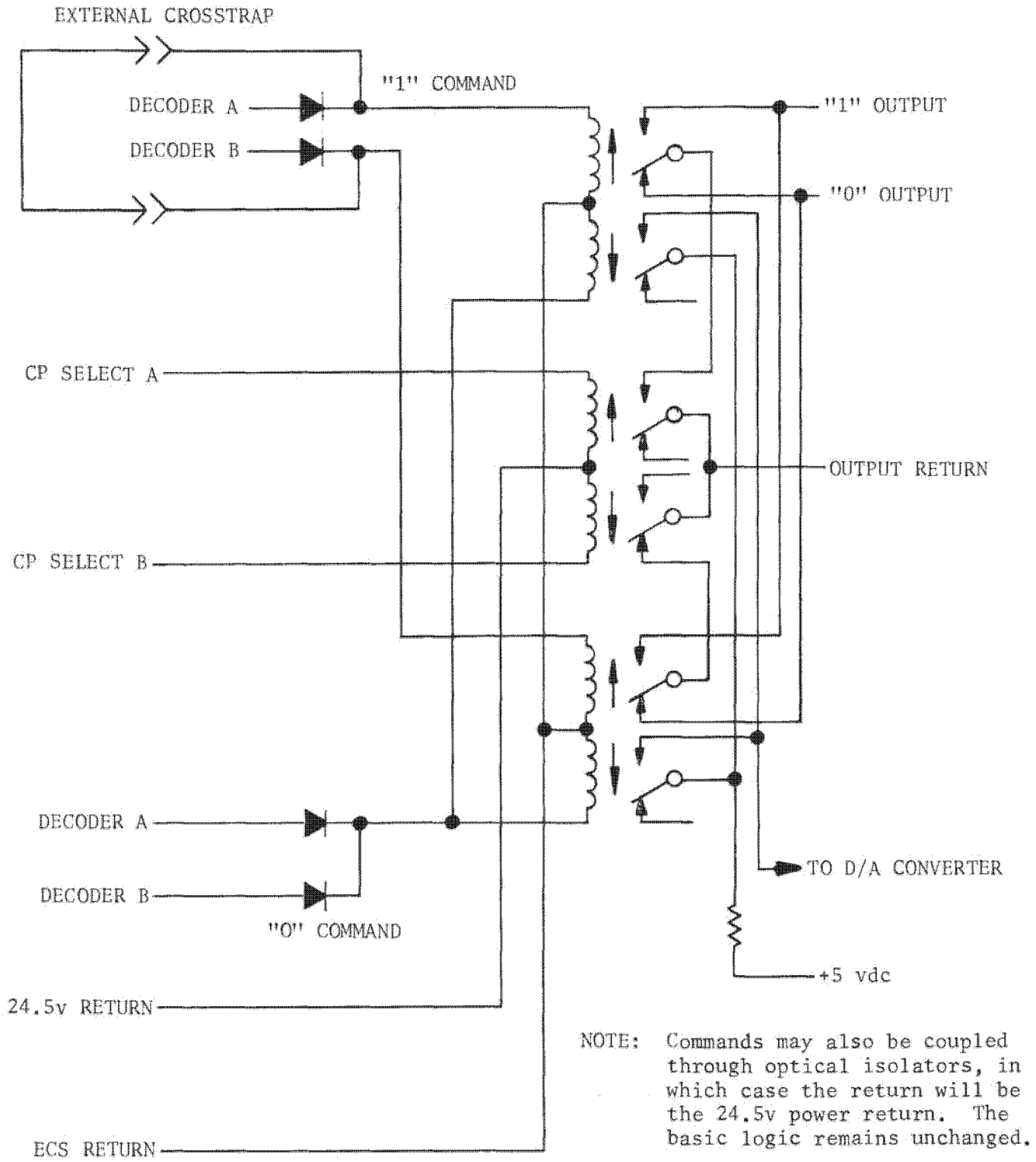


Figure 3.9-22. Basic Servo Mode Switch Circuit

9.8.2.3 CP Functional Circuit Description. All processing circuits can be operated by commands from ECS decoder A or decoder B. A limited number of functions can also be controlled by commands from the MCS decoder. Instrumentation is provided to monitor the receipt of commands for all functions. No monitoring of outputs to the PM and C is provided. The 4-digit function codes on the circuit logic diagrams which follow are assigned by BIF-008, and are used in the 9 x 5 Interconnection Diagram (1418-235) to trace power and signal lines through the PPS/DP EAC cabling.

9.8.2.3.1 CP A select, CP B Select. The CP select circuit (Figure 3.9-23) provides a pulsed output within the CP to select the desired channel of redundant crab and stereo servo command processing circuitry. The pulse also controls a latching relay which steers unregulated power (24.5v) to the desired channel of redundant processing circuitry for 9 and 5 operational power control.

9.8.2.3.2 9 and 5 Operational Power ON/OFF. Both the 9 and 5 operational power commands (Figure 3.9-24) are processed identically. The following description applies to either.

Redundant sides or channels (A and B) are provided in the CP for processing OP commands. Channel selection is controlled by the CP A/B SELECT circuitry, which directs 24.5v power to either channel A or channel B of the OP command circuitry. Optical isolators/drivers in the selected channel send pulse outputs to the PM and C to turn operational power on or off. Redundancy is preserved in the PM and C through the use of separate switches for the A and B signals. The power outputs are paralleled and fed to the associated frequency phase lock loop electronics (FPLLE) and film handling subsystem control electronics (the film handling electronics for 5 OP, and the film control electronics for 9 OP). Additional logic in the PM and C also supplies power to the mirror servos (stereo and crab) when either 9 OP or 5 OP is on (reference Part 3, Section 7).

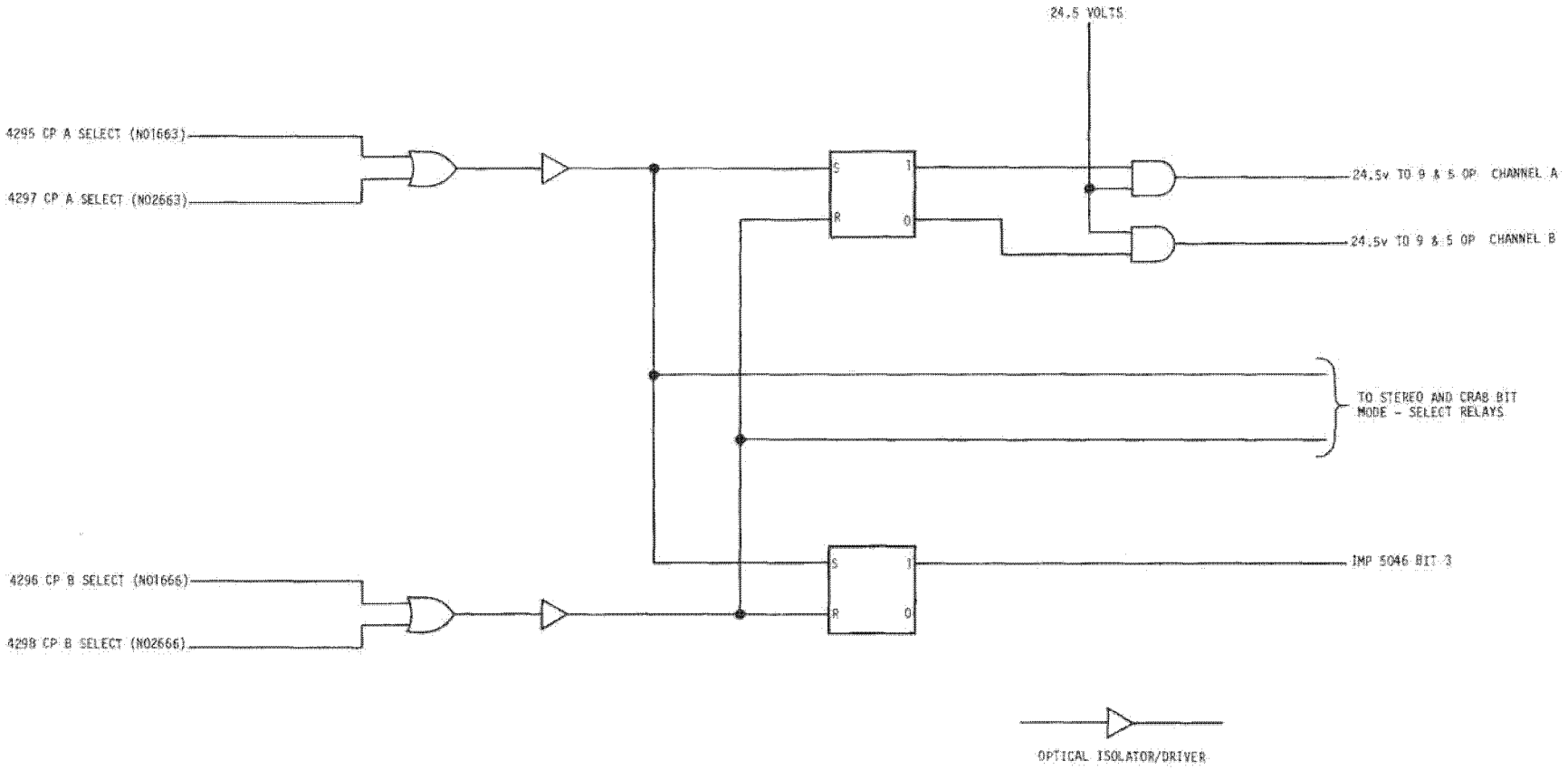


Figure 3.9-23. CP A Select/CP B Select

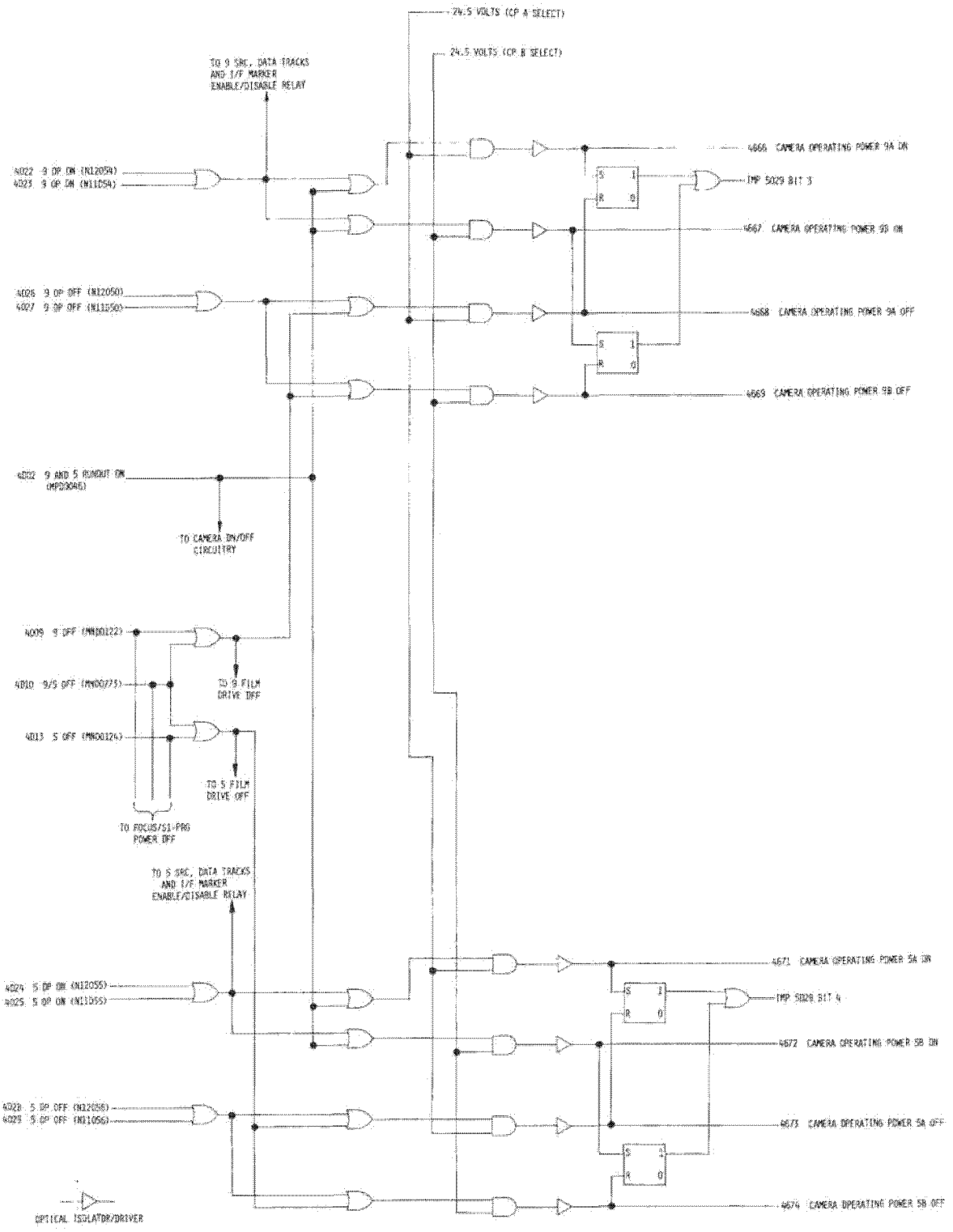


Figure 3.9-24. 9 and 5 Operational Power ON/OFF

Within the CP, 9 OP ON from either channel will reset the 9 SRC, data tracks, and I/F marker disable relay, and 5 OP ON will reset the 5 SRC, data tracks, and I/F marker disable relay. The respective functions will then operate in conjunction with the associated camera (film drive) ON/OFF commands.

The operational power control logic is such that switching "sides" of the CP while operational power is on will result in incorrect instrumentation outputs when the operational power is commanded OFF, since only the instrumentation relay in that channel will be reset. In addition, the wiring of logic within the PM and C will result in operational power being turned off if OP ON is commanded through one side while the operational power switch is on in the other. Power will then turn on when one switch is commanded OFF. This reverse commanding will continue until the logic is reset to its proper state by a corrective command sequence (for a clarification of PM and C logic, refer to Part 3, Section 7).

Other commands controlling operational power as part of their function include:

(1) 9 AND 5 RUNOUT ON (MCS) which turns both 9 and 5 OP on

(2) 9 OFF (MCS) which turns 9 OP off

(3) 5 OFF (MCS) which turns 5 OP off

(4) 9/5 OFF (MCS) which turns both 9 OP and 5 OP off

9.8.2.3.3 9/5 Camera ON/OFF. Processing circuitry for the 9 and 5 camera ON/OFF functions (film drive ON/OFF) is identical (see Figure 3.9-25). Separate circuits are provided for FPLLE side A and FPLLE side B. Selection of the redundant sides is similar to that shown in Figure 3.9-21. The mode relays are operated by the FPLLE A SELECT and FPLLE B SELECT commands. Additional logic is provided such that selection of side A automatically turns side B OFF.

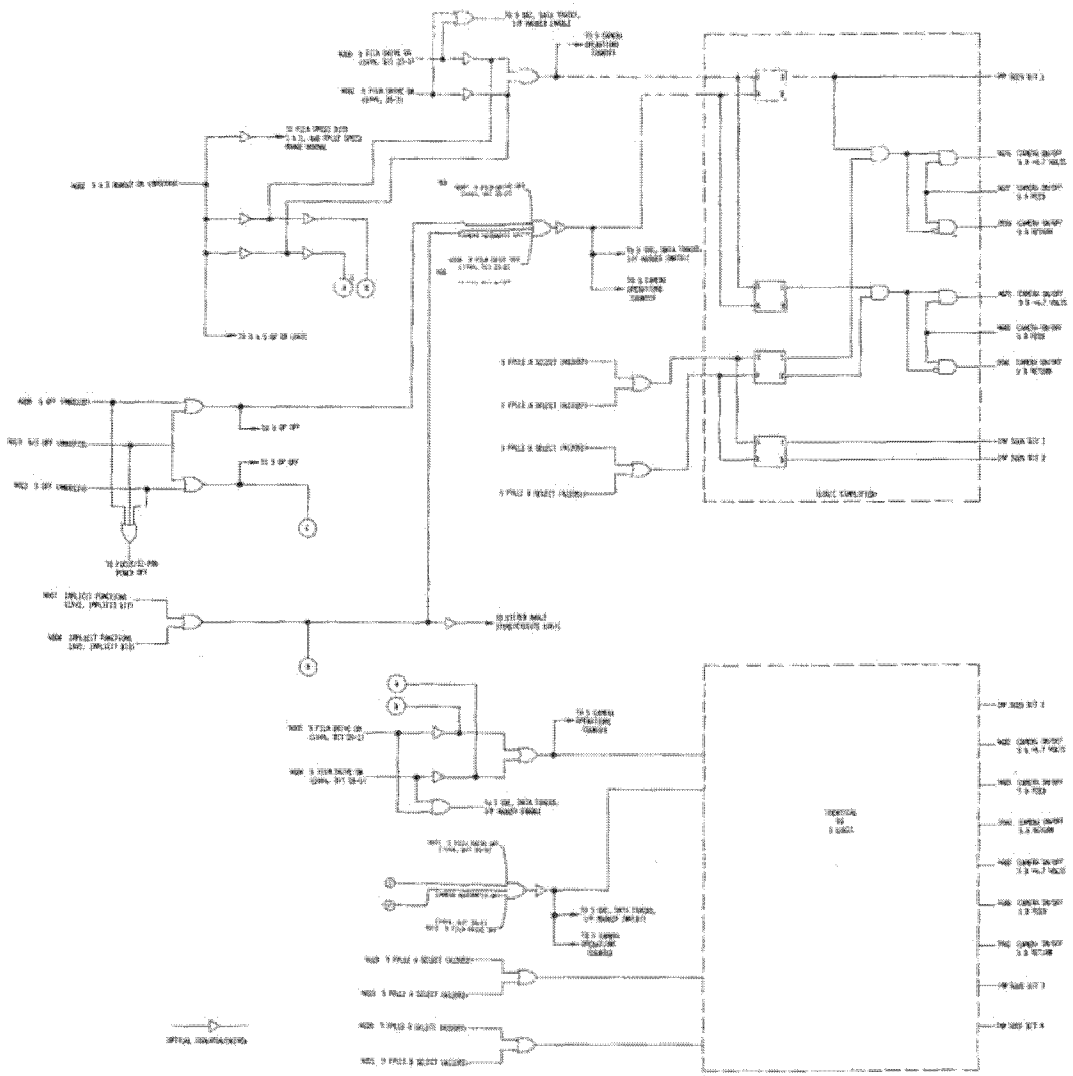


Figure 3.9-25. 9/5 Film Drive ON/OFF

Approved for Release: 2017/02/14 C05097359

Other commands which operate the film drives are:

(1) 9 AND 5 RUNOUT ON which turns on both the 9 and 5 film drives, selects "1" for the two most significant film-drive speed bits, selects the normal speed range for both the 9 and 5 FPLLE's, and turns on both 9 and 5 operational power.

(2) 9 OFF (MCS) which turns off the 9 film drive (9 FPLLE), and inhibits the 9 SRC, data track, and I/F marker functions, turns off 9 operational power, and turns off the focus sensor electronics and S1-PRG power.

(3) 5 OFF (MCS) which turns off the 5 film drive (5 FPLLE), and inhibits the 5 SRC, data track, and I/F marker functions, turns off 5 operational power, and turns off the focus sensor electronics and S1-PRG power.

(4) 9/5 OFF (MCS) which turns off both 9 and 5 film drives (9 and 5 FPLLE's), and inhibits both 9 and 5 SRC, data track, and I/F marker functions, turns off both 9 and 5 operational power, and turns off the focus sensor electronics and S1-PRG power.

(5) 13V WORD implicit bit which turns off both the 9 and 5 film drives (9 and 5 FPLLE's), and inhibits the 9 and 5 SRC, data track, and I/F marker functions. The 13V WORD implicit bit also causes execution of the stereo angle stored by the last 14V WORD command provided 9 or 5 operational power is on.

Film drive can also be stopped by operation of the camera automatic off (CAO) circuit in the CP. The CAO circuits turn off either the 9 or 5 film drives after two supply loopers of film drive have executed, and if no CAMERA OFF command is received. See section 9.8.2.3.23 for a description of operation of the camera automatic off circuits.

9.8.2.3.4 9 and 5 Camera Operations Counters. The 9 and 5 operations counters (Figure 3.9-26) function identically. Each circuit consists of 6 relays interconnected to form a 3-bit, singly-enabled, clocked counter. A camera (film drive) ON command enables the counter, and a camera OFF command clocks it. The counter resets to the zero state on every eighth ON/OFF command pair. Neither multiple

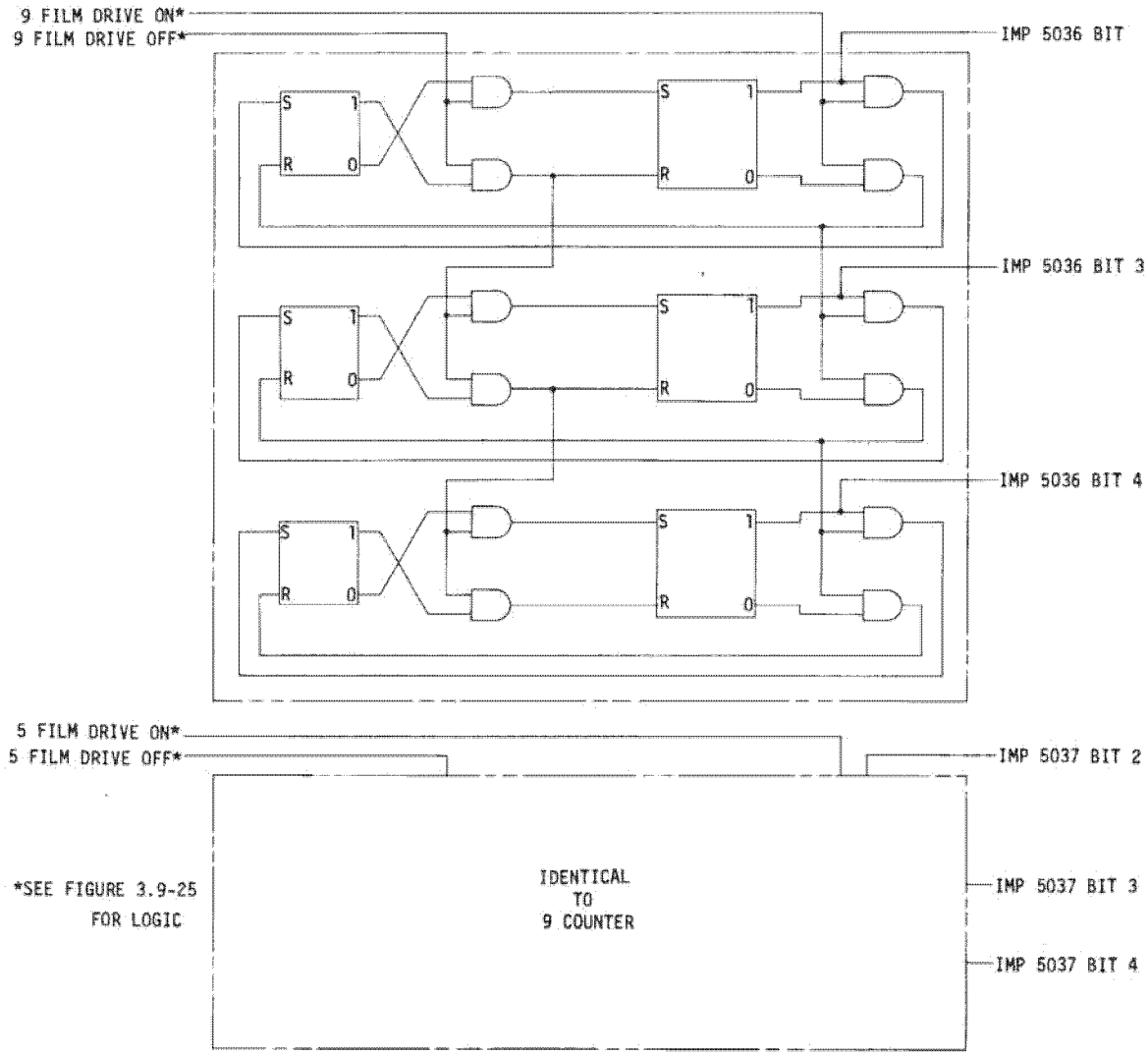


Figure 3.9-26. 9 and 5 Camera Operations Counters

enables nor multiple clocks affect operation. Operational power is not required for the counter to increment.

The relay outputs are fed to the three most significant input bits of a standard digital-to-analog instrumentation converter (Figure 3.9-19). Thus, the output occurs in 8 discrete steps ranging from 0.25 volt to 4.45 volts in 0.6-volt increments.

9.8.2.3.5 9 and 5 Film-Drive Speed Bits 1-10 and SRC Bits. The film-drive speed bit relays function by connecting the bit output to the common return from the associated FPLLE side for the logic 1 state, or opening the circuit for the logic 0 state. Only one film-drive speed may be stored in the CP at a time. Separate relays are provided for the A and B sides of the FPLLE's. One relay contains individual contacts for 9 FPLLE side A and 5 FPLLE side A, and the second relay has individual contacts for side B of the 9 and 5 FPLLE's. A third relay is used for instrumentation monitoring.

FDS bits 1 (MSB) through 4 also produce SRC bits 1 (MSB) through 4 (LSB) in a similar fashion, connecting the output to common or leaving it open in the low altitude mode. In the high-altitude mode, all four SRC bits are commanded to open the common line; resulting in a fixed SRC position when in the high altitude mode (Figure 3.9-27). The 9 subsystem SRC bits are wired to the unused set of contacts on the instrumentation relay, and an additional relay is supplied for the 5 subsystem SRC bits.

FDS bits 1 and 2 have one other controlling command, 9 AND 5 RUNOUT ON, which when executed, sets the two most significant film-drive speed (FDS) bits to the logic 1 state.

Figures 3.9-28 through 3.9-30 represent the FDS bit logic. Bits 1 and 2 are identical, bits 3 and 4 are identical, and bits 5 through 10 are identical.

9.8.2.3.6 Film-Drive Speed Range High/Normal. The film-drive speed range is selected in the same manner as the film-drive speed bits are controlled. The

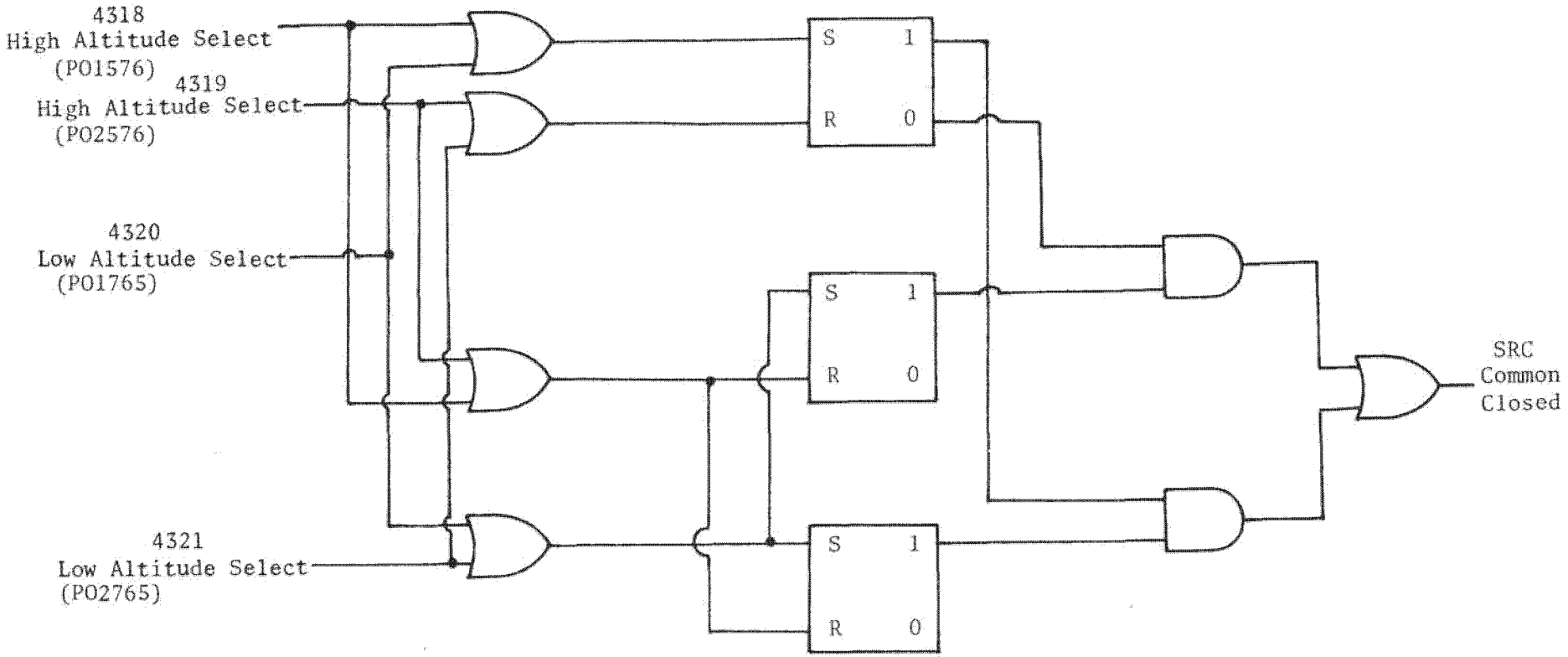


Figure 3.9-27. SRC Command Common Line

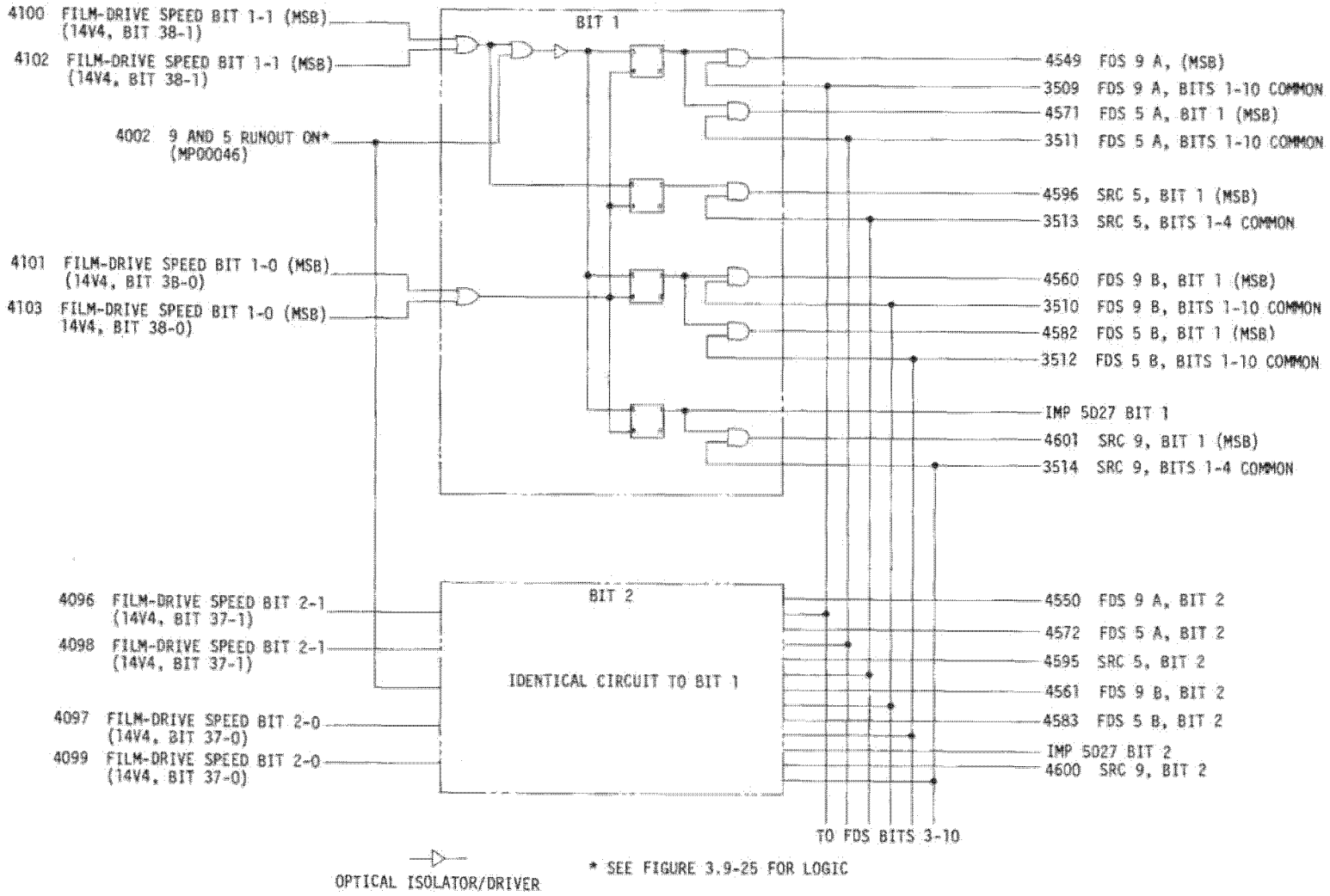


Figure 3.9-28. FDS and SRC Bits 1 and 2

Handle via BYEMAN
Control System Only

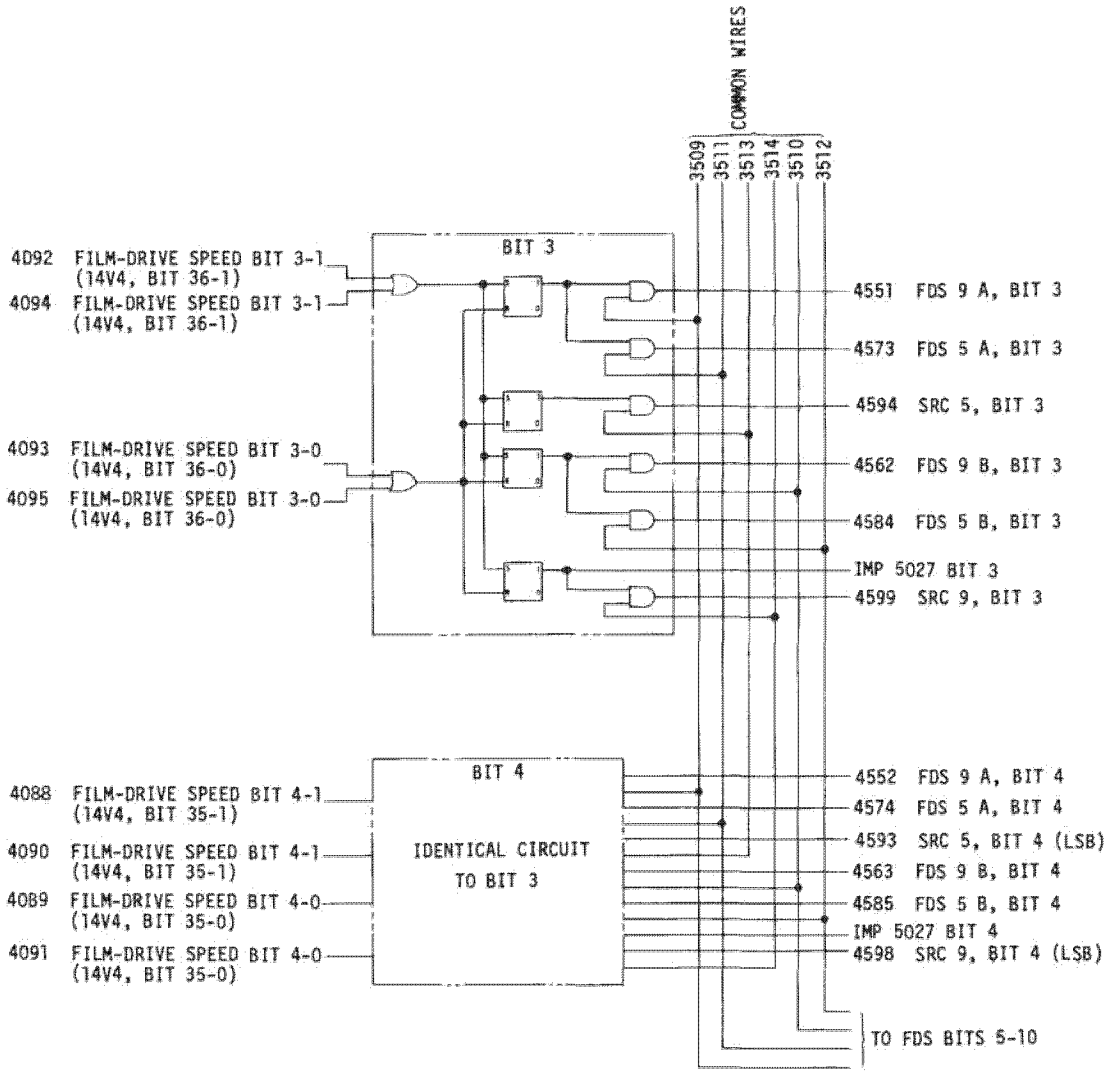


Figure 3.9-29. FDS and SRC Bits 3 and 4

Handle via BYEMAN
Control System Only

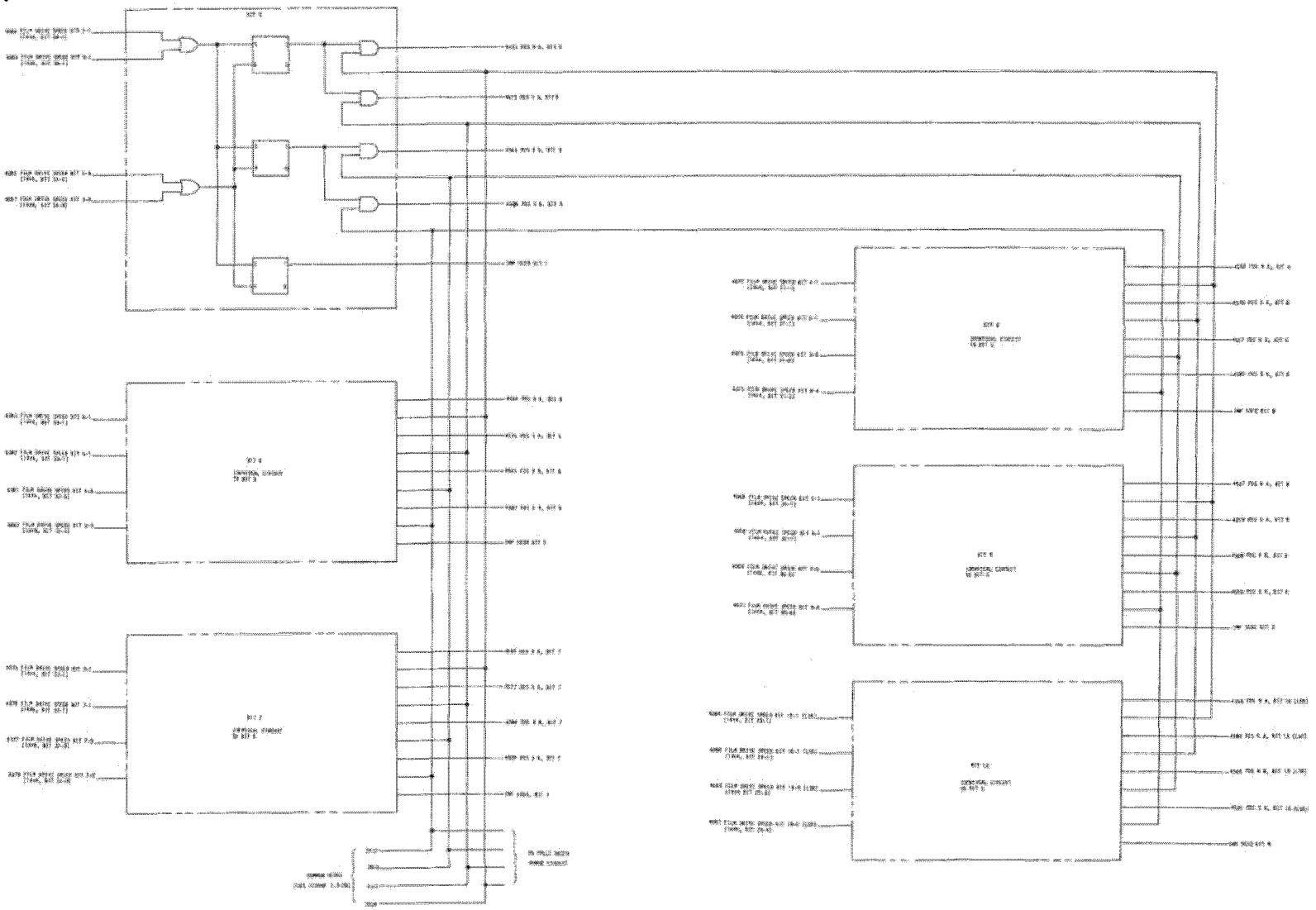


Figure 3.9-30. PDS Bits 5 through 10

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output is connected to the common return from the associated FPLLE side for the high-speed range, and is left open for the low-speed range (see Figure 3.9-31).

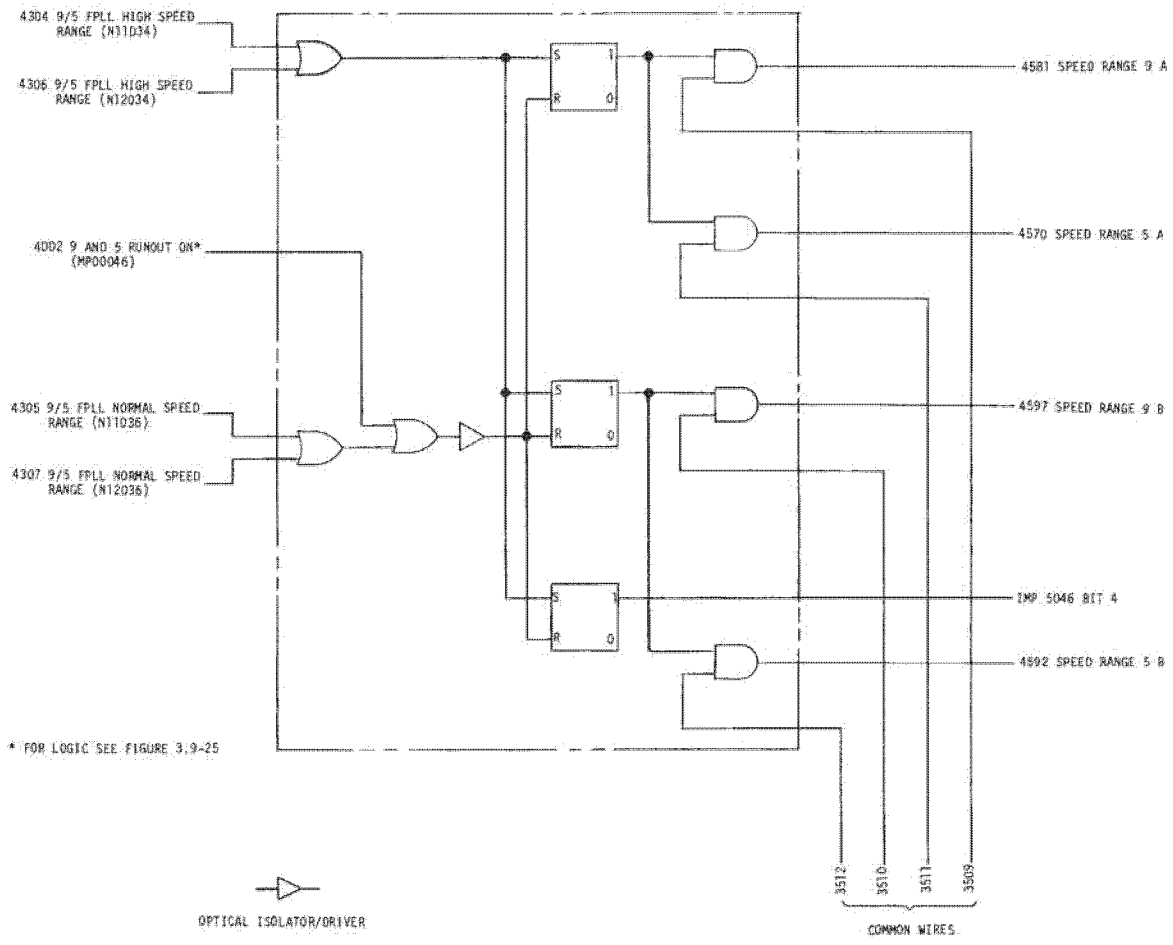
Separate contacts are provided for each side of each FPLLE. However, the relays cannot be individually controlled. Both FPLLE's (9 and 5) will be in the high-speed range or the normal range; the 9 FPLLE cannot be in the high-speed range while the 5 FPLLE is in the normal range, or the 9 FPLLE in the normal range while the 5 FPLLE is in the high range.

The two film drive speed ranges are altered by the HIGH ALTITUDE SELECT and LOW ALTITUDE SELECT commands. When in the high-altitude mode, the normal and high-speed ranges are one-fourth the speeds obtained when in the low-altitude mode. The CP provides commands to the 9 and 5 FPLLEs in the form of switch closures to change film drive speeds to the required high-altitude/low-altitude ranges (see Figure 3.9-48).

9.8.2.3.7 Nominal Platen Adjust Enable/Inhibit and Mode Select. Both the 9 and 5 subsystem commands are processed identically. The output (A for the prime mode, B for the backup mode) is connected to its associated return wire when the platen adjust is enabled (Figure 3.9-32). The mode selection relay, prime or backup, is controlled by command, and selects output A or B (see Figure 3.9-21 for typical selection circuit schematic).

9.8.2.3.8 Nominal Platen Adjust Drive (Plus/Minus/Stop). The NPA drive logic shown in Figure 3.9-33 accepts stored program commands. The plus direction and minus direction circuits follow the basic concept of Figure 3.9-20. The "1" commands are analogous to direction commands, the "0" commands to stop commands.

Signals used by the NPA primary mode circuitry in the camera electronics assembly (CEA) are simple relay closings, connecting the output wire to common. When operating in the primary mode, stored program commands can be used, however, since the NPA backup mode requires a pulse input, it can only be controlled by real-time commands.



NOTE: See Figure 3.9-48 for a logic description of CP Commands which revise film-drive speeds for high altitude modes.

Figure 3.9-31. Film-Drive Speed Range High/Normal

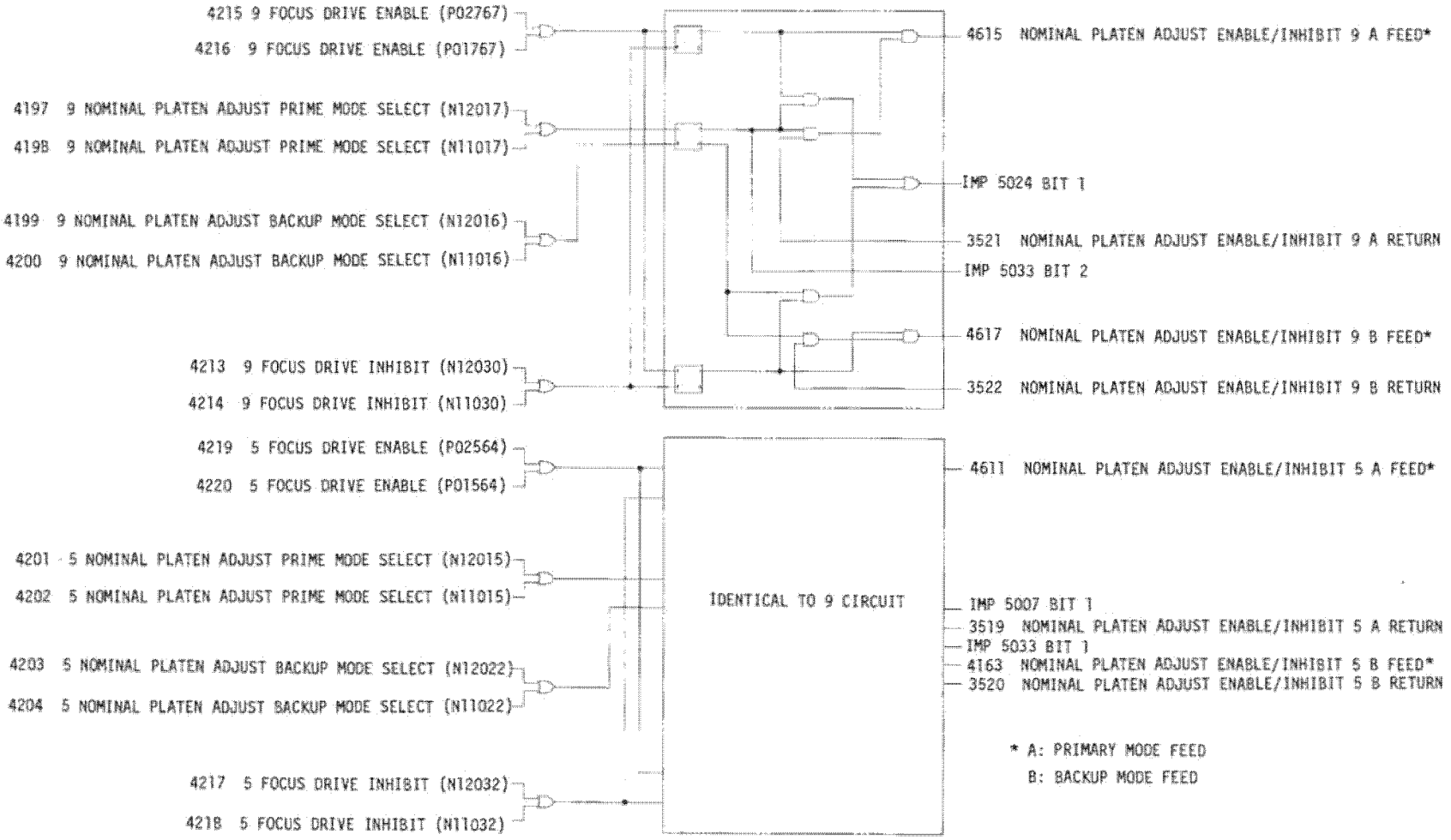


Figure 3.9-32. Nominal Platen Adjust Enable/Inhibit and Mode Select

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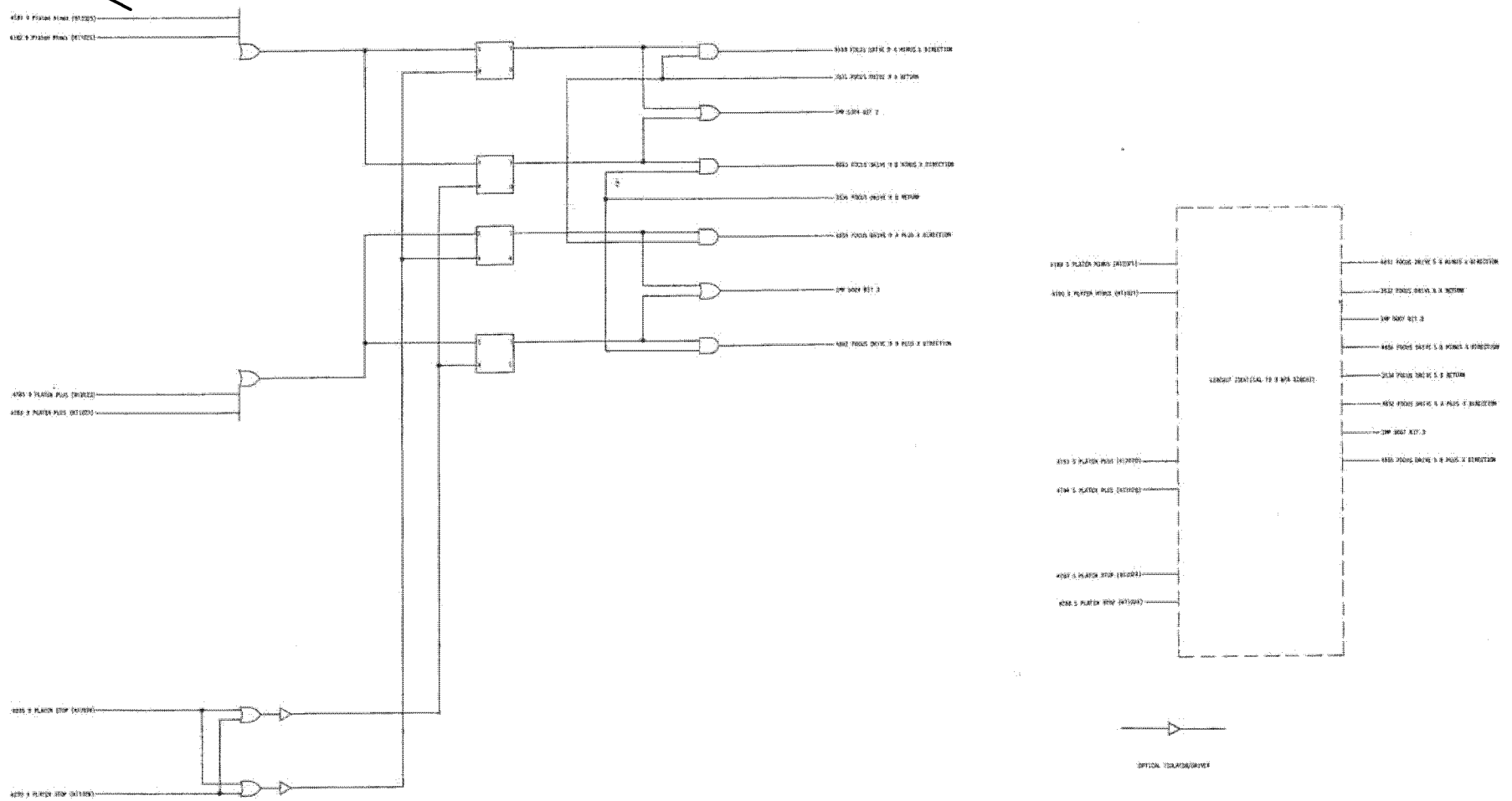

Figure 3.9-33. Nominal Platen Adjust Drive Control

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9.8.2.3.9 9 and 5 SRC Enable/Inhibit/Disable. Two latching relays with contacts in series comprise the circuit for each subsystem (9 and 5). Both relays must be set for the SRC to be enabled (see Figure 3.9-34). One relay (the enable/inhibit relay) is set by the firm drive ON command and reset by the film drive OFF command.* The second relay is reset (opened) by the SRC DISABLE command, to prevent SRC operation with film drive ON/OFF commands, and is set by the operational power ON command.

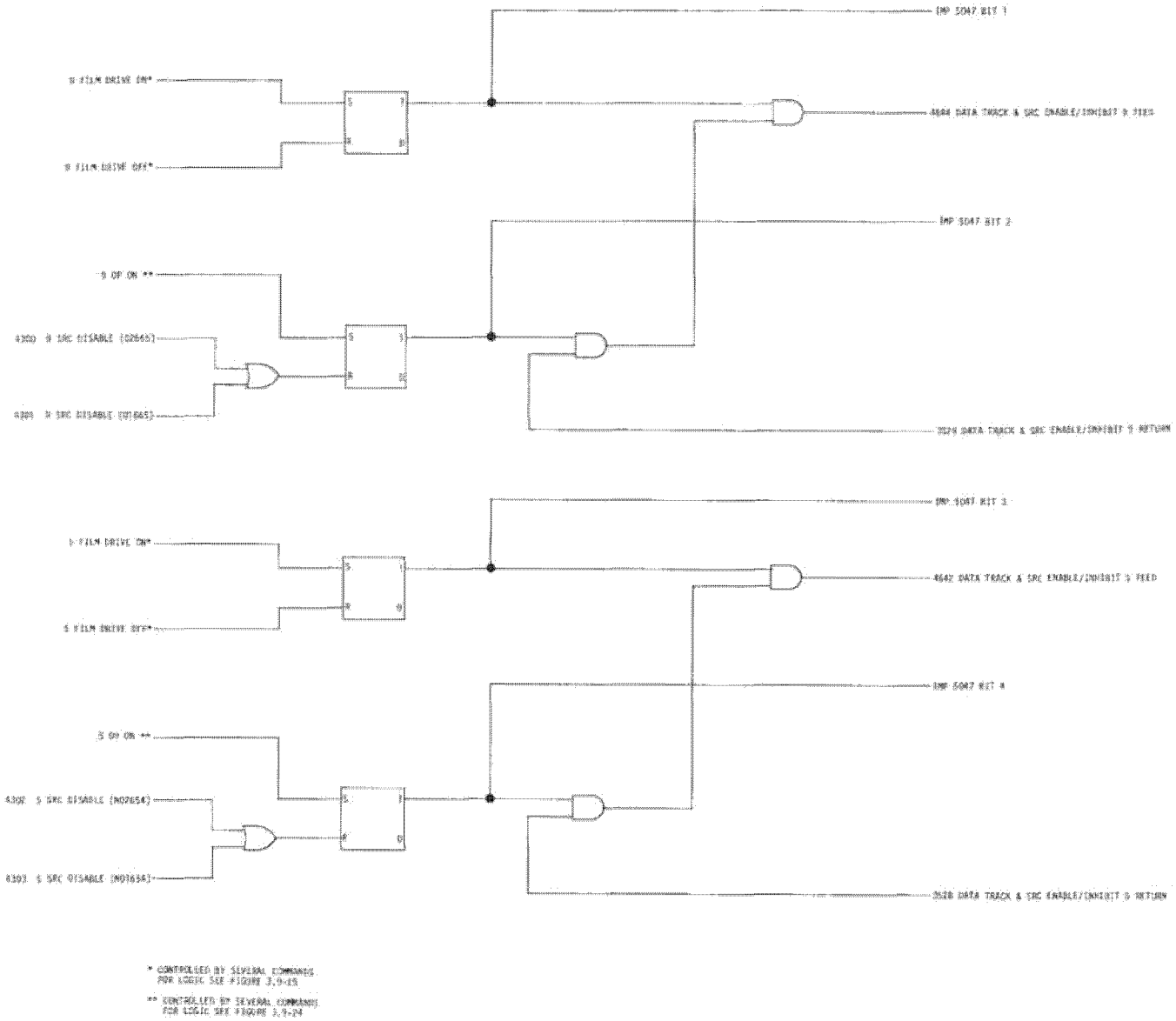
Within the CEA unit, the data track and interframe marker circuits are powered through the SRC power switch. Therefore, these functions will be lost whenever the SRC is inhibited or disabled.

9.8.2.3.10 9 and 5 Slit Enable/Inhibit/Select. The 9 and 5 commands are processed identically as shown in Figure 3.9-35. Separate outputs are provided for each side of the redundant variable exposure mechanism control electronics in the associated CEA. Selection circuitry follows the basic concept illustrated in Figure 3.9-21. The 14V WORD implicit bit which turns off both the 9 and 5 slit drives, also inhibits both the 9 and 5 take-ups.

9.8.2.3.11 9 and 5 Slit Bits 1-4. The 9 and 5 slit bit logic circuits shown in Figures 3.9-36 and 3.9-37, respectively, are identical. Separate outputs are provided following the circuit concept of Figure 3.9-20 for each side (A & B) of the variable exposure mechanism control circuit in each camera electronics assembly.

9.8.2.3.12 9/5 Take-Up Enable/Inhibit. The 9 and 5 take-up drives are enabled and inhibited together. The inhibit is controlled by the implicit bit of the ECS 14V WORD, which inhibits the drives each time a 14V WORD is executed. The enable is controlled by normal stored program commands.

*9 AND 5 RUNOUT ON will not enable the 9 and 5 SRC circuits.



* CONTROLLED BY SEVERAL COMMANDS
FOR LOGIC SEE FIGURE 3.9-25

** CONTROLLED BY SEVERAL COMMANDS
FOR LOGIC SEE FIGURE 3.9-24

Figure 3.9-34. SRC, Data Tracks, and I/F Marker Enable/Inhibit/Disable

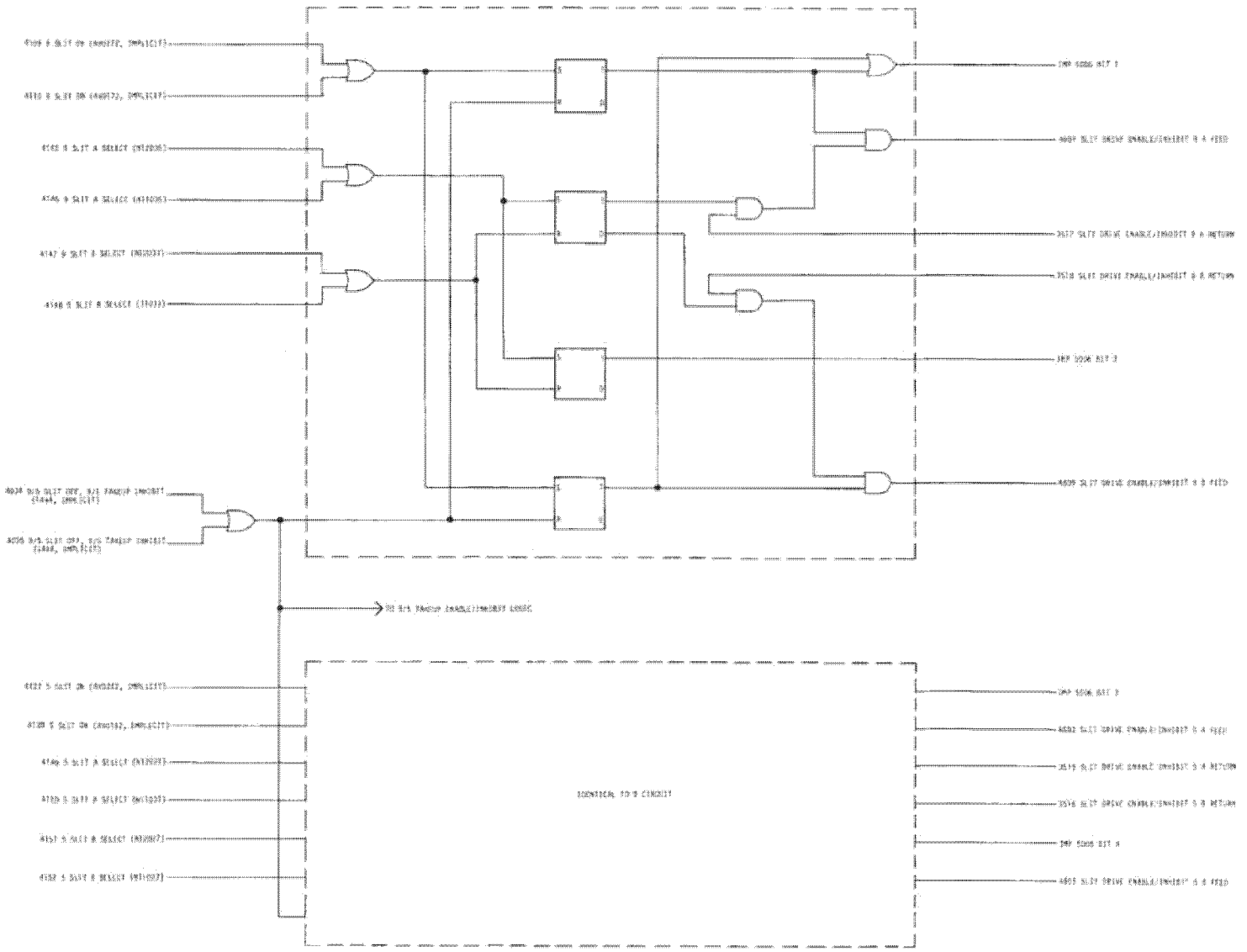


Figure 3.9-35. 9 and 5 Slit Drive Enable/Inhibit/Select

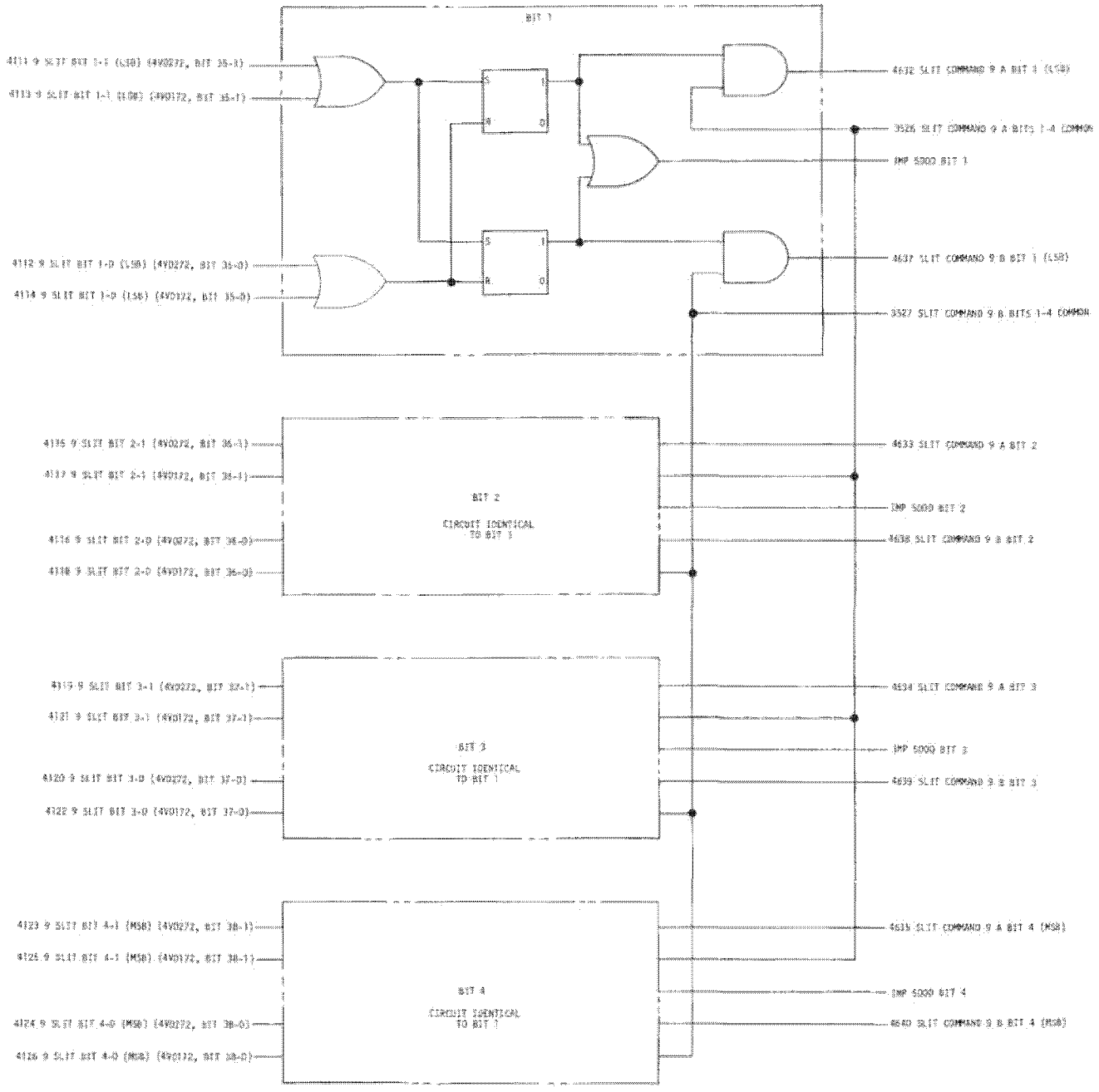


Figure 3.9-36. 9 Slit Bits 1-4

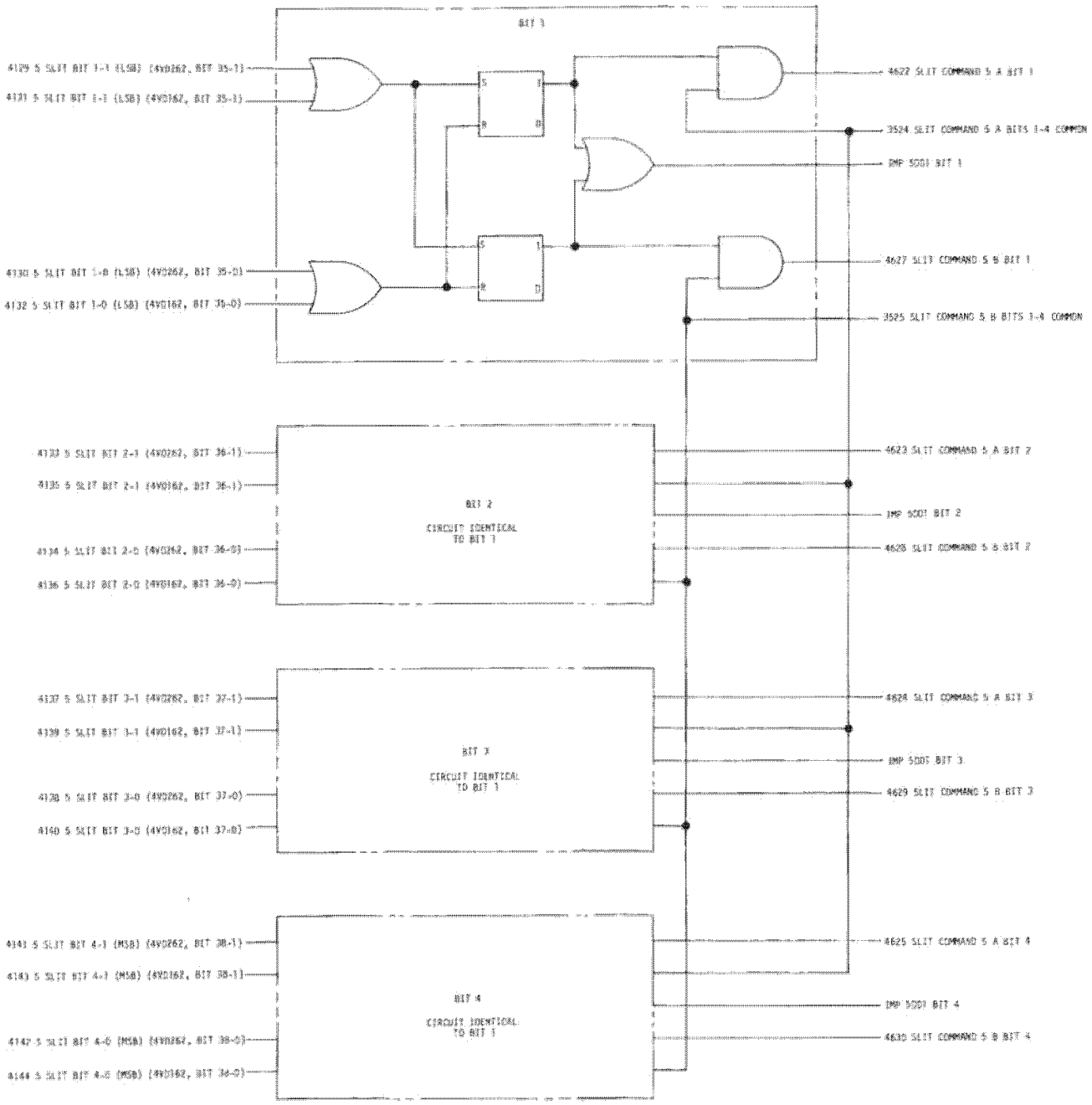


Figure 3.9-37. 5 Slit Bits 1-4

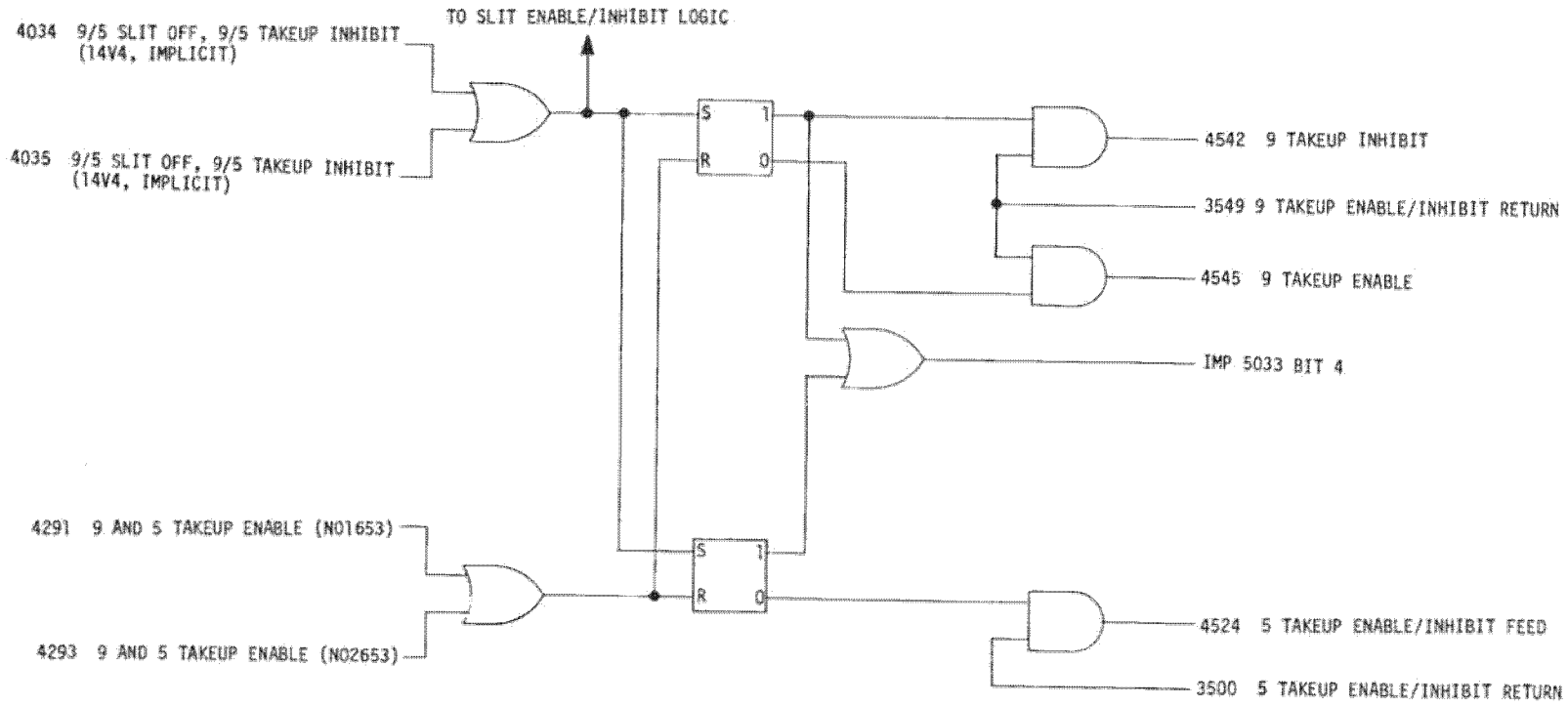
Separate outputs are provided for the 9 and 5 take-ups as shown in Figure 3.9-38. The inhibit override in each subsystem for looper-full or low-tension conditions is located in the film subsystem control unit (film handling electronics (5), film control electronics (9)). For additional detail on these units, refer to Part 3, Section 2.

9.8.2.3.13 Heater Power On/Off. Processing circuitry is the same for all heater branches (1, 2, 4, 5, and 6) and for EPSM 1 and EPSM 2 (see Figure 3.9-39). Optical isolator/driver circuits provide pulsed outputs to the PM and C which turn the given heater circuit power on or off. The output pulse also operates a latching relay within the CP for instrumentation.

Both ECS and MCS commands are available to control the heaters. Redundant ECS commands switch all heater branches on, including EPSM 1 and EPSM 2, and also turn the 5 parking brake power on. Separate ECS commands are used to switch each branch off individually. Three bits of the MCS variable command M6V002YZ control the on/off state of certain branches. Bit 35 controls branches 1, 2, 4, 5, 6 and the 5 parking brake power. Bits 36 and 37 control EPSM 1 and EPSM 2 respectively.

9.8.2.3.14 5 Parking Brake On/Off. The 5 parking brake circuit is identical to the circuits used to operate the heater branches. An optical isolator/driver provides a pulsed output to the PM and C to switch the 5 parking brake power on or off (see Figure 3.9-40). A latching relay in the CP is also controlled by this pulse, and is used to generate the command receipt instrumentation signal.

Lockout circuitry for the 5 parking brake is located in the 5 supply assembly. The 5 operational power actuates a non latching relay in the supply which disables the parking brake (refer to the 5 film handling subsystem logic diagram in Part 3, Section 2). Once actuated, the relay is not released until both 5 OP and 5 parking brake power are off.



3.9-65

Figure 3.9-38. 9/5 Takeup Enable/Inhibit

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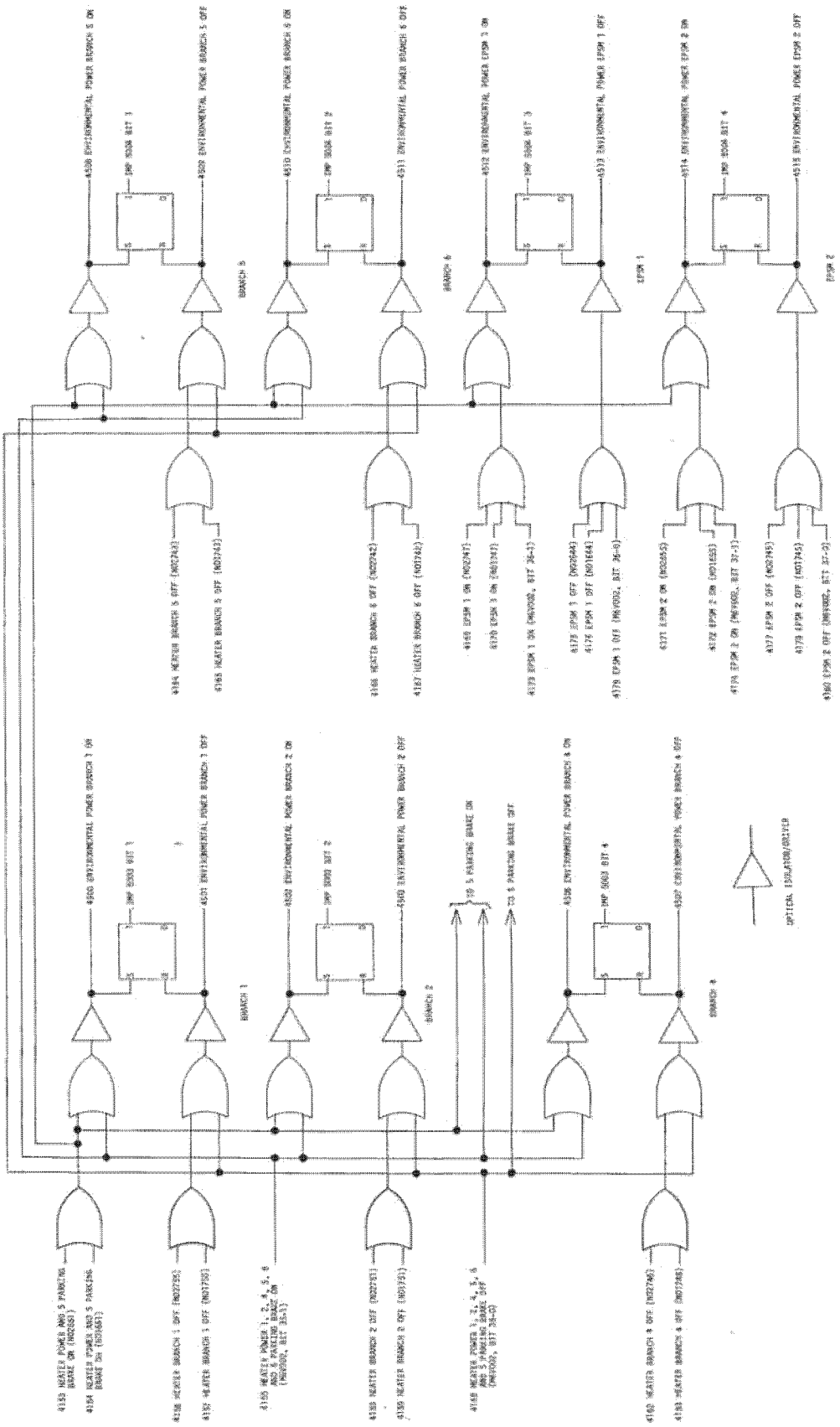

Figure 3.9-39. Heater Branches ON/OFF

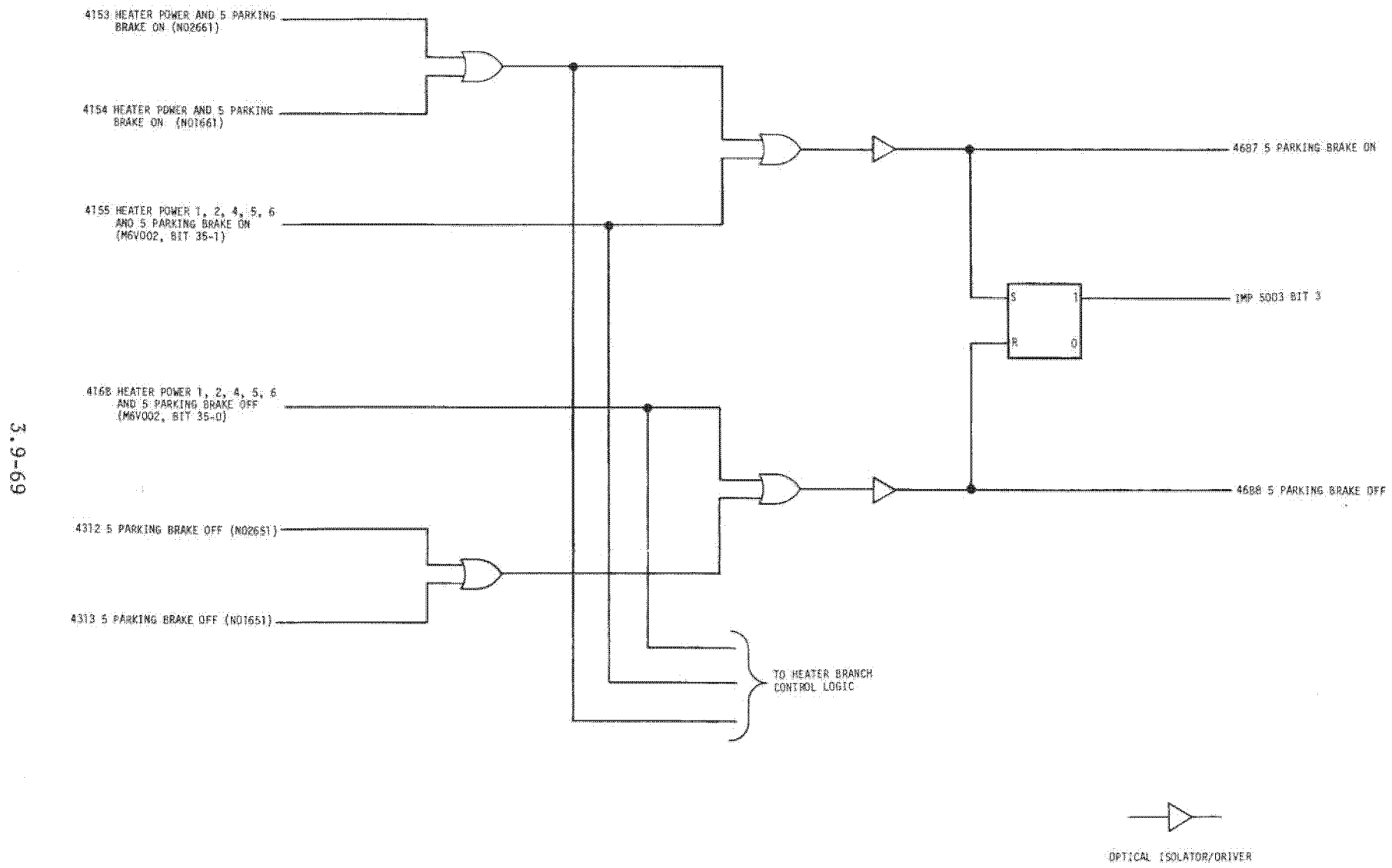

Figure 3.9-40. 5 Parking Brake ON/OFF

9.8.2.3.15 Crab Angle Bits. The four crab angle bits and the crab polarity bit are processed as shown in Figure 3.9-41. The logic 1 input commands for each bit and the crab polarity plus input commands are cross strapped external to the CP to facilitate testing of redundancy. Within the CP, redundant channels are provided for each bit and the outputs logically combined. Channel selection is determined by the CP SELECT commands according to the basic servo mode switch circuit concept illustrated in Figure 3.9-22.

The circuits for crab angle bits 1 through 4 operate by connecting either the logic 1 feed or logic 0 feed to the bit common. The crab polarity circuit operates similarly. However, the polarity common line is powered by a +4.7-volt supply in the crab servo, and, in addition to controlling the polarity state, resets the servo overload relay whenever the polarity is switched (reference Part 3, Section 4).

9.8.2.3.16 Stereo Servo Store/Execute Bits 1 and 2. Stereo angle command bits from the 14V WORD are stored in the CP in parallel redundant relays (Figure 3.9-42). Upon execution of the 13V WORD implicit bit (9/5 cameras OFF, SRC inhibit, stereo execute), pulses are generated within the CP which pass through the contacts of the "store" relays and into the "execute" relays (the standard servo mode switch circuit of Figure 3.9-22), to transfer the 14V WORD command bit information.

The selection relay in the execute section is controlled by the CP A SELECT/CP B SELECT commands. The +4.7-volt level on the stereo angle bit 1 common lead is generated in the stereo servo. Switching bit 1 will reset the overload relay in the servo if it has been tripped (reference Part 3, Section 4).

9.8.2.3.17 Viewport Door OPEN/CLOSE. The viewport door OPEN/CLOSE commands are the only non pyrotechnic related commands which are not processed in the CP. The command pulses pass through the CP and operate latching relays in

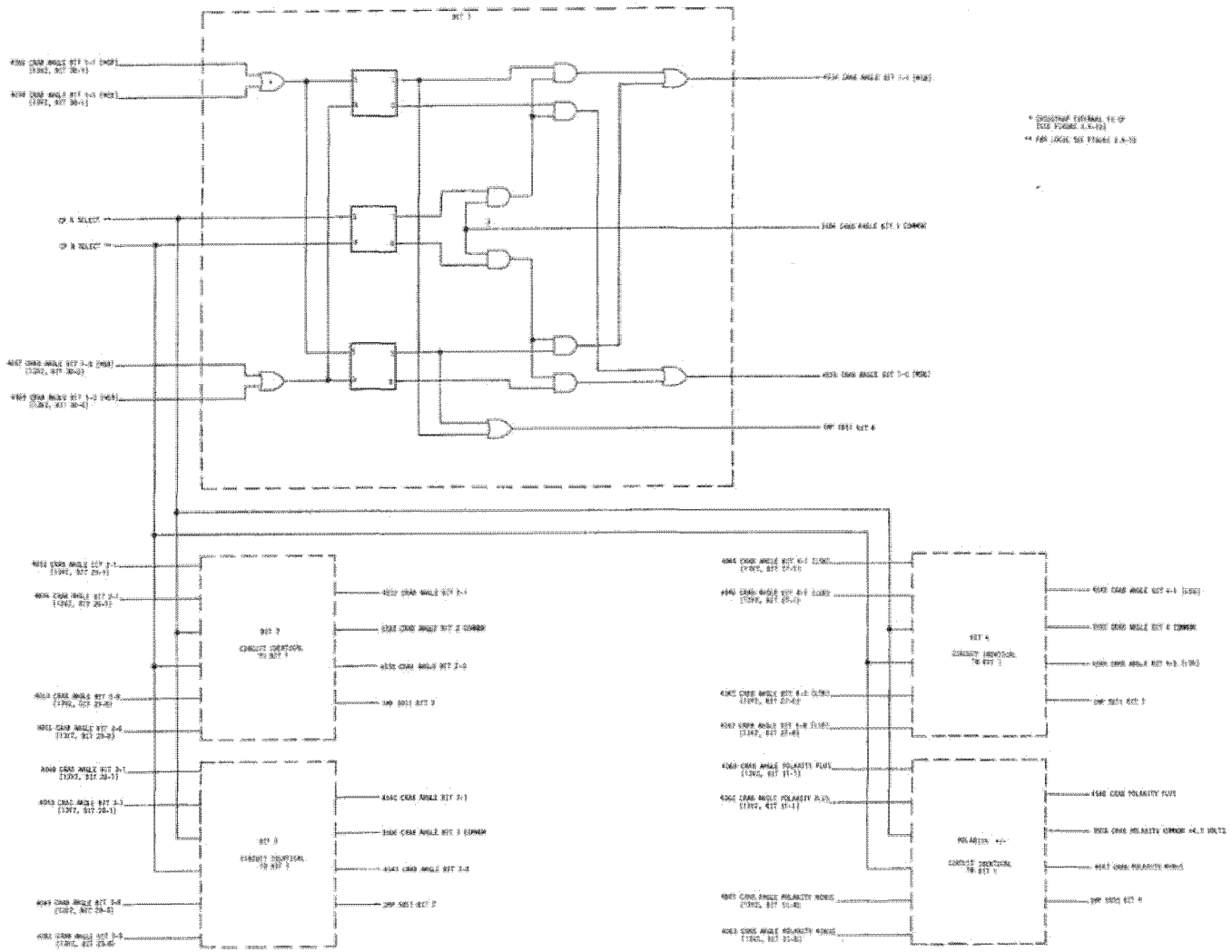

Figure 3.9-41. Crab Angle

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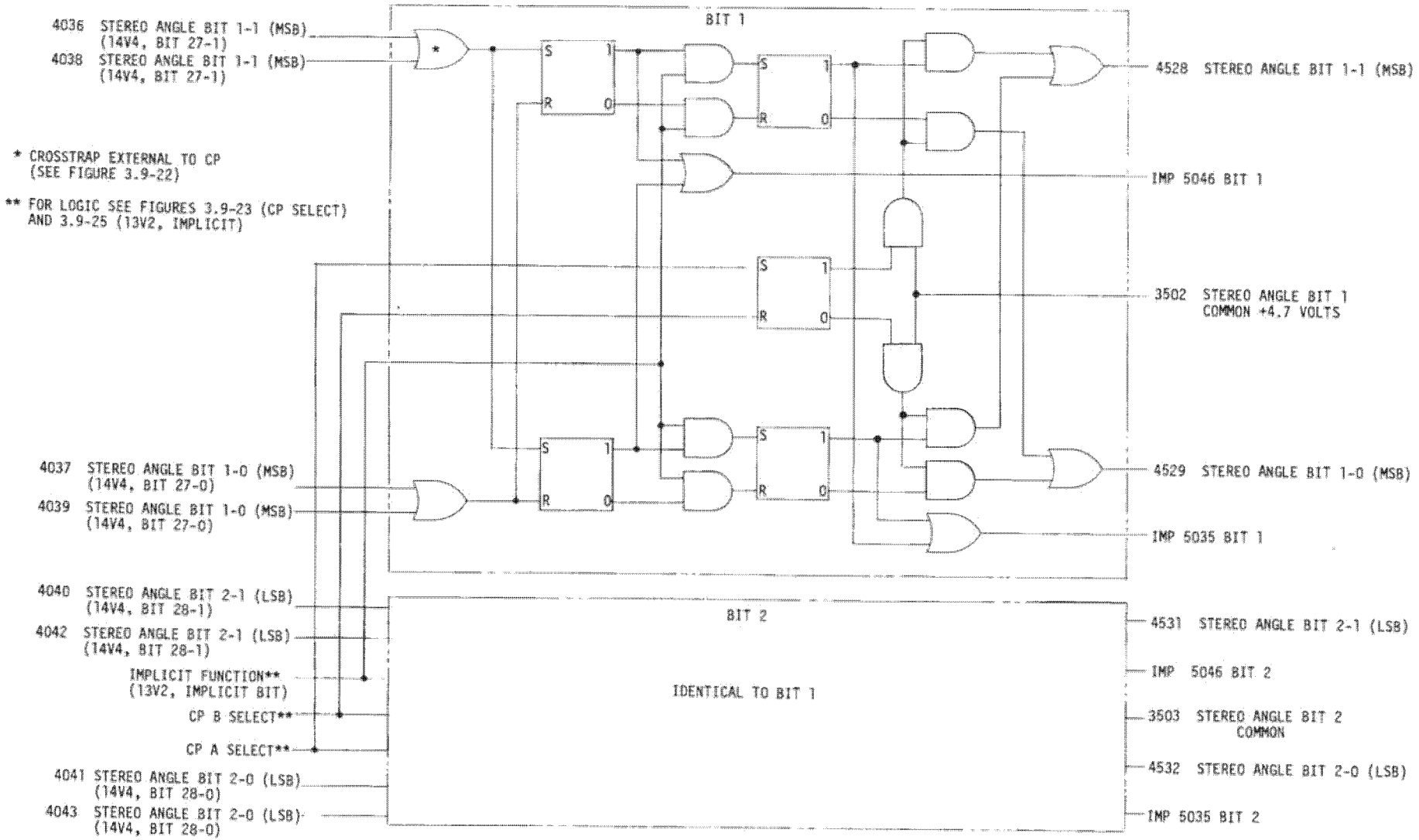


Figure 3.9-42. Stereo Angle Store/Execute

the viewport door electronics unit (reference Part 3, Section 5).

To prevent feedback to the ECS/MCS, the commands are diode decoupled in the CP. The commands also operate a single latching relay in the CP to monitor the receipt of command pulses for telemetry (see Figure 3.9-43).

9.8.2.3.18 DTU 1 and 2 ON/OFF. Separate optical isolator/driver circuits in the CP provide pulsed outputs to the PM and C to turn DTU 1 on or off and DTU 2 on or off. Logic within the PM and C also turns on the instrumentation power supplies whenever either DTU is on. Should both DTU's be commanded ON, the PM and C logic will turn both OFF. Power for one will then turn on when the opposite is turned off. This behavior will continue until both are commanded OFF to restore normal operation. For a logic diagram of the PM and C circuit, refer to Part 3, Section 7.

As seen in Figure 3.9-44, an umbilical command is also provided to turn both DTU's off. This is the only umbilical command which enters the CP.

9.8.2.3.19 Focus Electronics Power ON/OFF. The optical isolator/driver circuits shown in Figure 3.9-45 provide pulsed outputs to the PM and C focus electronics and S1-PRG power switches. Focus electronics and S1-PRG power are turned off by the MCS commands 9 OFF, 5 OFF, and 9/5 OFF which also halt the 9/5 film drives and turn off 9 and 5 operational power.

9.8.2.3.20 Focus Calibrate. The focus calibrate logic is shown in Figure 3.9-46. The command input pulses operate latching relays which control the focus calibrate levels in the focus detection subsystem by connecting or disconnecting the output and return lines. Output bit 1 (instrumentation bit A) controls the Cal signal frequency, and bit 2 (instrumentation bit B) controls the amplitude. Instrumentation bit A is an exception to the general CP design in that it will be in a logic 1 state when the bit 1 output and return are not connected and logic 0 when the two are connected.

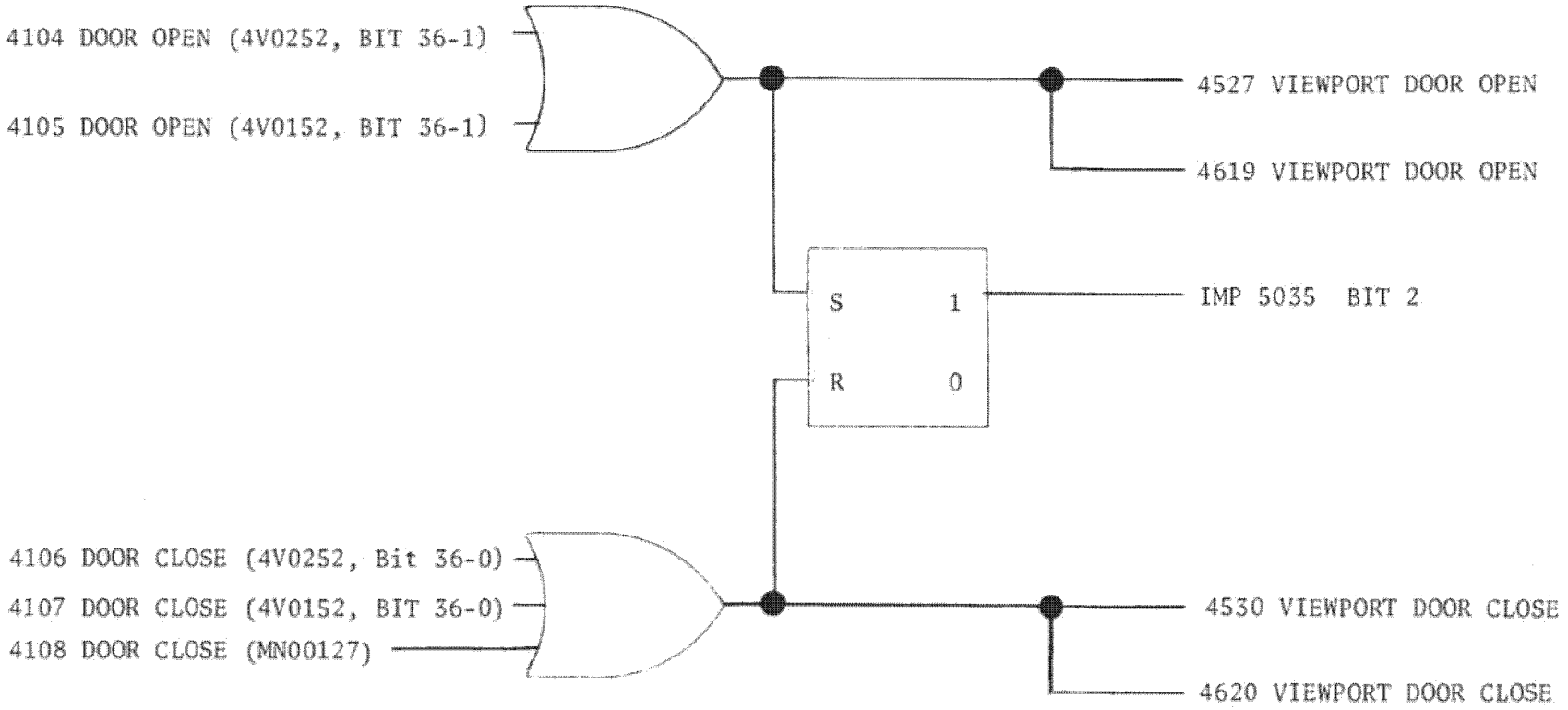


Figure 3.9-43. Viewport Door Open/Close

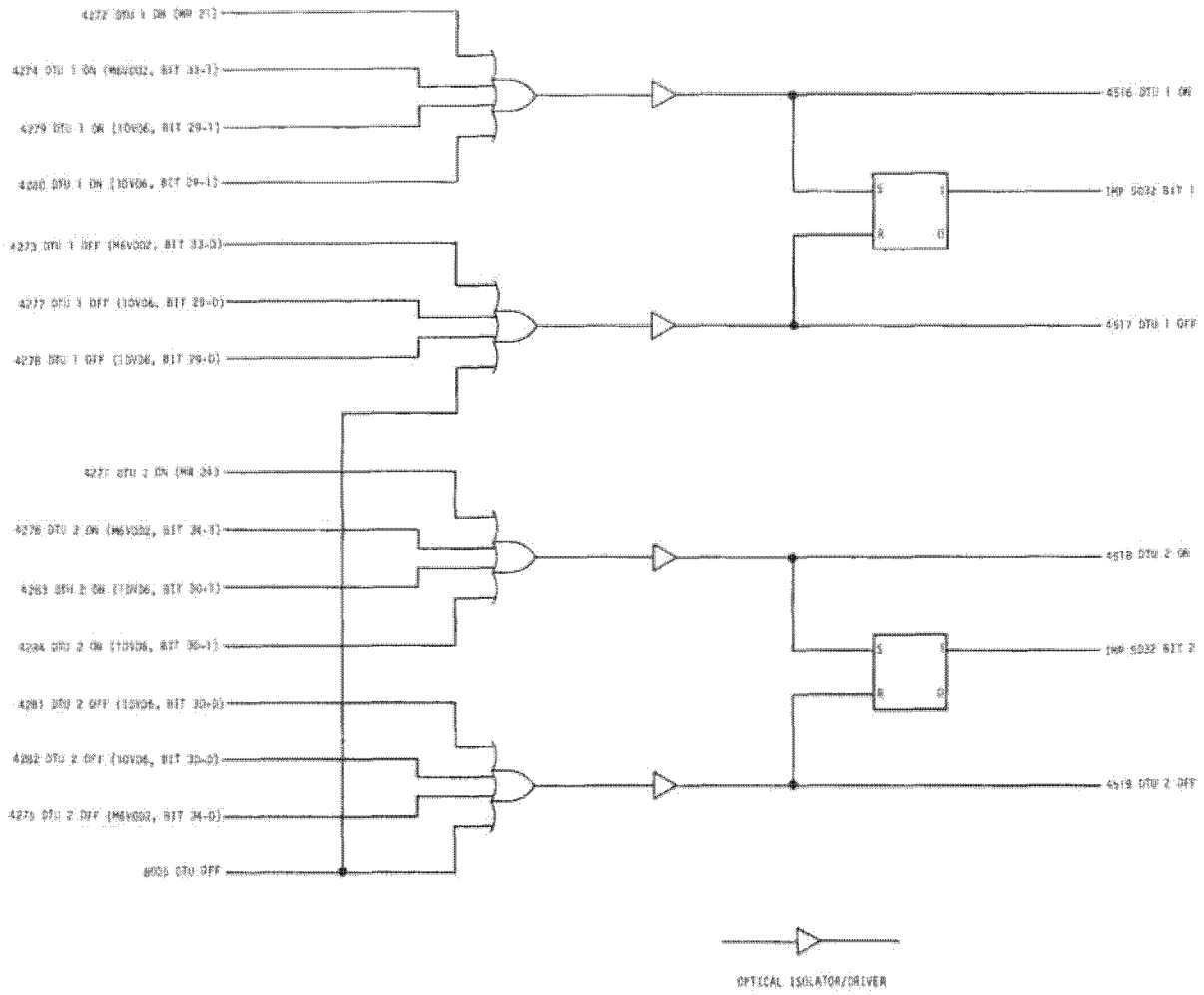


Figure 3.9-44. DTU 1 and 2 ON/OFF

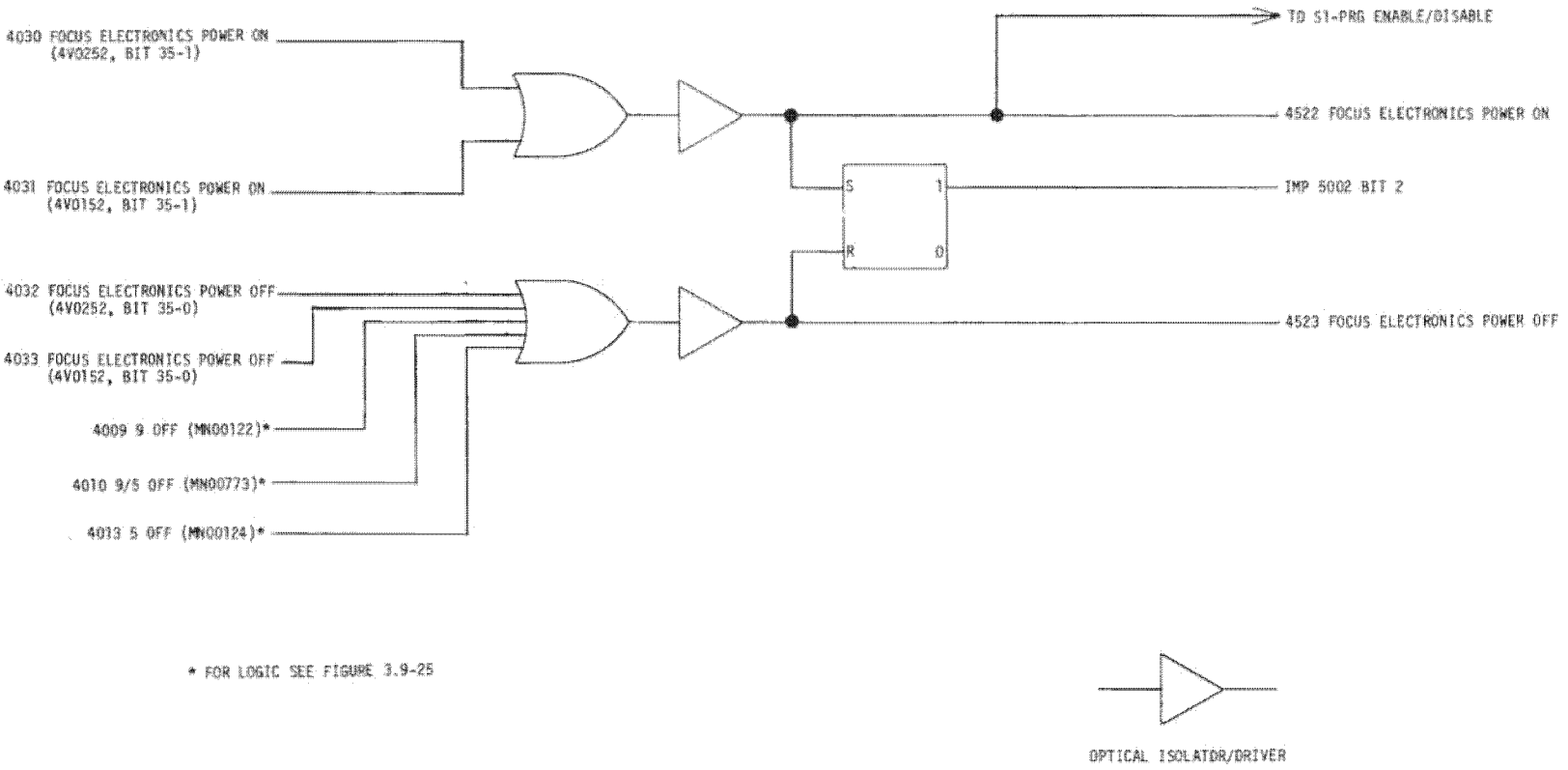
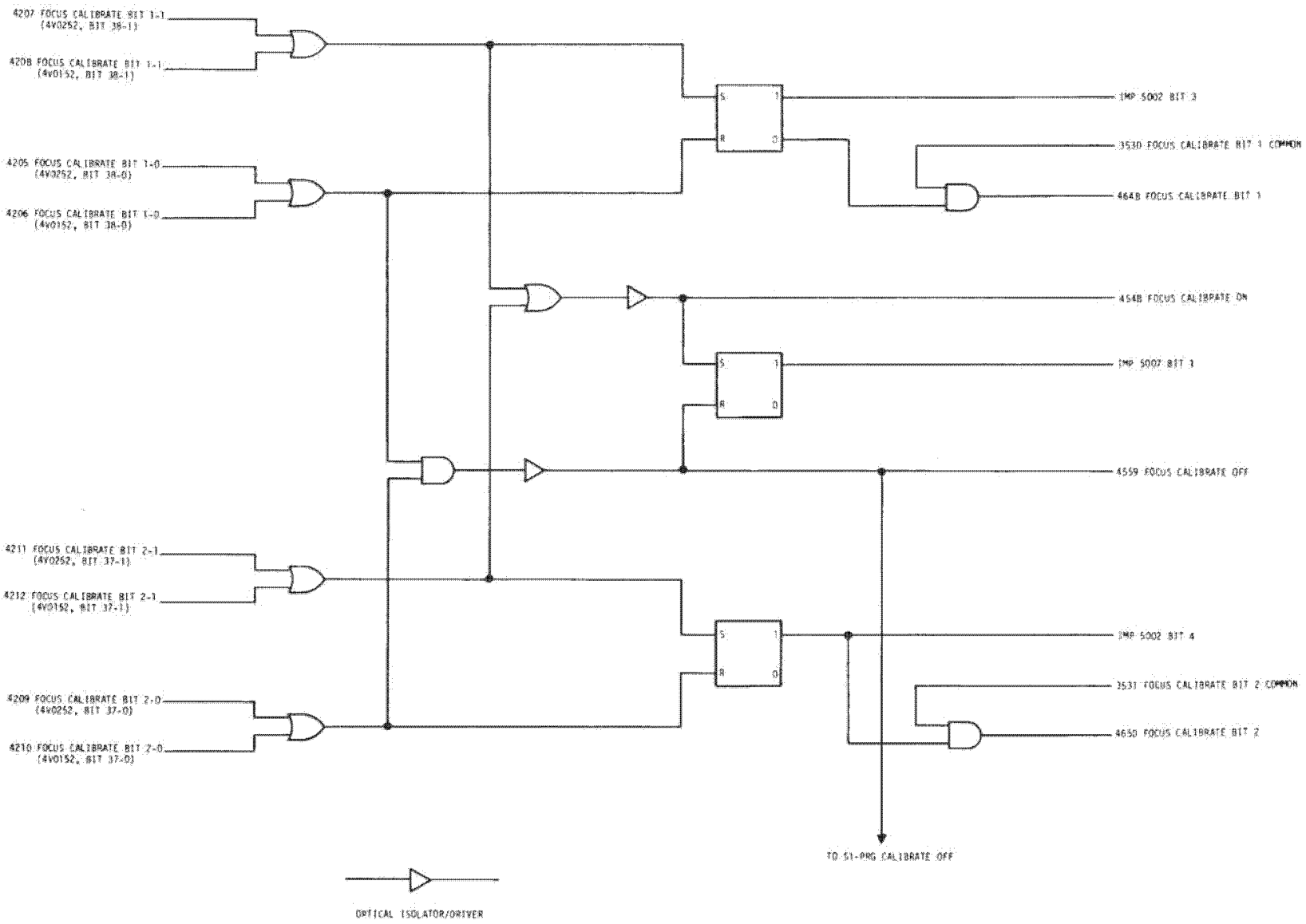


Figure 3.9-45. Focus Electronics Power ON/OFF



3.9-78

Figure 3.9-46. Focus Calibrate

The optical isolators/drivers are employed in a simple decode circuit to turn focus calibrate power off (and also S1-PRG calibrate off) when both focus calibrate bits are logic zeroes, and to turn focus calibrate power on in all other cases.

EAC design changes created a third focus calibrate bit; however, the CP was not modified to provide this command. The CALIBRATION BIT 3 command to the focus sensor is obtained from the second set of relay contacts of the 9 data track switching relay in the camera. The 9 data track relay is operated by the HIGH ALTITUDE/ LOW ALTITUDE SELECT commands.

9.8.2.3.21 S1-PRG Calibrate/Disable. S1-PRG power is turned on in the PM and C in conjunction with the focus electronics power (reference Part 3, Section 7). Power is turned off with FOCUS ELECTRONICS POWER OFF or by S1-PRG DISABLE, which turns off only the S1-PRG power.

S1-PRG CALIBRATE sets a latching relay for calibration which is reset by the focus calibrate power off output pulse. A second relay operated in parallel provides the instrumentation signal (see Figure 3.9-47).

9.8.2.3.22 Select High/Low Altitude. This command configures the PPS/DP EAC for either high-altitude or low-altitude operation. The low-altitude PPS/DP EAC configuration is the same as the pre-EAC configuration. When HIGH ALTITUDE SELECT is commanded, the following changes take place in the PPS/DP EAC:

(a) the FPLL film drives are set to the two high-altitude speed ranges. These speed ranges are one-fourth the speed of the two low-altitude speed ranges.

(b) the four SRC position bits for both 9 and 5 are set to the step 1 command and remain set in step 1 until the LOW ALTITUDE SELECT command is received.

(c) the two data track LEDs are changed to two other LEDs which provide smaller data track marks on the film.

(d) the bandpass center frequency of the focus sensor electronics is changed from 1990 Hz to 830 Hz.

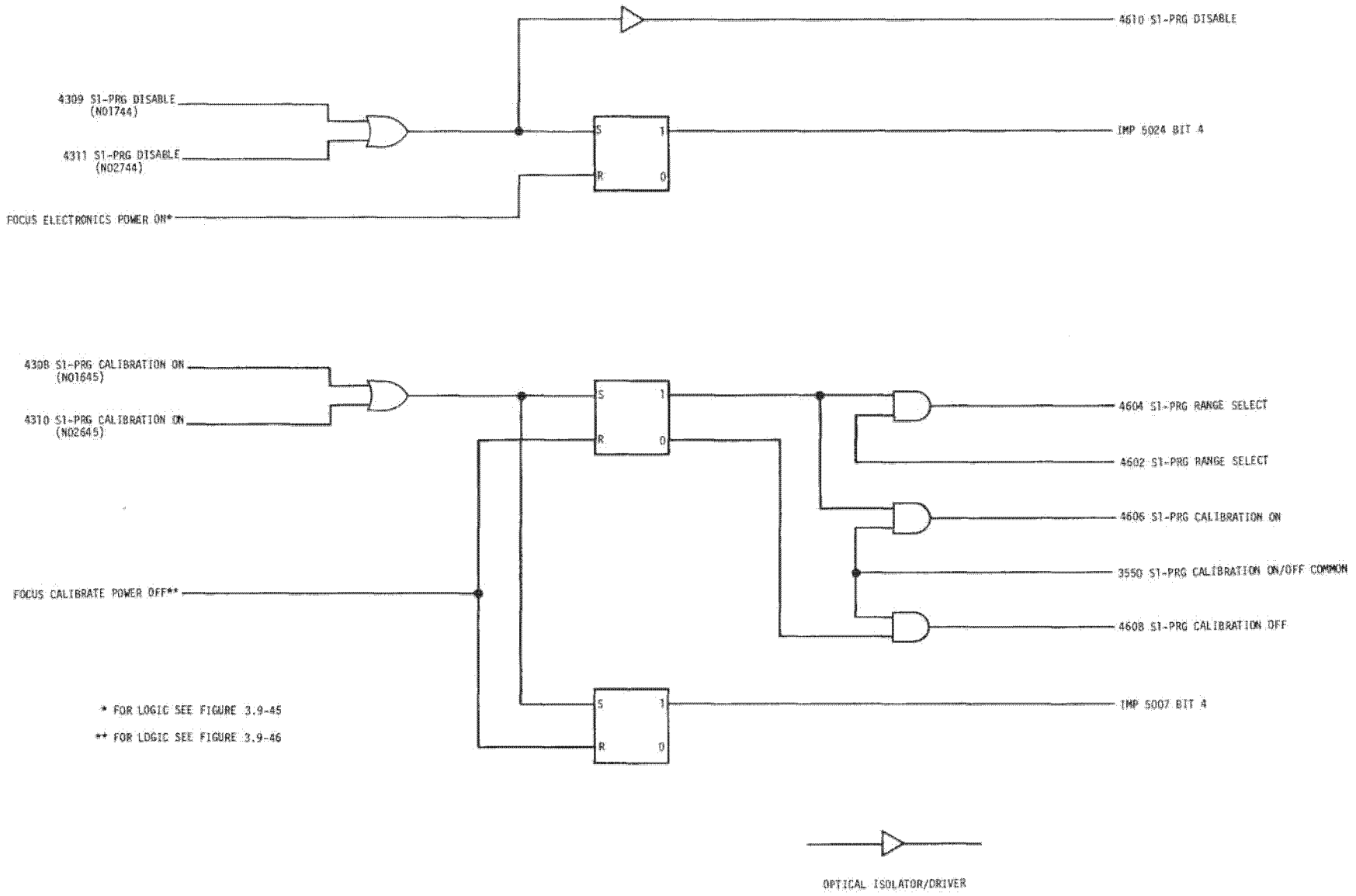


Figure 3.9-47. S1-PRG Calibrate/Disable

(e) the two focus sensor calibrate signals are changed from 1000 Hz and 1600 Hz to 300 Hz and 850 Hz.

The Select-High/Low-Altitude commands are processed by relays and command driver circuits within the CP to provide the following functions:

(1) open or close the SRC 9 and 5 bits 1 - 4 common lines to the 9 and 5 DREAs. The SRC bits 1 - 4 common lines are opened or closed by relay contacts in the CP to provide the proper commands to the 9 and 5 DREAs.

(2) set or reset relays in the 9 and 5 FPLLEs which switch film drive speed ranges. Command driver circuits in the CP generate commands to the FPLLEs.

(3) set or reset relays in the 9 x 5 camera which switch data lamps and provide a focus sensor calibration bit 3 command. Command driver circuits in the CP generate commands to the camera relays.

(4) set or reset relays in the focus sensor which change the pass frequencies of bandpass filters in the focus sensor. Command driver circuits in the CP generate commands to the focus sensor relays.

(5) indicate command status by switching +5 vdc to the D/A converter for IMP 5379.

The logic diagrams describing the Select High/Low Altitude Commands are shown in Figures 3.9-48 and 3.9-49.

9.8.2.3.23 Camera Automatic OFF Enable/Disable. The 9 and 5 camera automatic off circuits (Figure 3.9-50) function identically. Each circuit consists of three relays and associated circuitry which provide a FILM DRIVE OFF command to the FPLLE if the normal CAMERA OFF command is not received. Inputs to the circuit which are processed by the CAMERA AUTOMATIC OFF (CAO) logic circuitry are:

(a) CAMERA ON command

(b) CAO ENABLE command

(c) CAO DISABLE command

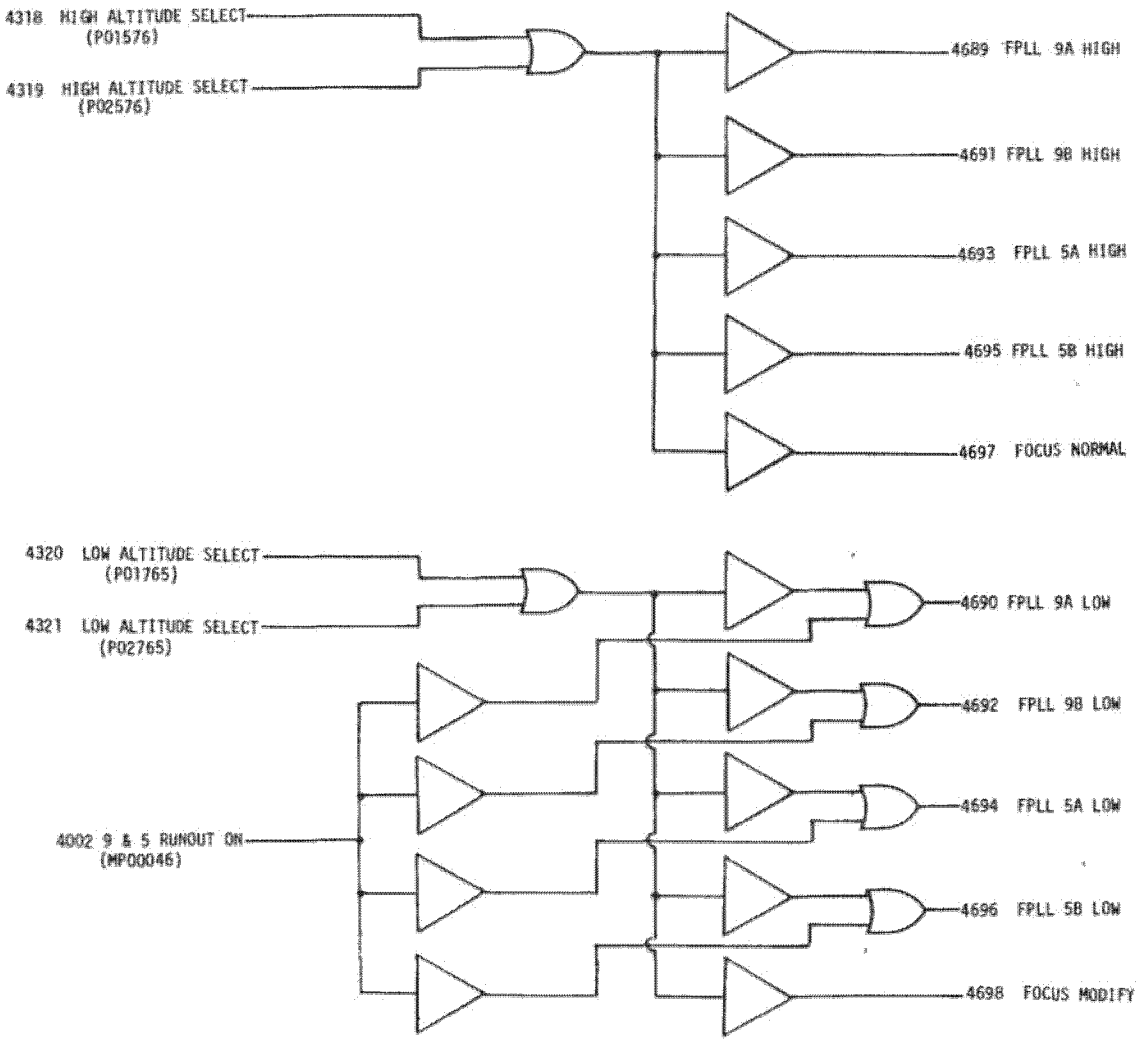


Figure 3.9-48. High/Low Altitude Select FPLL Altitude Range and Focus Normal/Modify

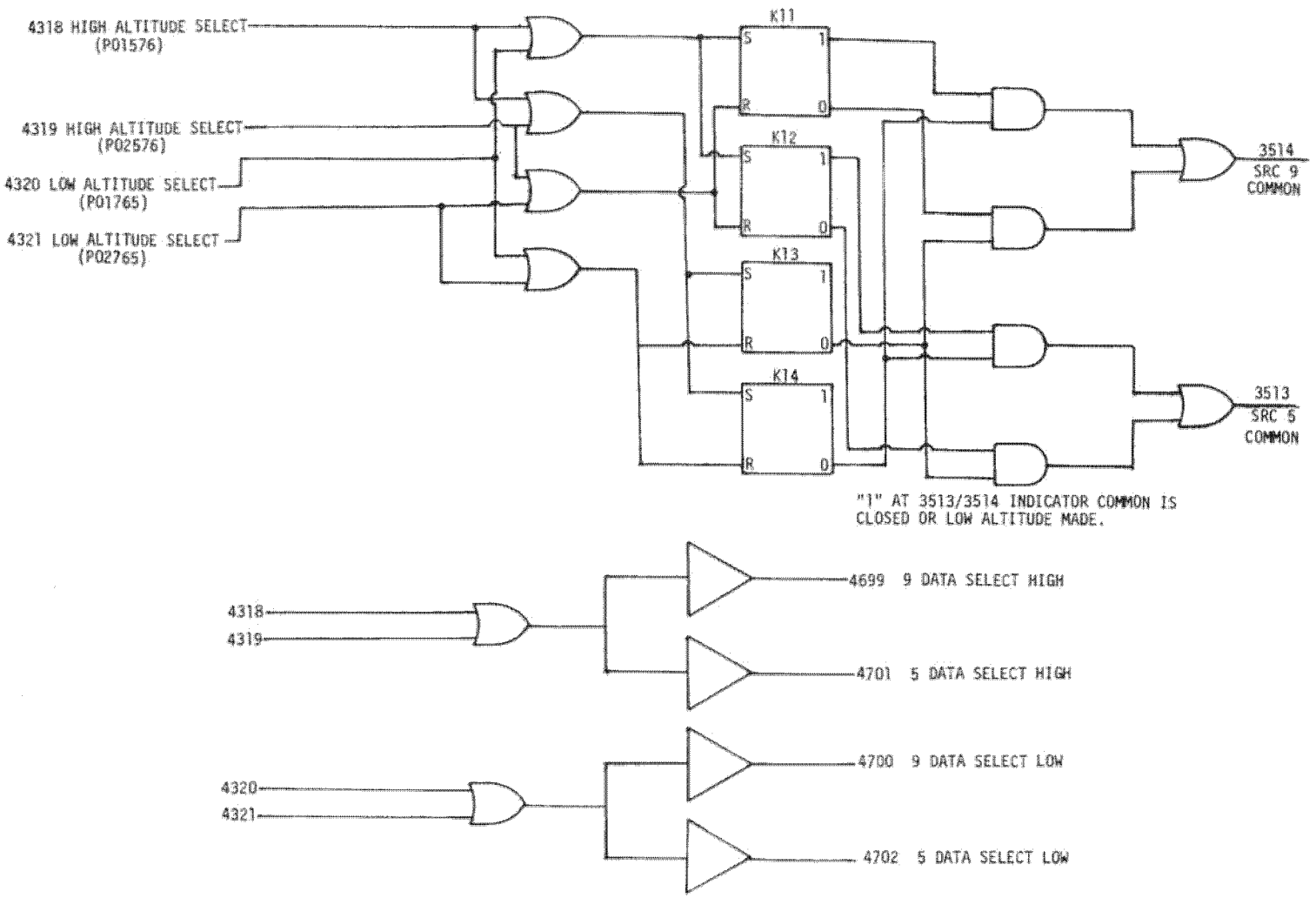


Figure 3.9-49. High/Low Altitude Select SRC Common and Data Lamp Select

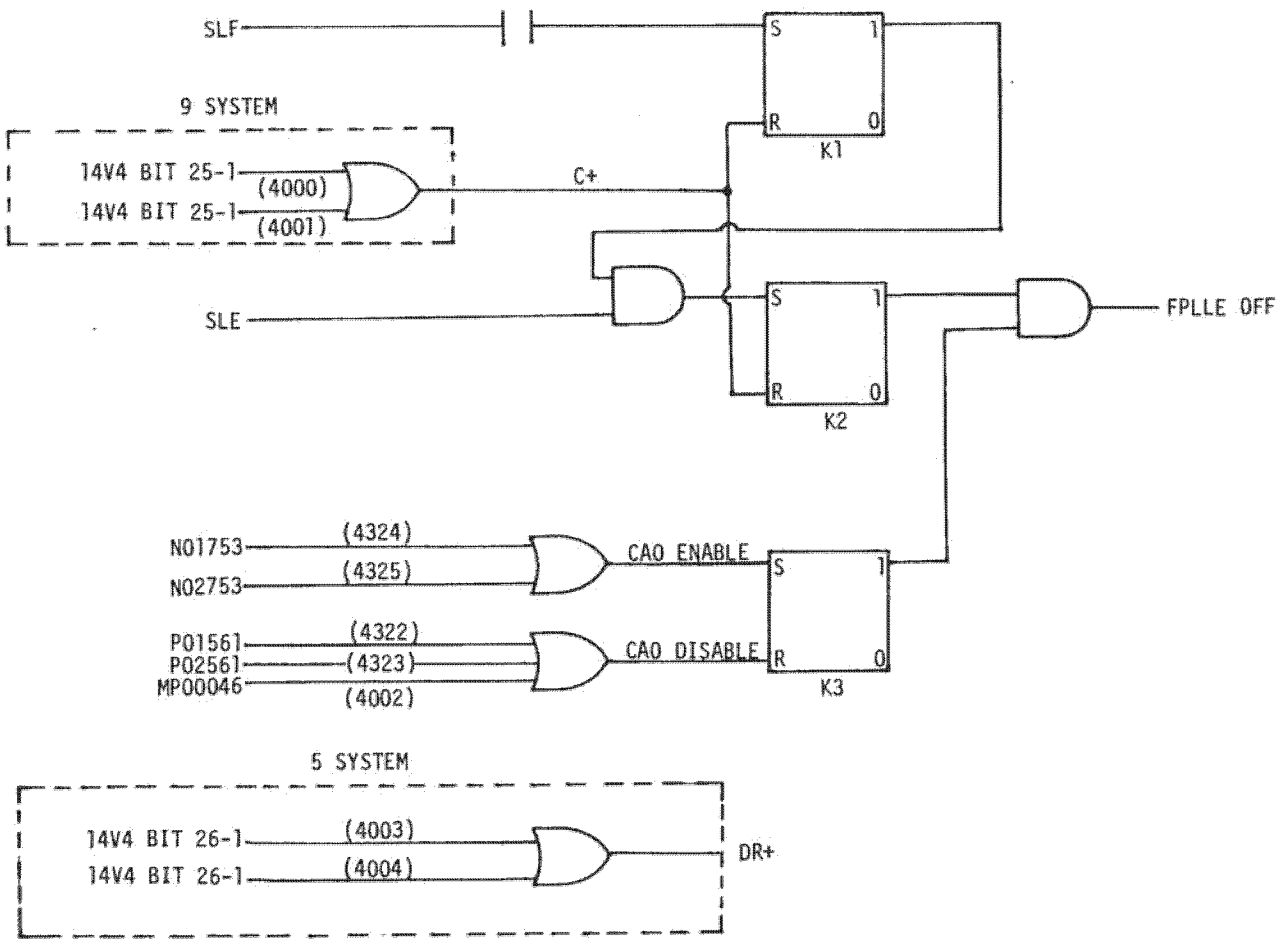


Figure 3.9-50. Camera Automatic Off Logic Diagram

(d) Supply Looper Full signal, and

(e) Supply Looper Empty signal

The last two signals are provided by encoder switch closures in the film handling system. The sequence of operations which will result in the CAO circuit commanding the film drive off is as follows (see Figure 3.9-50):

(1) film drive is initiated by a CAMERA ON (C+) command. This command also resets CAO relays K1 and K2.

(2) if no CAMERA OFF (C-) command is received the supply looper empty encoder switch will close, initiating a take-up cycle of the film handling system. This signal will not change the state of the CAO logic since relay K1 is still reset.

(3) operation of the film handling system will cause the supply looper full (SLF) encoder switch to close, terminating the take-up cycle. This signal also sets CAO relay K1, resulting in a change in state of the CAO logic.

(4) if no C- command is received, the supply looper empty (SLE) encoder switch will close again. If no C+ command has been received since K1 was set (in step 3 above), the SLE signal, with K1 in the set state, will cause relay K2 to be set. This generates the CAMERA AUTOMATIC OFF command if the CAO circuit is enabled.

(5) normal operation of the film drive system returns with the next C+ command, since the C+ command resets both relays K1 and K2.

It should be noted that the 9 AND 5 RUNOUT ON command (MP00046) disables the CAO circuits, permitting proper operation of the runout function.

9.9 Command Processor Instrumentation

All instrumentation in the CP makes use of the standard circuit illustrated in Figure 3.9-19. Each point accepts up to four discrete inputs and produces a single multi-level output which represents the state of each input. A summary of the command processor instrumentation points is presented in Table 3.9-4.

TABLE 3.9-4

COMMAND PROCESSOR INSTRUMENTATION

IMP	Title	Description	Power
5000	9 Slit Bits 1,2,3,4	Latching relays tracking the command input relays of the command processor monitor the receipt of commands from the satellite control section and feed either 0.0v or 5.0v to an integrated circuit D/A converter. Four relays and one 4-bit D/A converter form the IMP. Output occurs in sixteen discrete steps ranging from 0.25v to 4.75v in 0.3v increments: Bit 1 (LSB) = 9 Slit Bit 1 (LSB) Bit 2 = 9 Slit Bit 2 Bit 3 = 9 Slit Bit 3 Bit 4 (MSB) = 9 Slit Bit 4 (MSB)	+5/±15 vdc
5001	5 Slit Bits 1,2,3,4	Similar to IMP 5000: Bit 1 (LSB) = 5 Slit Bit 1 (LSB) Bit 2 = 5 Slit Bit 2 Bit 3 = 5 Slit Bit 3 Bit 4 (MSB) = 5 Slit Bit 4 (MSB)	+5/±15 vdc
5002	Cal On/Off, FEP On/Off Cal Bit A/$\bar{A}$, Cal Bit B/$\bar{B}$	Similar to IMP 5000: Bit 1 (LSB) = Cal On/Off Bit 2 = FEP On/Off Bit 3 = Cal Bit A/$\bar{A}$ (Command Bit 38; Bit 1 in the Focus Electronics) Bit 4 (MSB) = Cal Bit B/$\bar{B}$ (Command Bit 37; Bit 2 in the Focus Electronics)	+5/±15 vdc

TABLE 3.9-4

IMP	Title	Description	Power
5003	Environmental Branches 1, 2, and 4, and 5 Parking Brake On/Off	Similar to IM[illegible] Bit 1 (LSB) = [illegible] 1 On/[illegible] Bit 2 = Env. br[illegible] 2 [illegible] Bit 3 = [illegible] brak[illegible]/Off Bit 4 (MSB) = En[illegible] ch 4 [illegible]/Off	+5/±15 vdc
5004	Environmental Branch 5, 6 EPSM 1, EPSM 2 On/Off	Similar to IMP 5000: Bit 1 (LSB) = Env. b[illegible]ch [illegible]/Off Bit 2 = Env. branch [illegible]/Off Bit 3 = EPSM 1 On/Off Bit 4 (MSB) = EPSM 2 On/Off	+5/±15 vdc
5005	9 FPLLE Select Side A, 9 FPLLE Select Side B, 5 FPLLE Select Side A, 5 FPLLE Select Side B	Similar to IMP 5000: Bit 1 (LSB) = 9 FPLL[illegible]ect Side A Bit 2 = 9 FPLLE Select Side B Bit 3 = 5 FP[illegible]lect Side A Bit 4 (MSB) = [illegible]	+5/±15 vdc
5006	9 Slit Enable/Inhibit 9 Slit Select A/B, 5 Slit Enable/Inhibit 5 Slit Select A/B	Similar to IMP 5000: Bit 1 (LSB) = [illegible]nable/Inhibit Bit 2 [illegible] Bit 3 [illegible]/Inhibit Bit 4 (MSB) = [illegible] A/B	+5/±15 vdc
5007	5 Focus Drive Enable/ Inhibit, 5 Minus/Stop, 5 Plus/Stop, S1-PRG Cal On/Off	Similar to IMP [illegible] Bit 1 (LSB [illegible] Enable/Inhibit Bit 2 Bit 3 Bit 4 (MSB [illegible]/Off	+5/±15 vdc

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TABLE 3.9

IMP	Title	Description	Power
5011	Crab Bits 1,2,3,4	Similar to [illegible] Bit 1 (LSB) = 1 = LSB (13V WORD Bit 27) Bit 2 = 3 (13V WORD Bit 28) Bit 3 = 2 (13V WORD Bit 29) Bit 4 (MSB) = 4 = MSB (13V WORD Bit 30)	+5/±15 vdc
5024	9 Focus Drive Enable/ Inhibit, 9 Minus/Stop, 9 Plus/Stop, S1-PRG Disable/Enable	Similar to [illegible] Bit 1 (LSB) = Focus Drive Enable/Inhibit Bit 2 = [illegible] Bit 3 = [illegible] Bit 4 (MSB) = S1-PRG Disable/Enable	+5/±15 vdc
5027	FDS Bits 1,2,3,4	Similar to IMP [illegible] Bit 1 (LSB) = [illegible] Bit 2 = [illegible] Bit 2 Bit 3 = FDS Bit 3 Bit 4 (MSB) = [illegible]	+5/±15 vdc
5028	FDS Bits 5,6,7,8	Similar to IMP [illegible] Bit 1 (LSB) = FDS Bit 5 Bit 2 = [illegible] Bit 3 = [illegible] Bit 4 (MSB) = [illegible]	+5/±15 vdc
5029	9 Camera ON/OFF, 5 Camera ON/OFF, 9 OP ON/OFF, 5 OP ON/OFF	Similar to [illegible] Bit 1 = [illegible] Bit 2 = [illegible] Bit 3 = [illegible] Bit 4 = [illegible]	+5/±15 vdc

TABLE 3.9-4 (CONT'D)

IMP	Title	Description	Power
5032	PCM 1 ON/OFF,* PCM 2 ON/OFF, FDS Bits 9,10	Similar to IMP 5000: Bit 1 (LSB) = PCM 1 ON/OFF Bit 2 = PCM 2 ON/OFF Bit 3 = FDS Bit 9 Bit 4 (MSB) = FDS Bit 10 (LSB)	+5/±15 vdc
5033	9 NPA Prime/BU 5 NPA Prime/BU, T/U Enable/Inhibit	Similar to IMP 5000; the output ranges from 0.25v to 1.15v and from 2.65v to 3.55v in 0.3v increments Bit 1 (LSB) = 5 NPA Prime/BU Bit 2 = 9 NPA Prime/BU Bit 3 = No Connection Bit 4 (MSB) = T/U Enable/Inhibit	+5/±15 vdc
5035	Stereo Drive Transfer Bit 1,2, Viewport Door Open/Close, Crab Polarity +/-	Similar to IMP 5000: Bit 1 (LSB) = Stereo Drive Transfer Bit 1 (14V WORD Bit 27) (MSB) Bit 2 = Stereo Drive Transfer Bit 2 (14V WORD Bit 28) (LSB) Bit 3 = Viewport Door Open/Close Bit 4 (MSB) = Crab Polarity +/- (13V WORD Bit 31)	+5/±15 vdc

*PCM (pulse code modulation) is an unclassified term for digital telemetry unit.

TABLE 3.9-4 (CONT'D)

IMP	Title	Description	Power
5036	9 OPS Counter Bits 1,2,3 Spare	Similar to IMP 5000; a counter circuit feeding the D/A converter increments at each 9 film drive OFF command that has been preceded by a 9 film drive ON command (14V WORD): Bit 1 (LSB) = No Connection Bit 2 = 9 OPS Counter Bit 1 Bit 3 = 9 OPS Counter Bit 2 Bit 4 (MSB) = 9 OPS Counter Bit 3 The circuit is a binary counter running from 0 to 7, resetting to 0 at the next pulse, and continuing. The IMP output ranges from 0.25v to 4.45v in 0.6v increments.	+5/±15 vdc
5037	5 OPS Counter Bits 1,2,3, Spare	Similar to IMP 5036; counts the number of 5 film drive ON/OFF command pairs: Bit 1 (LSB) = No Connection Bit 2 = 5 OPS Counter Bit 1 Bit 3 = 5 OPS Counter Bit 2 Bit 4 (MSB) = 5 OPS Counter Bit 3	+5/±15 vdc
5046	Stereo Bit 1 Stored, Stereo Bit 2 Stored, CP Select A/B, FPLLE Speed Range High/Normal	Similar to IMP 5000: Bit 1 (LSB) = Stereo Bit 1 Stored (14V WORD Bit 27) (MSB) Bit 2 = Stereo Bit 2 Stored (14V WORD Bit 28) (LSB) Bit 3 = CP Select A/B Bit 4 (MSB) = FPLLE Speed Range High/Normal	+5/±15 vdc
5047	Data Tracks and SRC, 9 Enable/Inhibit 9 Enable/Disable, 5 Enable/Inhibit, 5 Enable/Disable	Similar to IMP 5000: Bit 1 (LSB) = 9 Enable/Inhibit Bit 2 = 9 Enable/Disable Bit 3 = 5 Enable/Inhibit Bit 4 (MSB) = 5 Enable/Disable	+5/±15 vdc

IMP	Title	Description	Power
5379	9 CAMERA AUTOMATIC OFF OFF/NORMAL, 5 CAMERA AUTOMATIC OFF OFF/NORMAL, CAMERA AUTOMATIC OFF ENABLE/DISABLE, ALTITUDE SELECT HI/LOW	Similar to IMP 5000	+5/±15 vdc

9 Camera Auto OFF/Normal	Bit 1 (LSB)	= 9 Camera Auto OFF/Normal
5 Camera Auto OFF/Normal	Bit 2	= 5 Camera Auto OFF/Normal
Camera Auto OFF Enable/Disable	Bit 3	= Camera Auto OFF Enable/Disable
Select High/Low Altitude	Bit 4 (MSB)	= Select High/Low Altitude

3.9-91

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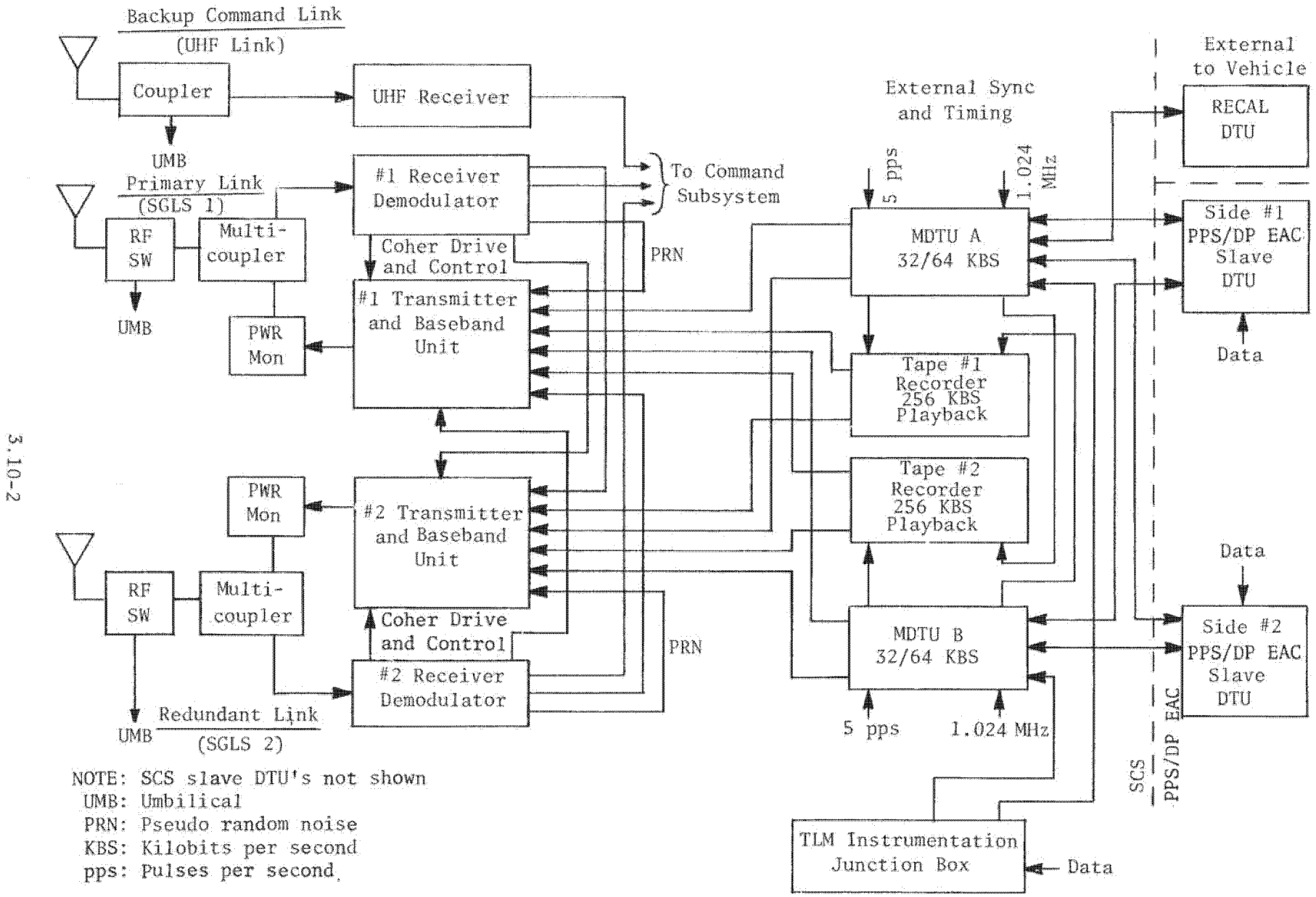
10.0 INSTRUMENTATION AND TELEMETRY

Instrumentation sensors throughout the vehicle monitor photographic payload section/dual platen extended altitude capability (PPS/DP EAC) related functions. This information is then processed through the telemetry subsystem and eventually transmitted to the ground for analysis. Together, the instrumentation and telemetry subsystems form the overall on-orbit monitoring system of the PPS/DP EAC, and for some portions of this section, will be treated collectively rather than described individually.

Components of the instrumentation subsystem include the instrumentation sensors, the instrumentation power supplies, and the instrumentation processor (IP). The telemetry subsystem includes slave DTU's* 1 and 2, master DTU's A and B, tape recorders 1 and 2, the transmitters, and two additional slave DTU's for the satellite control section (SCS). Of these, only slave DTU's 1 and 2 are contained within the PPS/DP EAC. All other components of the telemetry subsystem are located in the SCS. An additional slave DTU, the RECAL** unit, which is used only for testing, is connected external to the PPS/DP EAC, and is removed prior to launch.

Figures 3.10-1 and 3.10-2 describe the telemetry and instrumentation subsystems for the satellite. Note that the major portion of Figure 3.10-1 illustrates components of the telemetry subsystem which are not the responsibility of BIF-008. It is presented here for informational purposes only. The output connectors on Figure 3.10-2 labeled test point (TSP)

* Digital Telemetry Unit
**Remote Electrical Checkout Via Air Link



NOTE: SCS slave DTU's not shown
UMB: Umbilical
PRN: Pseudo random noise
KBS: Kilobits per second
pps: Pulses per second

Figure 3.10-1. PSV Telemetry Subsystem

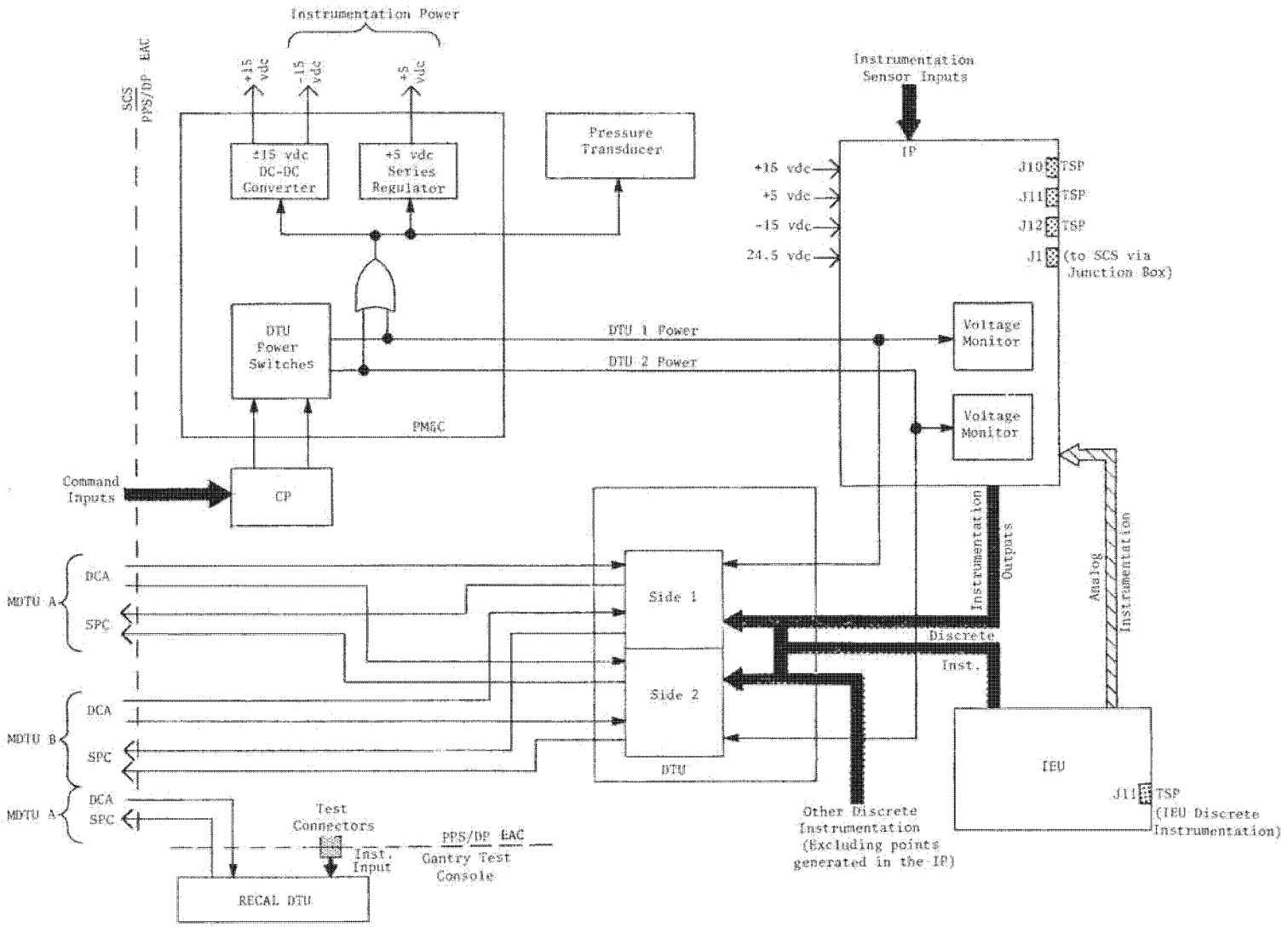


Figure 3.10-2. PPS/DP EAC Instrumentation and Telemetry Subsystem

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and umbilical monitoring point (BIL) allow hardline monitoring of most instrumentation points rather than analyzing the digitized output from the DTU. These points are used during testing both at BIF-008 facilities and at the launch pad.

10.1 Instrumentation

Within the PPS/DP EAC, the design of all instrumentation attempts to isolate the sensors from the functions they monitor. No single point failure mode exists in the instrumentation subsystem that would affect the operation of the vehicle. As an additional benefit, this isolation, through the use of separate power supplies for instrumentation, and a separate instrumentation unipoint ground in the IP, reduces electrical noise in the data signals.

The placement of sensors in the PPS/DP EAC follows the general guideline of providing maximum data return for day-to-day monitoring, and for failure analysis. In addition to tracking the operation of the various subsystems, monitoring power drain, rates of movement, etc., several points have been assigned to monitor such PPS/SCS electrical interface requirements as power levels and command receipt.

All functions defined as critical have redundant instrumentation sensors associated with them. This not only achieves greater system reliability, but also provides an additional measure of confidence in the data received. Where possible, redundant points are powered from separate supplies (+5 or +15 volts) to prevent the failure of one supply from eliminating the monitoring of a critical function.

10.1.1 Instrumentation Signal Characteristics

PPS/DP EAC instrumentation consists of both analog and discrete monitors. Analog signals are those whose voltages are encoded by the DTU at the level of

input. Discrete signals are those included by the DTU as bilevel inputs which are either in a high state (high input voltage) or a low state (low input voltage).

The voltage limits and impedance requirements for both analog and discrete points are controlled by the input requirements of the slave DTU. All instrumentation monitoring points (IMP's), either upon generation or through additional processing in the IP, must meet these requirements as listed:

(1)	Analog instrumentation:	
	a) Operating range	0 to 5.06 volts
	b) Output resistance	0 to 10 KΩ
	c) Shunt capacitance	less than 2000 pf or greater than 0.1 μf
(2)	Discrete instrumentation:	
	a) Operating range	-4 to +33 volts, as follows:
	Logic 0	-4 to +1 volts
	Logic 1	+3 to +33 volts
	b) Output resistance	50 KΩ, or less
	c) Shunt capacitance	Less than 2000 pf, or greater than 0.1 μf

10.1.2 Test Points (TSP's) and Umbilical Monitoring Points (BIL's)

Hardline monitoring of most instrumentation points is available at the test connectors located on the IP and on the initiator electronics unit (IEU). These outputs are in parallel with the IMP outputs to the DTU, and are isolated by 27 KΩ of series resistance in each line. The hardlines make it possible to obtain constant readings of the vehicle sensors, avoiding the restrictions of DTU sampling rates and analog-to-digital conversion of the signals. A handful of selected points, including one special point measuring the conditioned air inlet temperature at the launch pad, also have parallel hard-

line outputs (BIL's) through a vehicle umbilical connector, and can be monitored up to the time of launch. Unlike other BIL points, the temperature sensor near the umbilical conditioned air inlet has no corresponding flight instrumentation output.

10.2 Instrumentation Processor

The IP provides conditioning of instrumentation signals as required to meet the input requirements of the DTU, and distributes these signals to the DTU, and to the IP hardline test connectors. The IP also generates a limited number of instrumentation points internally which meet the DTU input requirements and are distributed in the same fashion as other IP instrumentation signals. Not every instrumentation point passes through the IP. However, all analog instrumentation points are routed through the IP prior to input to the DTU. For discrete instrumentation, only selected points of those initially generated in the IP have hardline TSP outputs in the IP. All other discrete instrumentation is routed directly to the DTU.

10.2.1 IP Mechanical

The IP is illustrated in Figure 3.10-3. The unit is approximately 11 3/4" x 12" x 6¼, excluding mounting feet, and weighs just under 15 pounds. It is located on the -Y side of the film supply enclosure attached to rails at Stations 45.3 and 59.6 (reference Part 3, Section 1). Components of the IP include 17 circuit board assemblies, two module assemblies, the patchboard assembly, and 18 electrical connectors, 6 of which are internal. The board and module assemblies are assigned according to Table 3.10-1. The patchboard is a removable subassembly that provides a flexible means to connect additional output signals, disconnect output signals, or reorder the existing output signal lines. This is accomplished by removing the patchboard and altering the point-to-point wiring between the IP output connectors and their associated internal connectors. Output connector J2 is wired to inter-

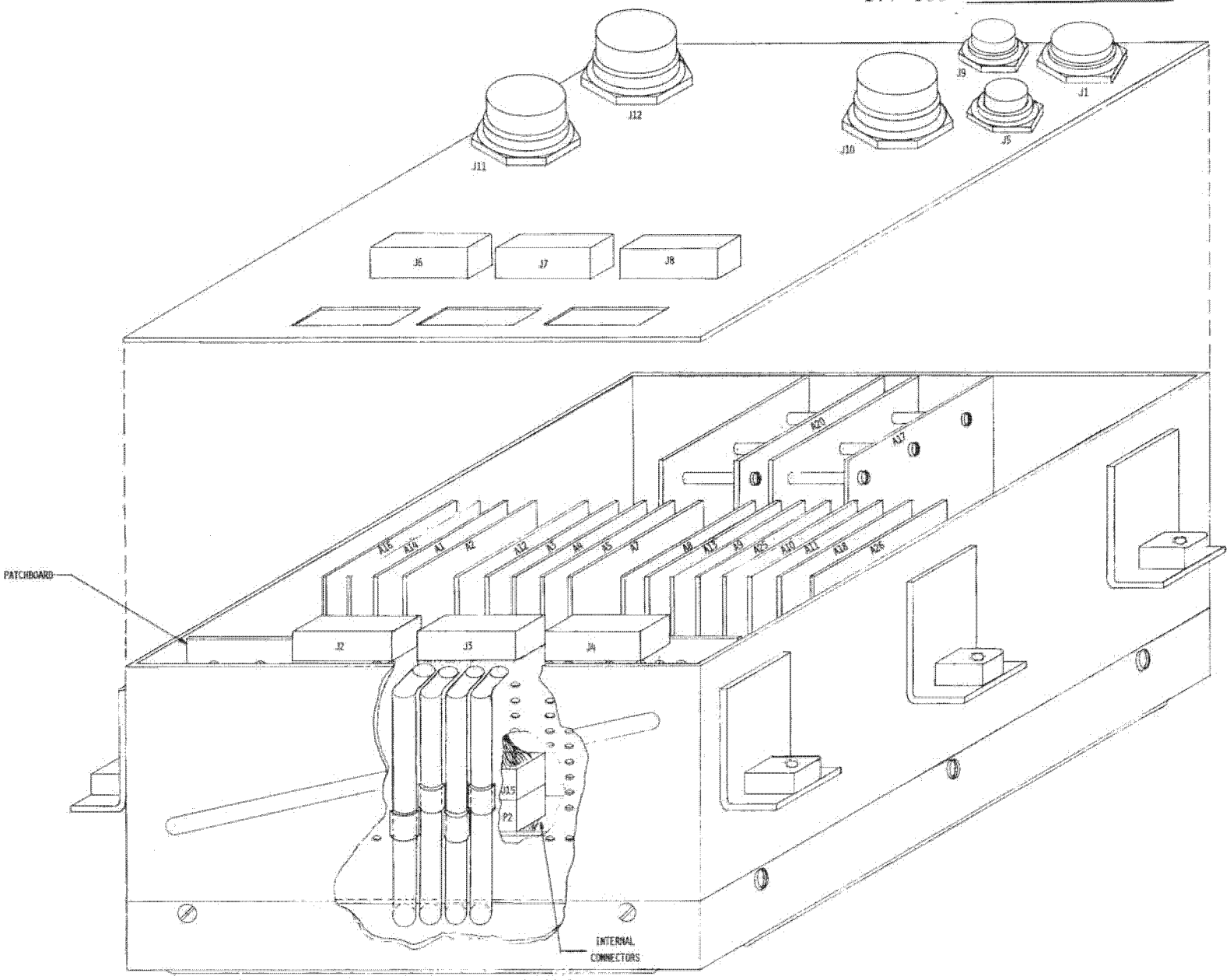

Figure 3.10-3. Instrumentation Processor

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TABLE 3.10-1

IP BOARD AND MODULE ASSEMBLIES

Assembly	Description
A1, A2, A4, A5, A7, A8, A10, A11, A12, A26	Each board assembly has twenty four-27 KΩ resistors which provide isolation for the test and umbilical points.
A3 Board	Contains circuits for analog instrumentation points 5196, 5198, 5200, and discrete instrumentation points 5574, 5575, 5589, and 5590.
A9 Board	Contains circuits for analog IMP's 5013, 5076, 5111, 5235, 5236.
A13 Board	Contains circuits for analog IMP's 5112, 5114, 5145.
A14 Board	Contains buffer amplifiers for analog IMP's 5099, 5110, 5150.
A16 Board	IP unipoint ground.
A17 Module	Contains circuits for discrete points 5576, 5614.
A18 Board	Contains resistors for terminating the frequency phase lock loop electronics (FPLLE) encoder test signals and spare capacitors that may be used in the event of electromagnetic interference (EMI) problems (none are presently used).
A20 Module	Contains the circuitry for processing analog point 5375.
A23	Patchboard
A25 Board	Contains buffer amplifiers for analog points 5113, 5115, 5120, 5155.

nal connector P1, J3 to P2, and J4 to P3.

10.2.2 IP Electrical

The IP electrical connections consist of the input, output, monitor and test signals, power inputs (+5, ±15, and 24.5 vdc), and the instrumentation and power return lines.

The input signals to the IP originate at remote instrumentation transducers and circuits on components and assemblies throughout the PPS/DP EAC and are routed into the IP through connectors J6, J7, J8, and J9. There are two classes of input signals, processed and unprocessed. Processed signals are those that have been previously processed outside the IP to conform to the IP output signal requirements. Unprocessed signals are those that require processing within the IP to conform to the output signal requirements.

Preprocessed analog signals, analog signals processed in the IP, and analog signals generated in the IP have the following output characteristics:

(1)	Amplitude	0 to 5 vdc	
(2)	Source impedance	Resistance	<10 KΩ
		Capacitance	< 1700 pf*
			or >0.1 μf

The output signals pass through the patchboard and are brought out of the IP through connectors J2, J3, and J4 which are routed directly to the DTU.

*This figure is lower than the input capacitance requirement of the DTU (2000 pf) to allow for cable capacitance between the IP and the DTU.

The test signals, which consist of parallel outputs of most instrumentation signals, are brought out of the IP through connectors J10, J11, and J12. These points are isolated from the instrumentation output signals with series resistors. The amplitude of the test signals is equal to that of the instrumentation signal. The source impedance is equal to the sum of the isolation resistor (27 KΩ) and the impedance of the instrumentation signal.

The monitor signals (BIL's) are hardline outputs of selected instrumentation points isolated by the same 27 KΩ resistors used to isolate the associated TSP, and brought out of the IP through connector J1. One additional BIL (8010) which has no corresponding instrumentation point is also processed through the IP.

Test connectors J10, J11, and J12 carry several additional signals not directly associated with instrumentation. Included are encoder signals from the 9 and 5 frequency phase lock loop platen drives and circuit continuity checks used during testing. These signals are representative of the test signals and testing provisions within the PPS/DP EAC components that have been incorporated to monitor the performance of hardware during various levels of assembly.

The IP receives main power (24.5 $^{+5.2}_{-3.5}$ vdc), instrumentation power (+5, ±15 vdc), and main power returns through connector J1. Connector J5 carries main power, +15-volt instrumentation power, and the main and instrumentation power returns for the DIU.

To control noise on the instrumentation lines, and to isolate instrumentation circuits from the functions they monitor, the main power and instrumentation power returns are separated. Most instrumentation returns from areas of the PPS/DP EAC are electrically connected at a single point within the IP to form the instrumentation unipoint ground (Figure 3.10-4) which in turn is con-

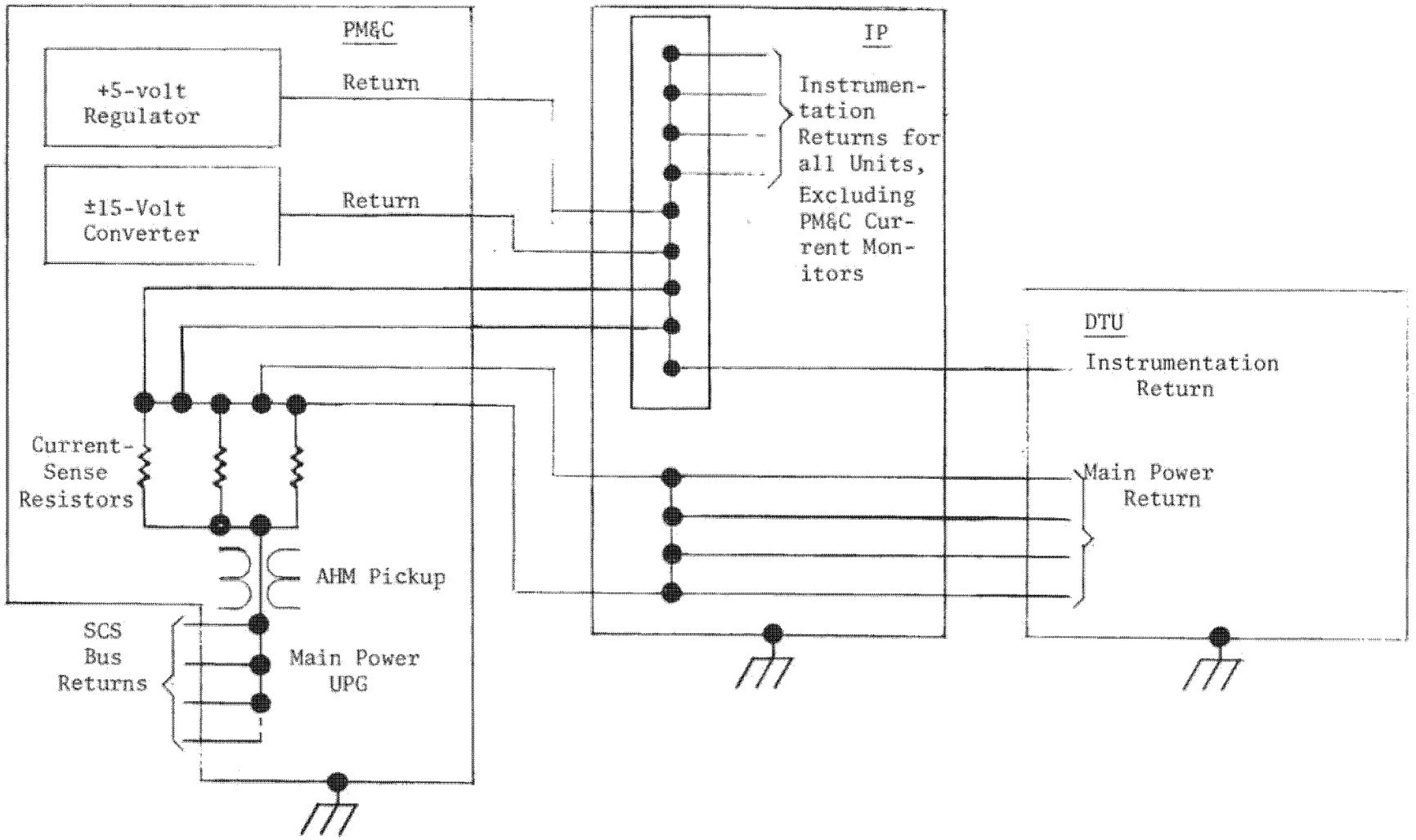


Figure 3.10-4. Instrumentation Unipoint Ground

nected to the lowest potential portion of the unregulated power unipoint within the power monitor and control (PM and C) unit. (Reference Part 3, Section 7.)*

10.2.2.1 IP Processing and Generating Circuitry. The majority of analog instrumentation signals are preprocessed before entering the IP and are carried through the IP as illustrated in Figure 3.10-5. Of the remaining analog points, three are generated in the IP, and 16 are processed (not counting BIL 8010 which has no corresponding IMP).

For discrete instrumentation, all points, except those originating in the IP, are routed directly to the DTU in accordance with Figure 3.10-6. Unlike analog points, not all discrete instrumentation points in the IP have corresponding test outputs, and there are no discrete umbilical outputs.

Table 3.10-2 presents a listing of the discrete and analog points either processed or generated in the IP and also lists the PPS/DP EAC umbilical monitors. The circuit designations on Table 3.10-2 refer to Figures 3.10-7 through 3.10-17 which are simplified schematics of the instrumentation and umbilical point IP circuitry.

10.3 PPS/DP EAC Slave Digital Telemetry Unit

The PPS/DP EAC slave DTU is a data processing unit that consists of two redundant halves in a single assembly. Each half is fully independent except for shared instrumentation input lines. In operation, the DTU interfaces

*Current monitor instrumentation in the PM and C is connected directly to the unregulated power unipoint ground.

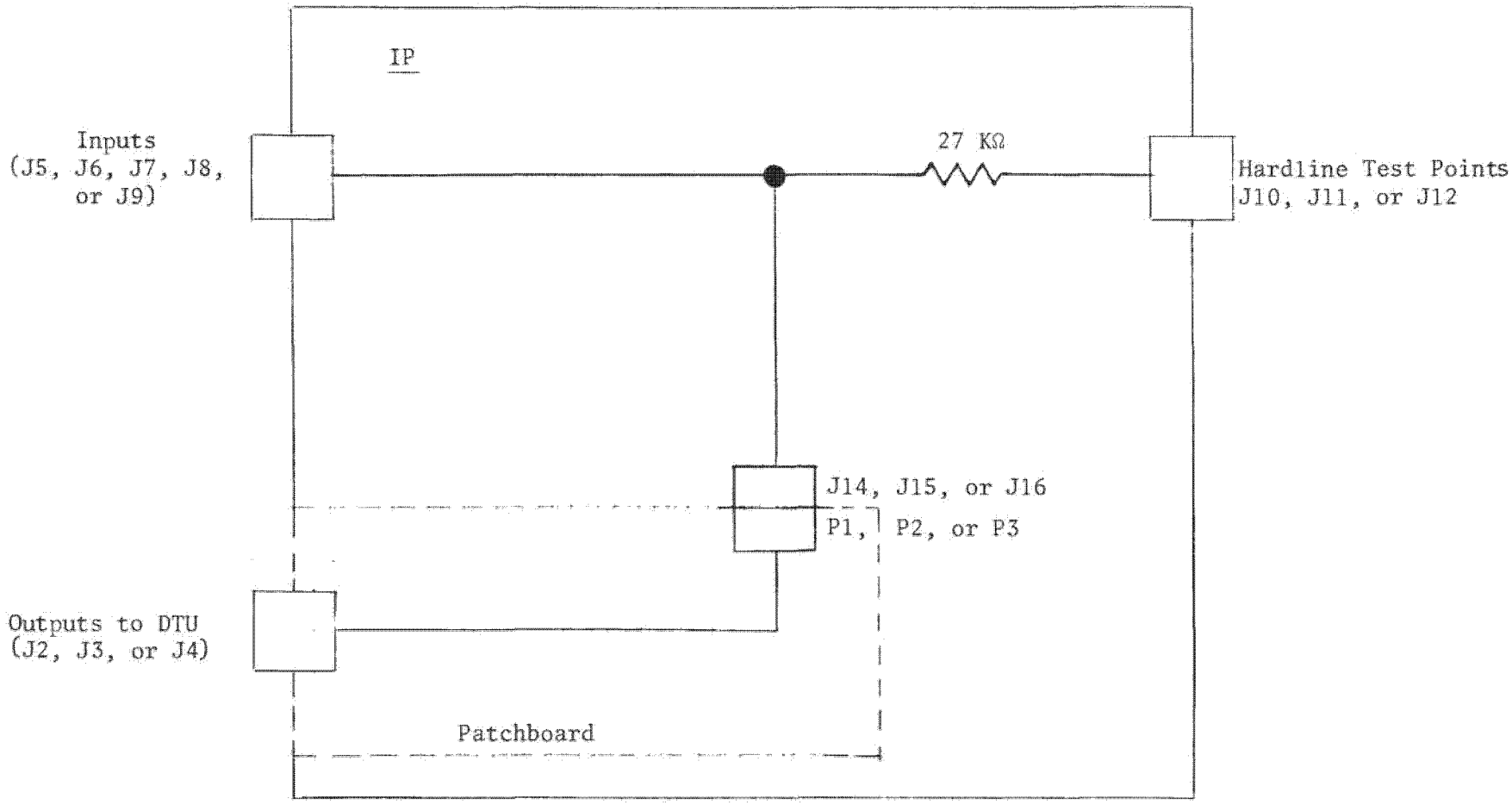


Figure 3.10-5. Typical Preprocessed Analog Signal IP Circuit

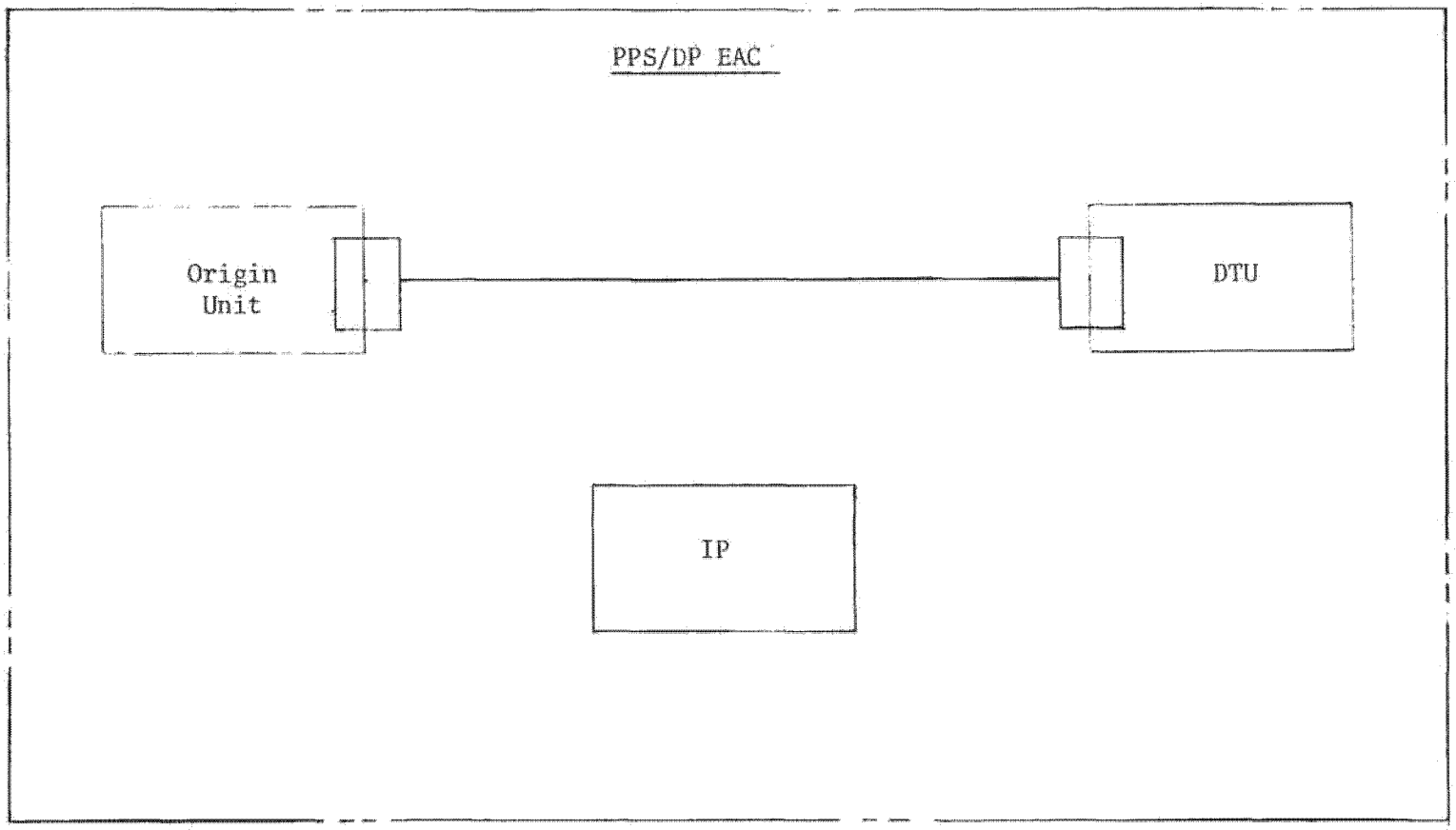


Figure 3.10-6. Typical Signal Routine for Non-IP Generated Discrete IMP's

TABLE 3.10-2

IP PROCESSED OR GENERATED INSTRUMENTATION AND UMBILICAL POINTS

IMP	TITLE	TYPE	CORRESPONDING BIL	CIRCUIT (FIGURE NO.)
5013	Temperature, Primary Film Supply	Processed	-	3.10-7
5076	Temperature, Secondary Film Supply		-	3.10-7
5099	Temperature, Stereo Mirror		8012	3.10-8
5110	Temperature, Corrector, Camera Spacer		8006	3.10-8
5111	Temperature V.P. Door Inside Insulation, -Y		-	3.10-9
5112	Temperature Lens Tube Fwd, Station (STA) 175, 279 degrees		8007	3.10-9
5113	Temperature, Lens Tube Aft, STA 244, 5 degrees		-	3.10-8
5114	Temperature V.P. Door, Inside Insulation, +Y		8002	3.10-10
5115	Temperature, Lens Tube Fwd, STA 175, 99 degrees		-	3.10-8
5120	Temperature, Insulation Inner STA 108, 7 degrees	Processed	-	3.10-8

TABLE 3.10-2 (CONT'D)

IMP	TITLE	TYPE	CORRESPONDING BIL	CIRCUIT (FIGURE NO.)
5145	Temperature, Primary Mirror 2 (-Y)	Processed	8008	3.10-9
5150	Temperature, Primary Mirror 1 (+Y)	Processed	8001	3.10-8
5155	Temperature, Insulation Inner, STA 244, 186 degrees	Processed	-	3.10-8
5196	+15 vdc Supply	Generated	-	3.10-11
5198	+5 vdc Supply	Generated	-	3.10-12
5200	-15 vdc Supply	Generated	-	3.10-12
5235	Temperature, SRV 1 Film T/U Assembly	Processed	-	3.10-7
5236	Temperature, SRV 2 Film T/U Assembly		-	3.10-7
5375	Differential Temperature, Stereo Mirror Lower		8000	3.10-13
-	Temperature, Inlet Air		8010	3.10-17
5574	Spinoff Disconnect 1		-	3.10-14
5575	Spinoff Disconnect 2	Processed	-	3.10-14

TABLE 3.10-2 (CONT'D)

IMP	TITLE	TYPE	CORRESPONDING BIL	CIRCUIT (FIGURE NO.)
5576	Arm/Continuity, 1	Processed	-	3.10-15
5589	DTU 1 On/Off		-	3.10-16
5590	DTU 2 On/Off		-	3.10-16
5614	Arm/Continuity, 2	Processed	-	3.10-15

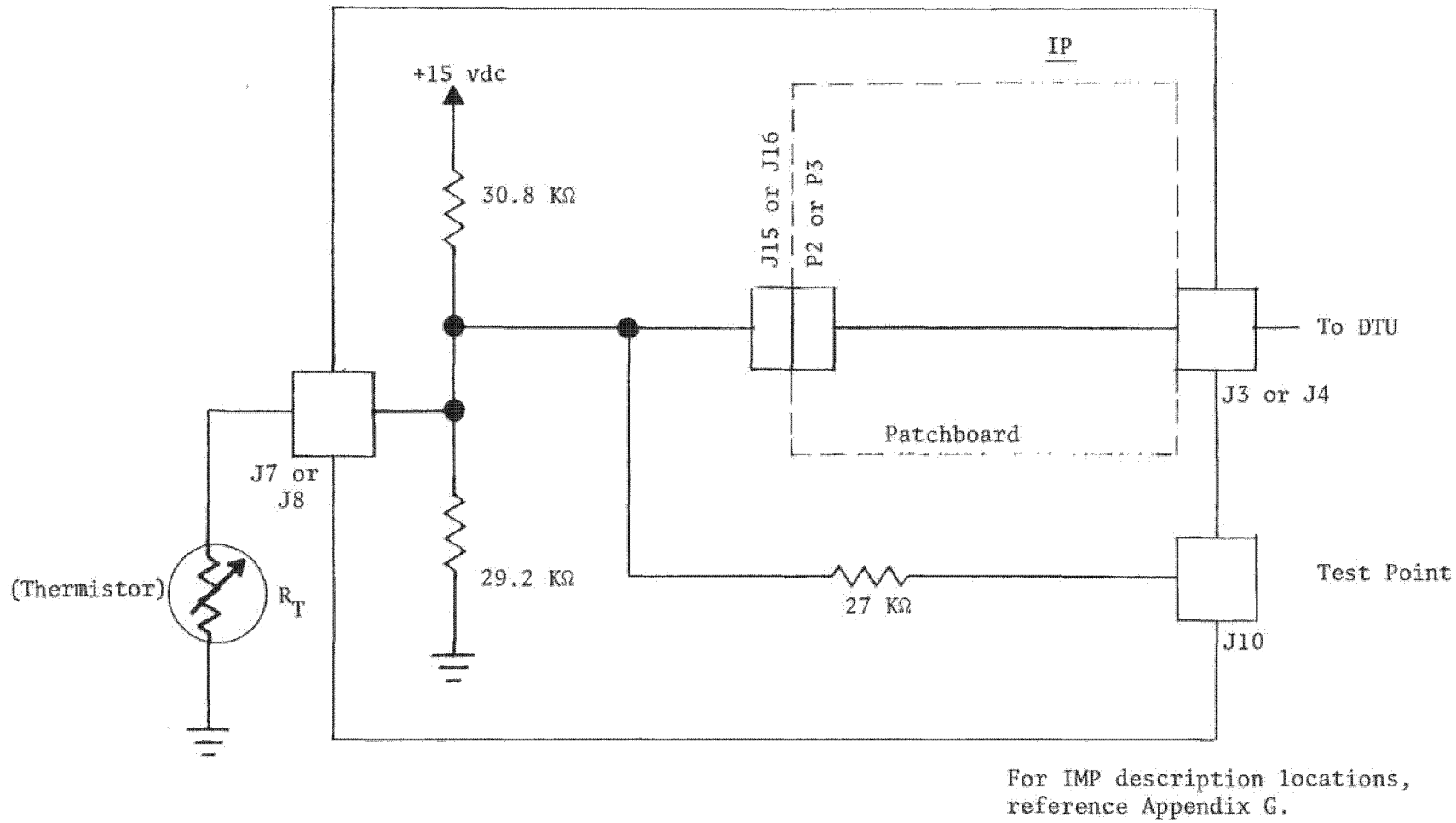
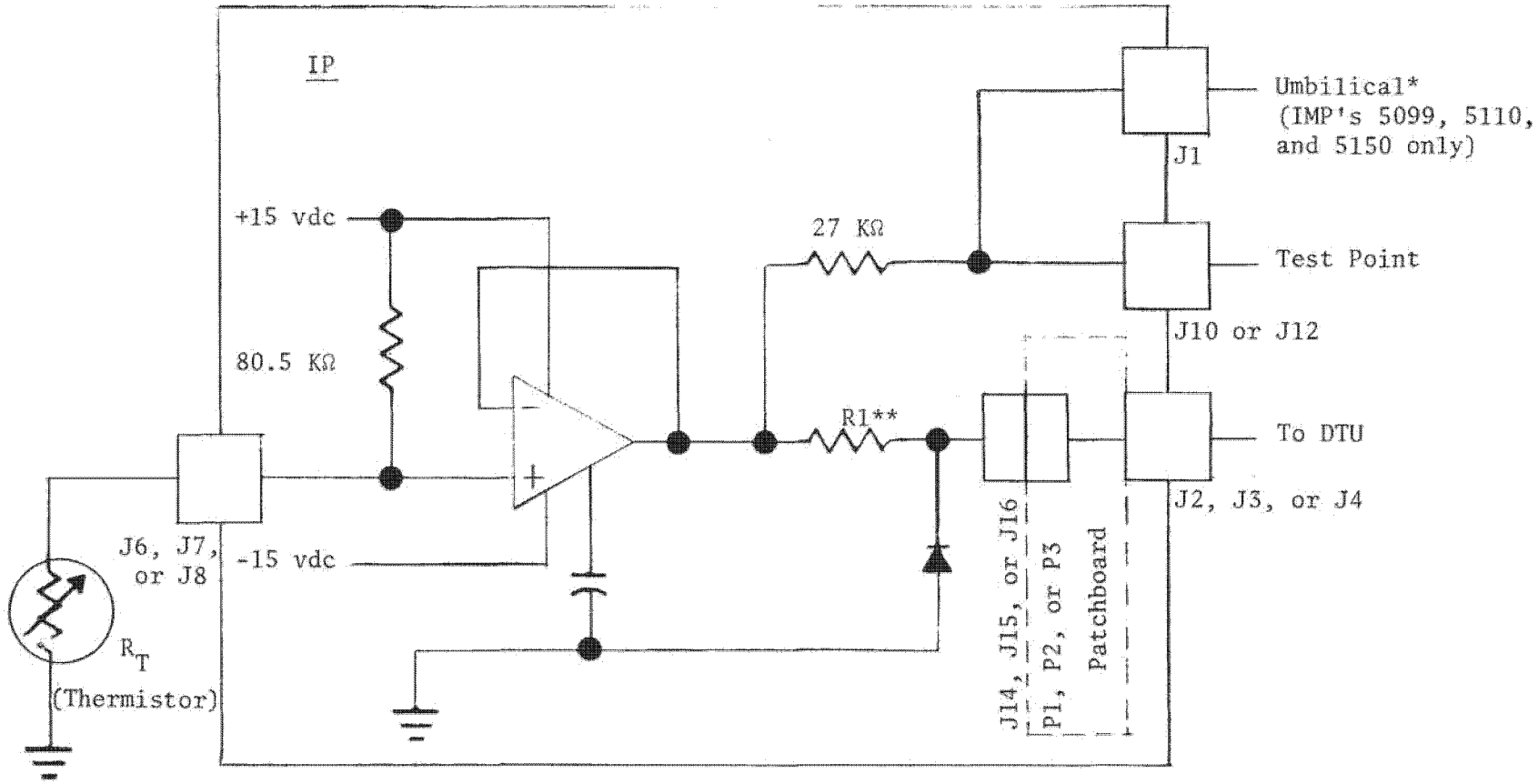


Figure 3.10-7. Typical Processing Circuit: IMP's 5013, 5076, 5235, 5236



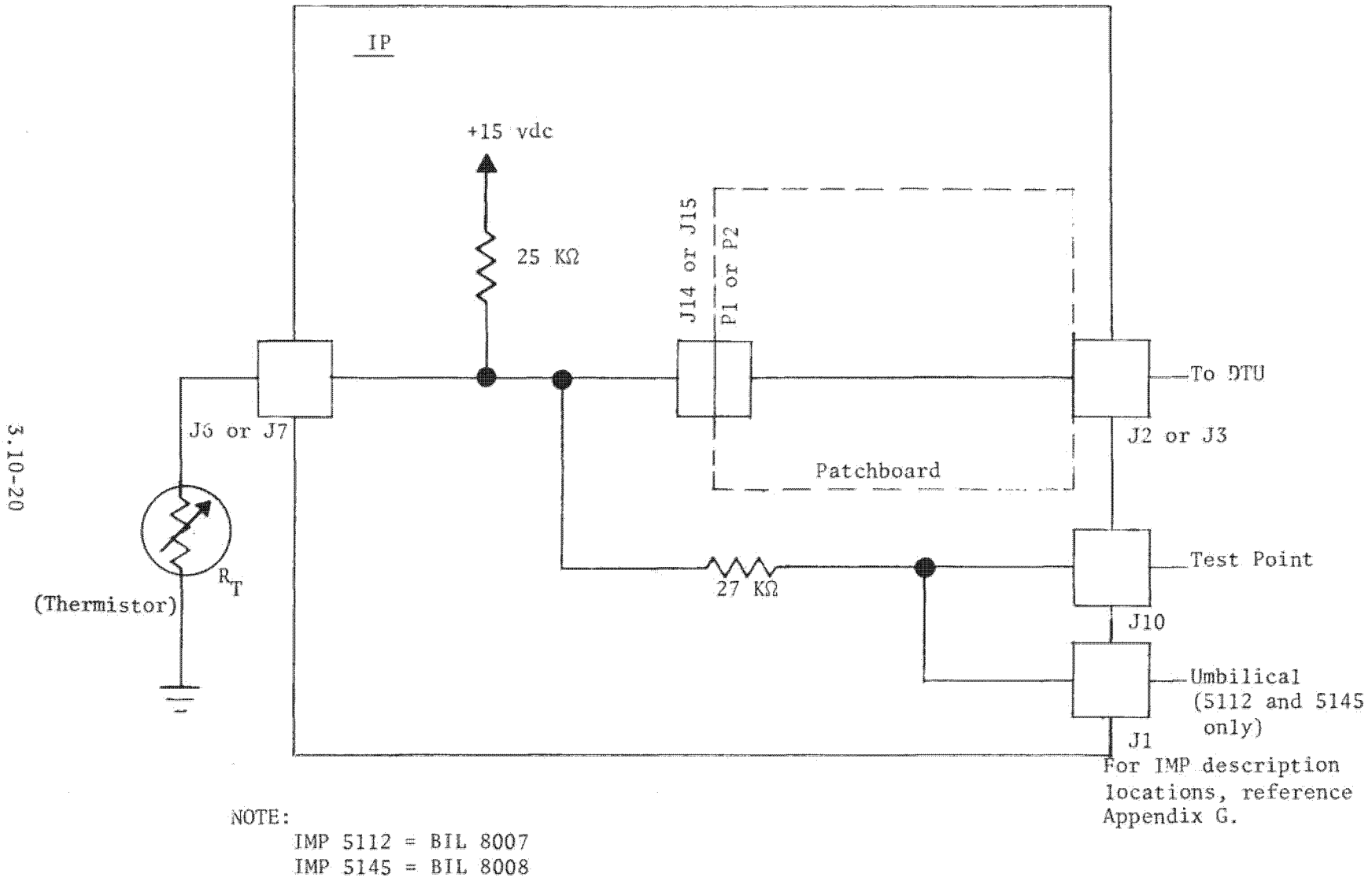
3.10-19

* IMP 5099 = BIL 8012
IMP 5110 = BIL 8006
IMP 5150 = BIL 8001

** R1 = 5 KΩ for IMP's 5110 and 5150
R1 = 499Ω for all others

For IMP description locations, reference Appendix G.

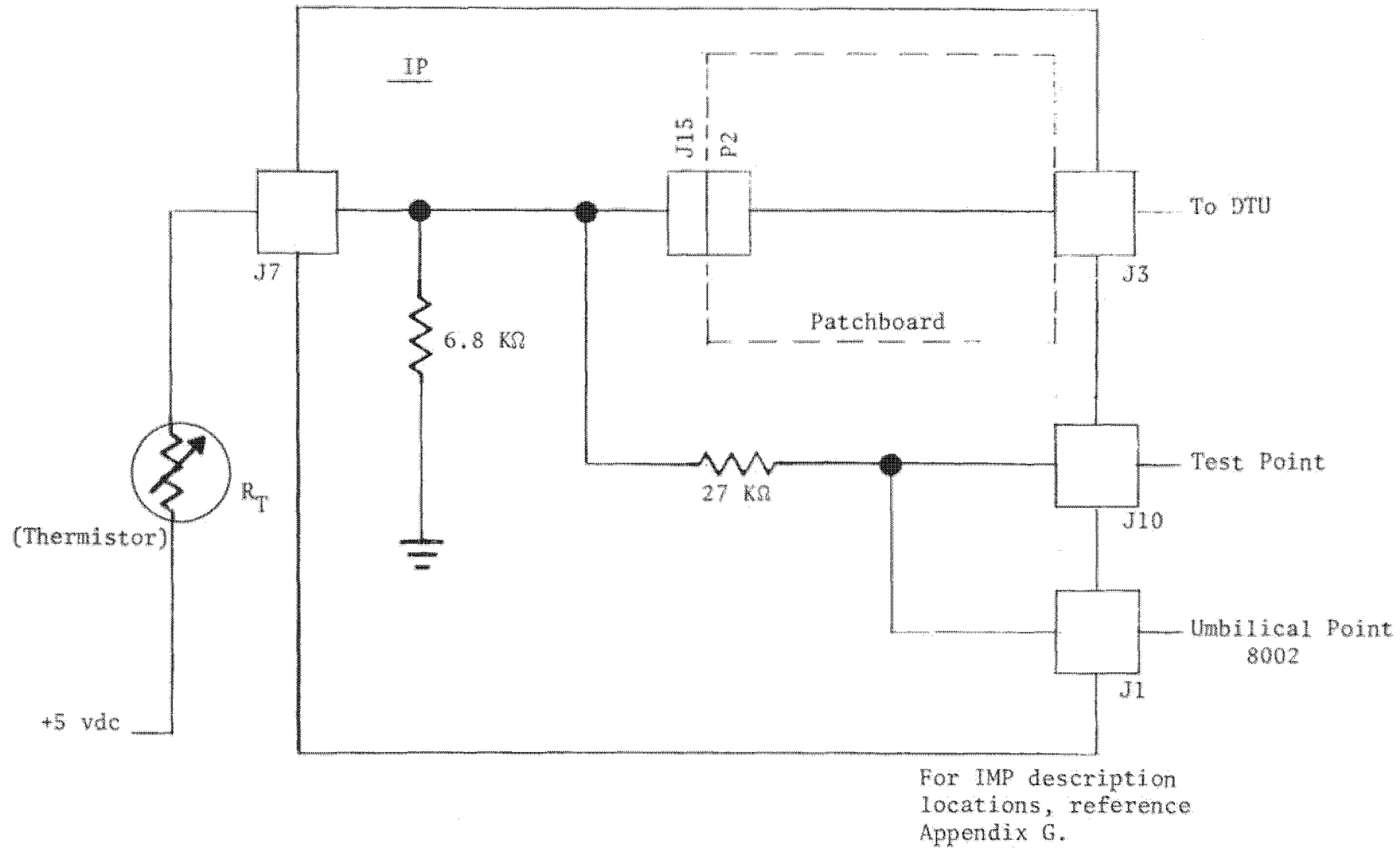
Figure 3.10-8. Typical Processing Circuitry: IMP's 5099, 5110, 5113, 5115, 5120, 5150, 5155



NOTE:
IMP 5112 = BIL 8007
IMP 5145 = BIL 8008

Figure 3.10-9. Typical IP Processing Circuits: IMP's 5111, 5112, and 5145

3.10-20



3.10-21

Figure 3.10-10. IMP 5114 Processing Circuit

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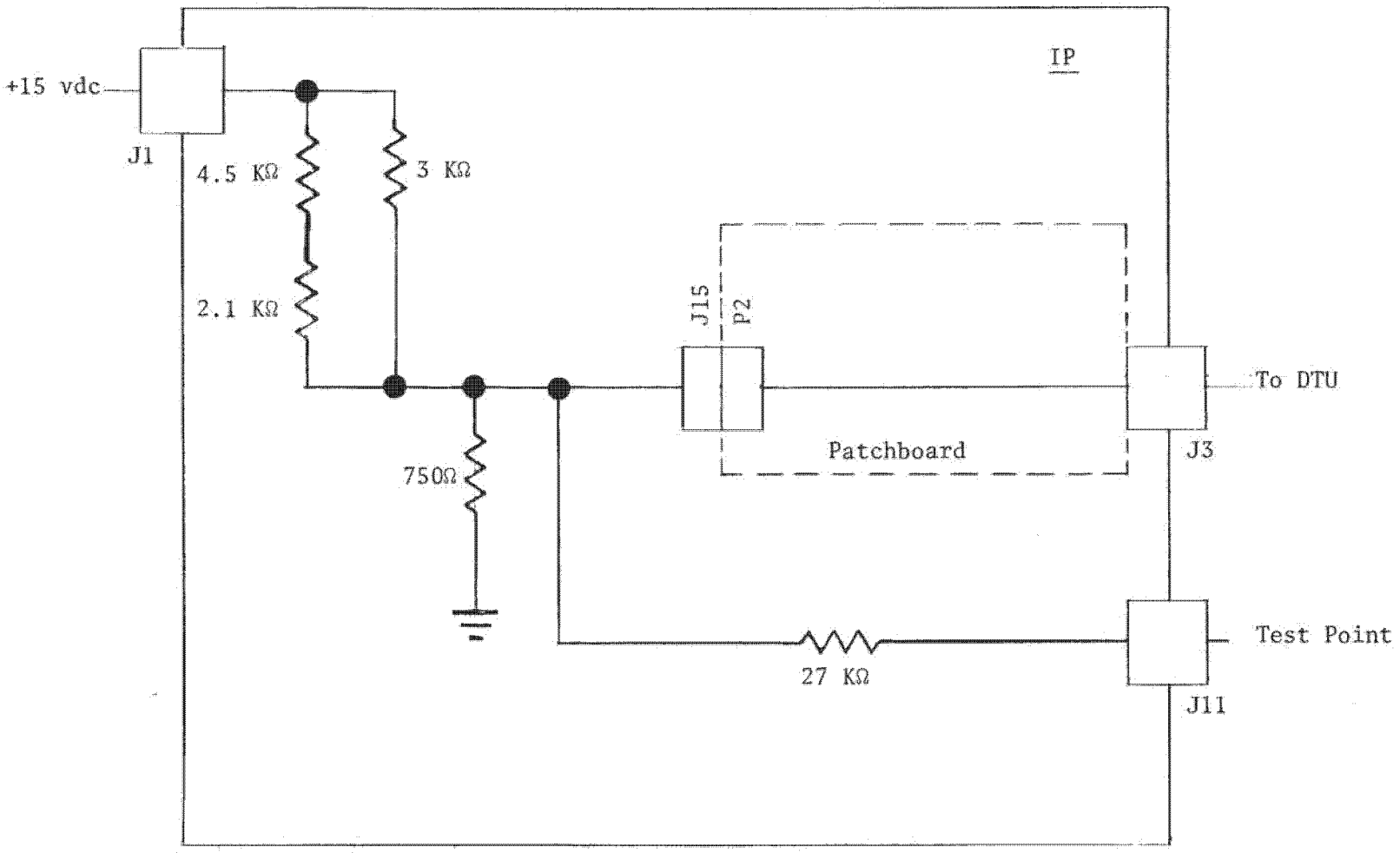
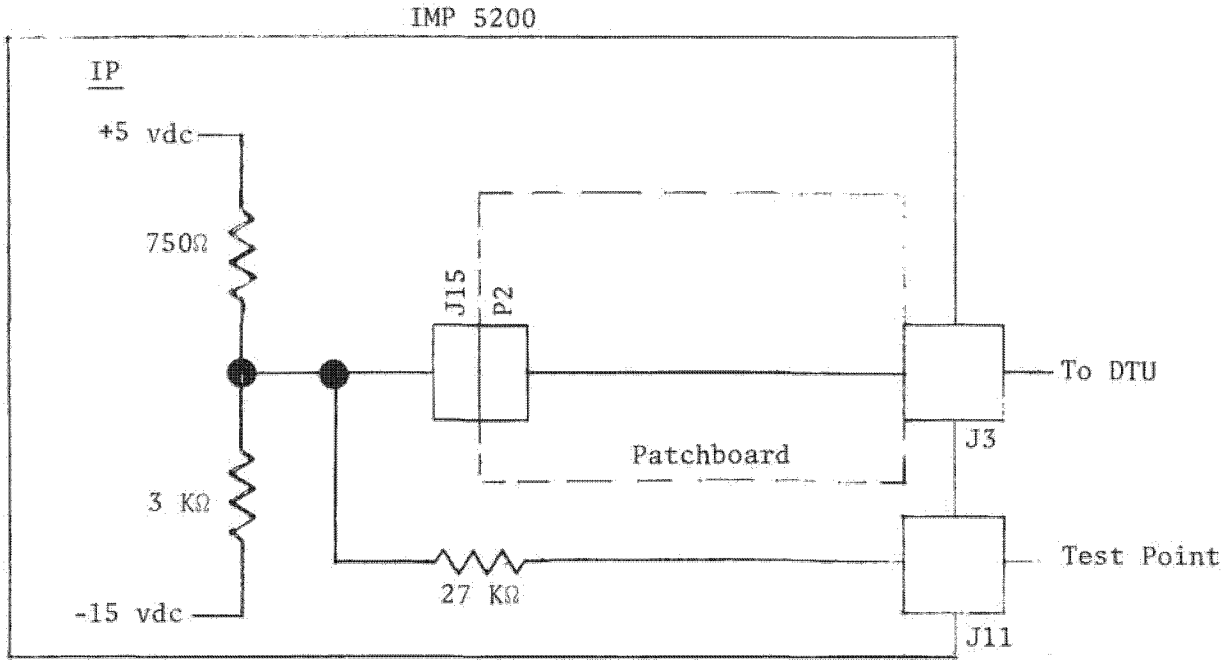


Figure 3.10-11. IMP 5196 Generating Circuit



For IMP descriptions, reference Table 3.10-10.

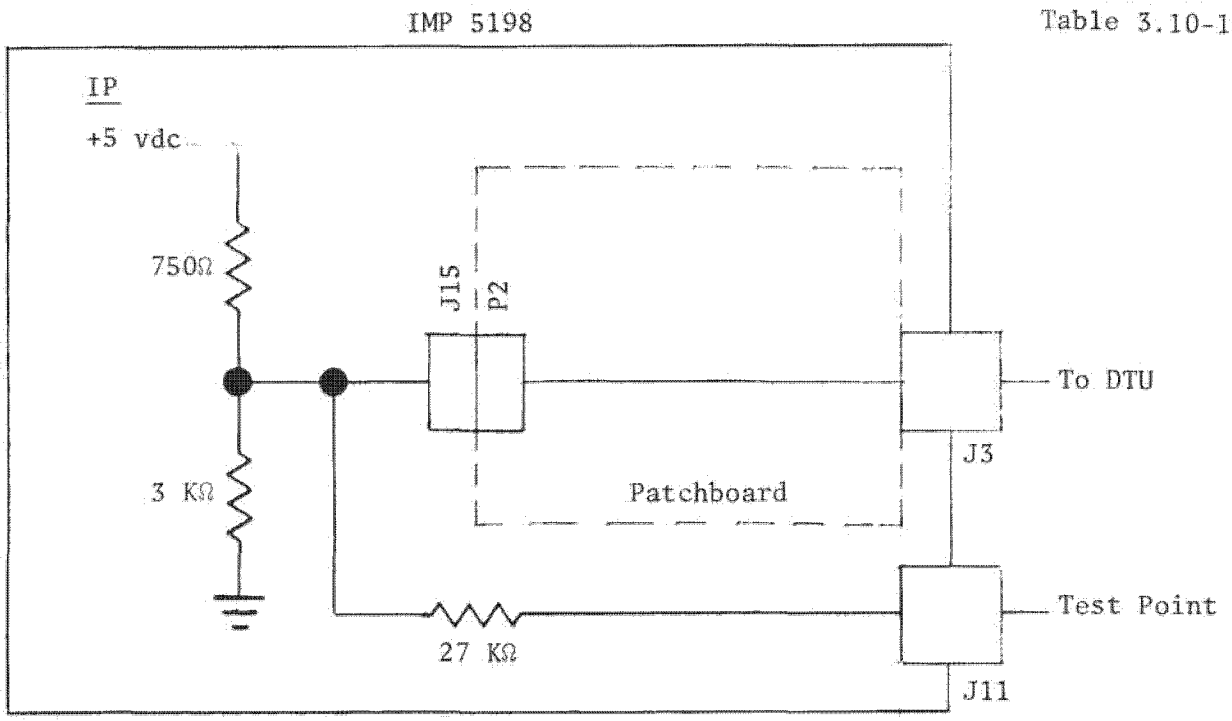


Figure 3.10-12. Generating Circuit: IMP's 5198 and 5200

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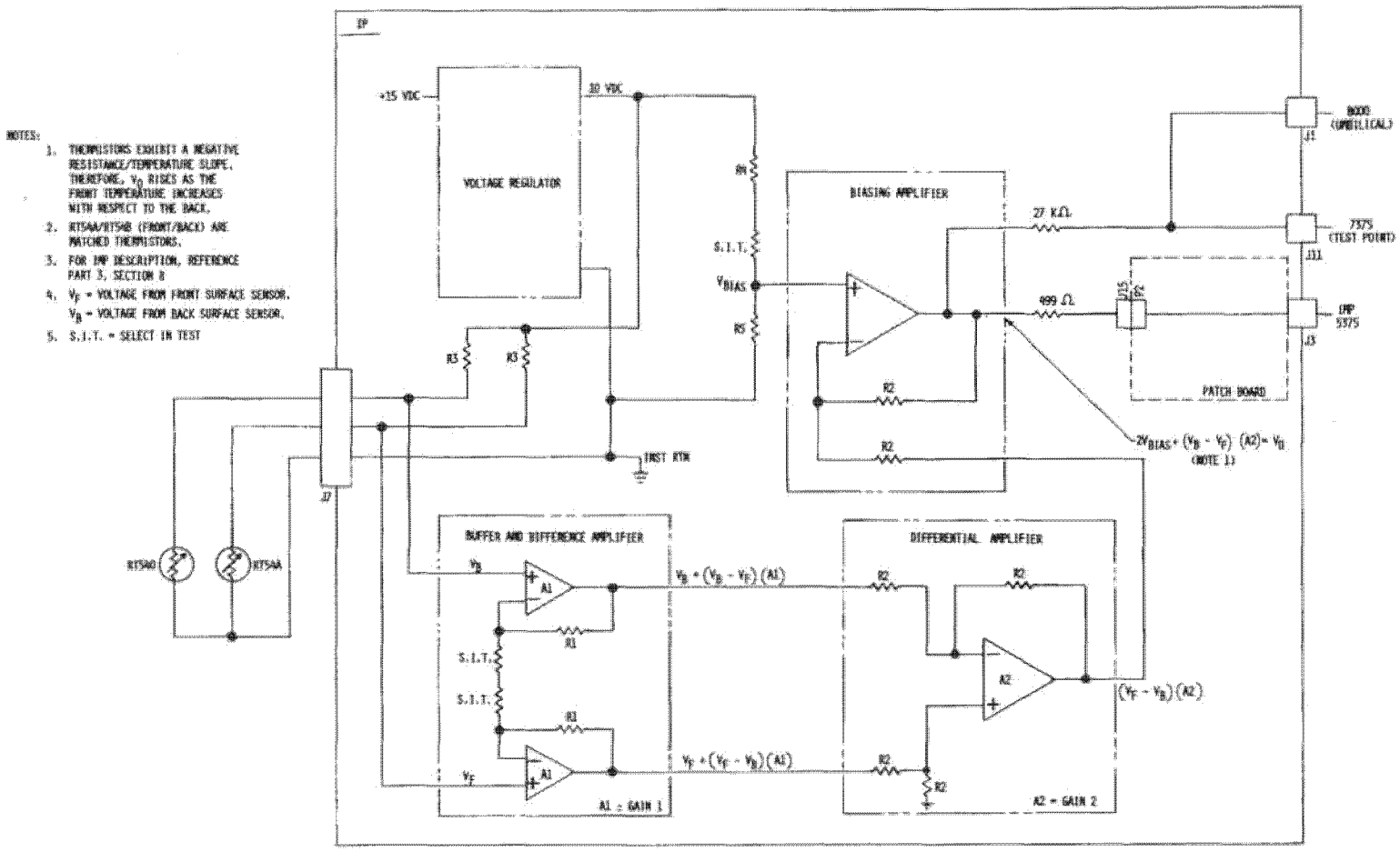
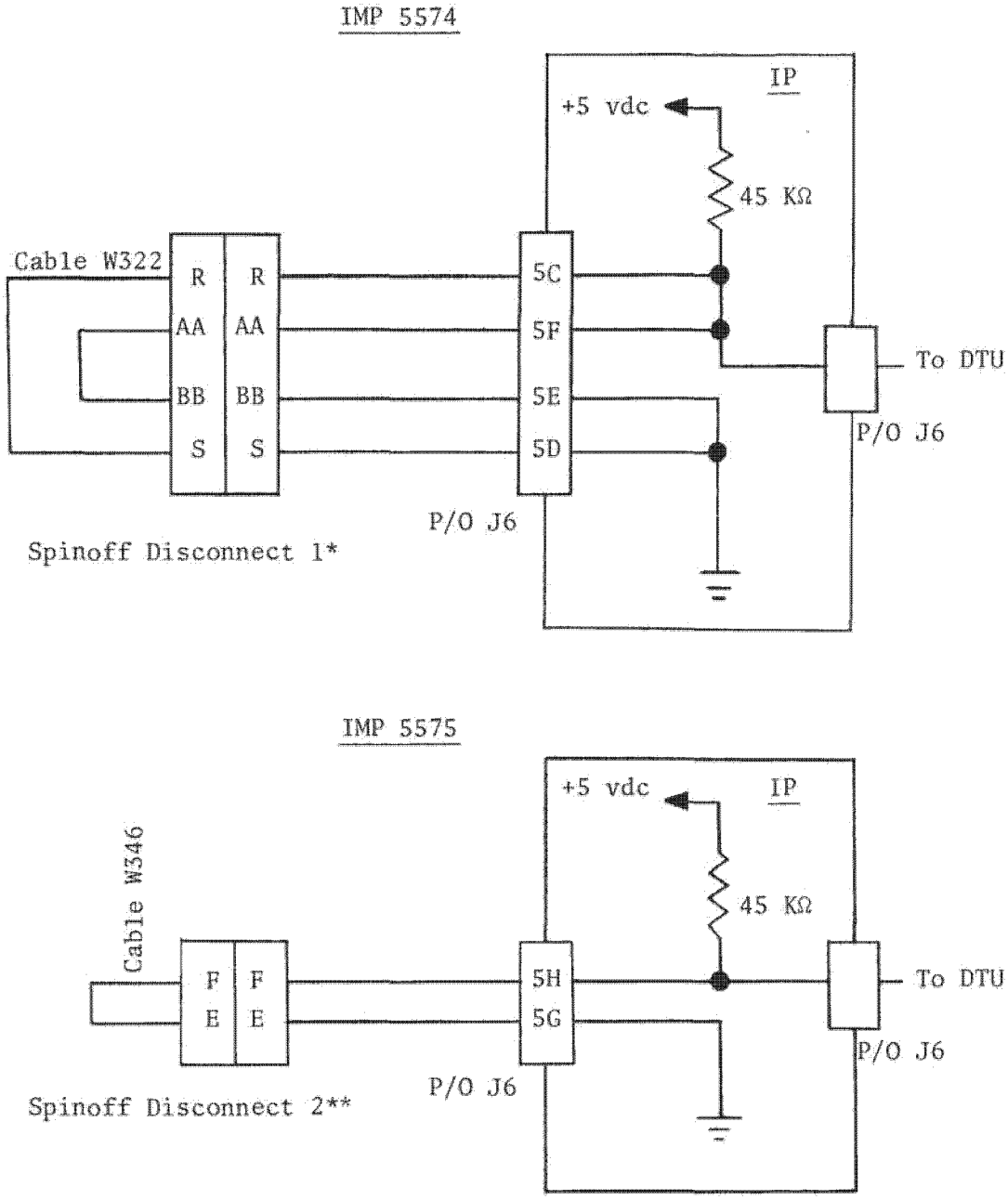


NOTES:

1. THERMISTORS EXHIBIT A NEGATIVE RESISTANCE/TEMPERATURE SLOPE, THEREFORE, V_O RISES AS THE FRONT TEMPERATURE INCREASES WITH RESPECT TO THE BACK.
2. RT5AA/RT5AB (FRONT/BACK) ARE MATCHED THERMISTORS.
3. FOR IMP DESCRIPTION, REFERENCE PART 3, SECTION 8
4. V_F = VOLTAGE FROM FRONT SURFACE SENSOR.
   V_B = VOLTAGE FROM BACK SURFACE SENSOR.
5. S.I.T. = SELECT IN TEST

Figure 3.10-13. IP Processing Circuit: IMP 5375



* Activated by SRV 1 SEPARATE command
** Activated by SPINOFF DISCONNECT 2 command

For IMP description location, reference Appendix G.

Figure 3.10-14. IP Processing Circuits: IMP's 5574 and 5575

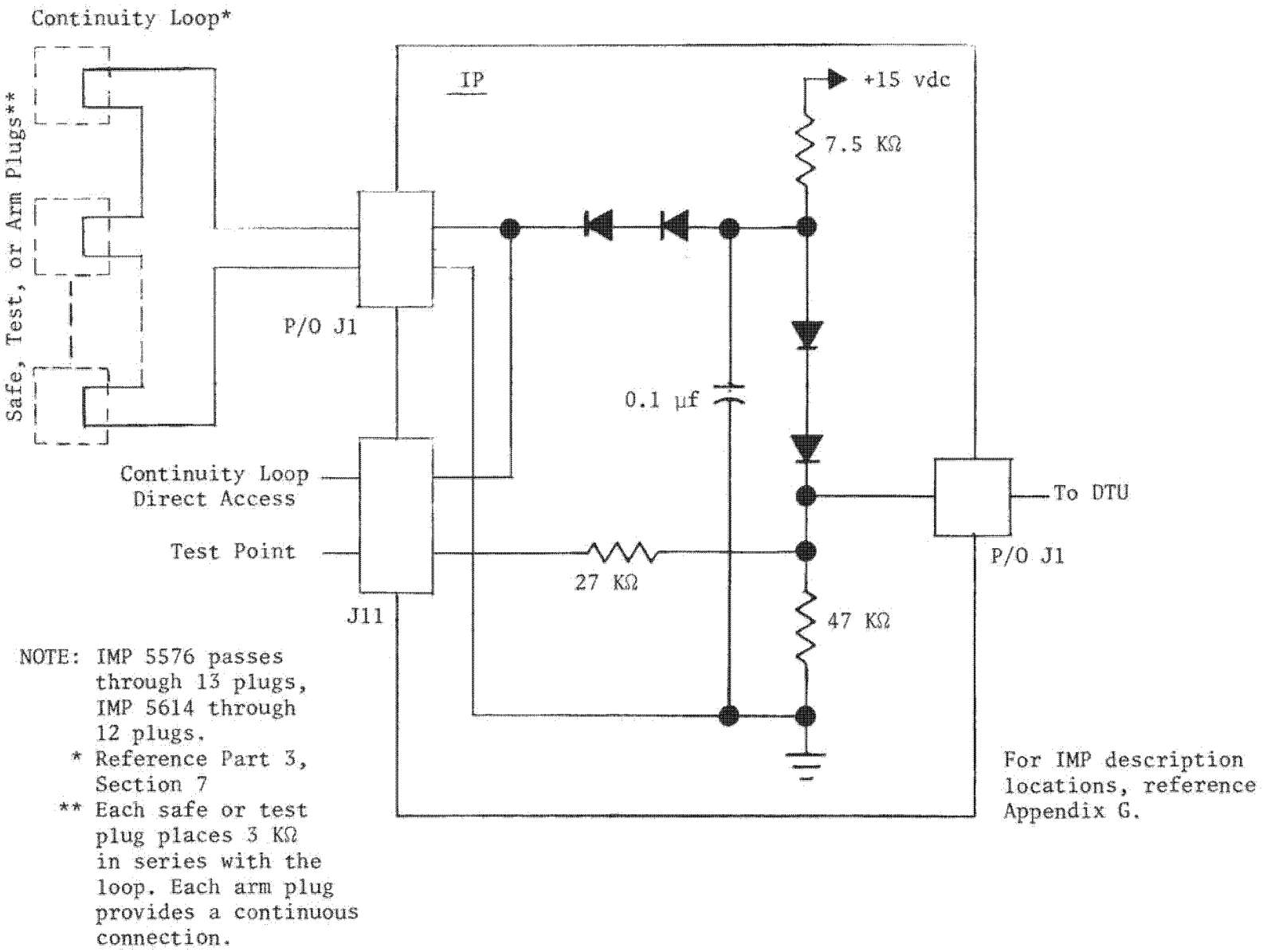
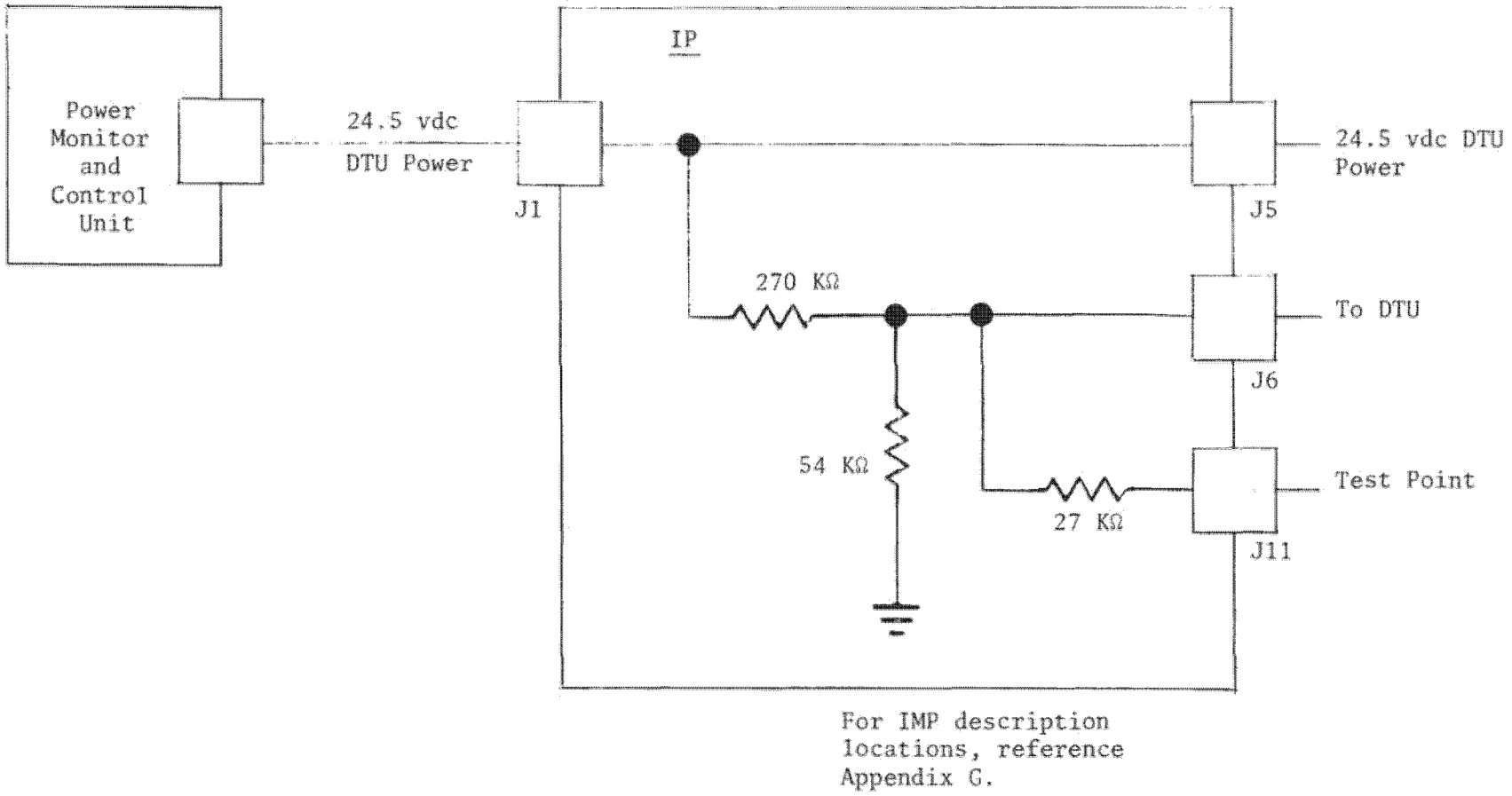


Figure 3.10-15. Typical IP Processing Circuit: IMP's 5576 and 5614



3.10-27

Figure 3.10-16. Typical IP Processing Circuit: IMP's 5589 and 5590

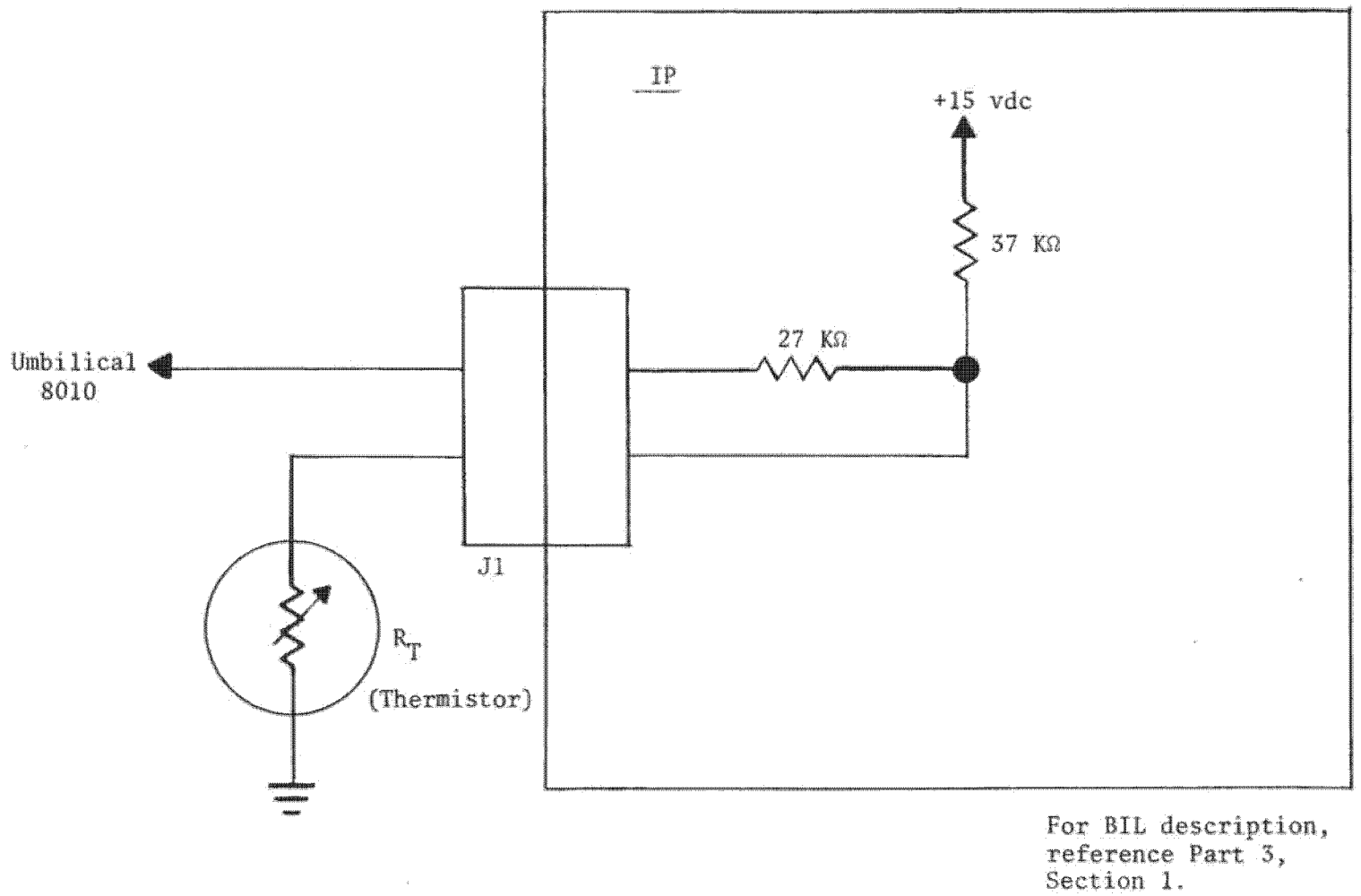


Figure 3.10-17. IP Processing Circuit: BIL 8010

with the master digital telemetry unit (MDTU) through separate address and reply lines (party lines), and formats analog and discrete data from the vehicle instrumentation based on party line address information. When an address that defines a unique analog data channel in the PPS/DP EAC slave DTU is received, the analog signal on that channel is sampled and input to an analog-to-digital (A/D) converter for digitizing. The digitized data is then formatted for output on the party reply line. Similarly, for discrete addresses, discrete data* is input to a level decision comparator, and then formatted into party reply line data. Figure 3.10-18 illustrates the DTU/MDTU interface.

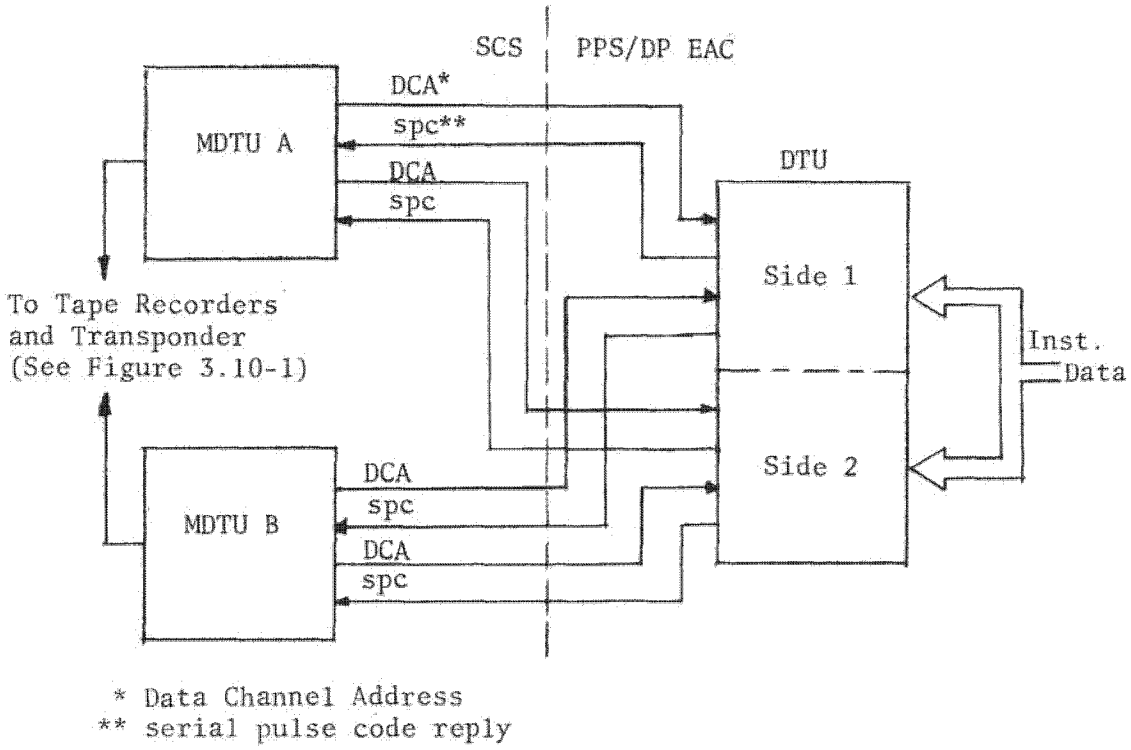


Figure 3.10-18. MDTU/DTU Interface

* A discrete data word consists of 8 separate instrumentation inputs, each of which is digitized by the DTU and controls one bit (high or low) of the 8-bit reply signal.

10.3.1 DTU Assembly

DTU slave units are composed of various combinations of two basic building blocks or slices: Converter units (CU's) and the multiplexer units, which can be either analog multiplexers (AMU's) or discrete multiplexers (DMU's). The PPS/DP EAC slave consists of two CU's, two AMU's, and one DMU. Each AMU slice contains redundant processing circuits for 128 analog inputs. The DMU is capable of processing 128 discrete inputs in 16 eight-bit words through its redundant circuits. This results in a maximum capacity of 256 analog and 128 discrete inputs for the PPS/DP EAC slave.

Each half or side of the PPS/DP EAC slave consists of one CU and one of the two redundant processing circuits in each multiplexer. Thus side 1, or DTU 1 as it is more commonly referred to, consists of CU A1 and one half of each multiplexer unit (AMU's A5 and A6, and DMU A3). Side 2, or DTU 2, consists of CU A2 and the remaining half of each multiplexer (see Figure 3.10-19).

Figure 3.10-20 illustrates the DTU assembly, showing the 5 individual units and the external electrical interface connectors. The entire assembly weighs less than fourteen pounds, and is mounted to rails on the -Y side of the film supply enclosure (reference Part 3, Section 1; Figure 3.1-13.)

Within each DTU slice, electrical components are supported on multilayer printed circuit boards held by retainers on the housing. Rather than direct wiring, printed circuit "mother" boards are used to interconnect the component boards and external electrical plugs. Power and signals are carried between slices by electrical connectors on the housing sides. These connectors are not referenced in the PPS/DP EAC as they are inaccessible on an assembled DTU. Figure 3.10-21 depicts a typical AMU or DMU (they are essentially identical mechanically) and Figure 3.10-22 a typical CU.

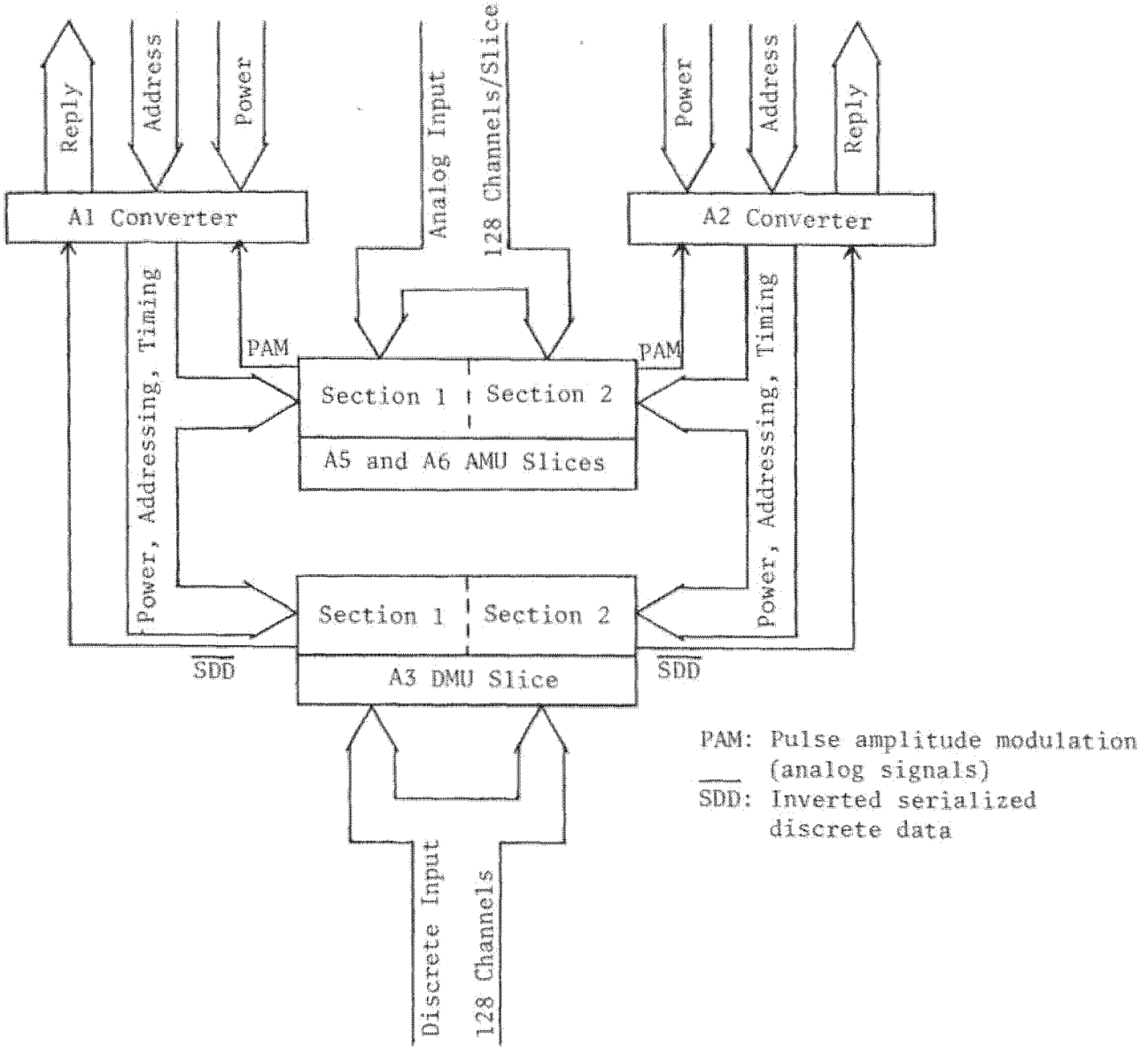


Figure 3.10-19. DTU Organization

A1: Converter Unit
A2: Converter Unit
A3: Digital Multiplexer Unit
A5: Analog Multiplexer Unit
A6: Analog Multiplexer Unit

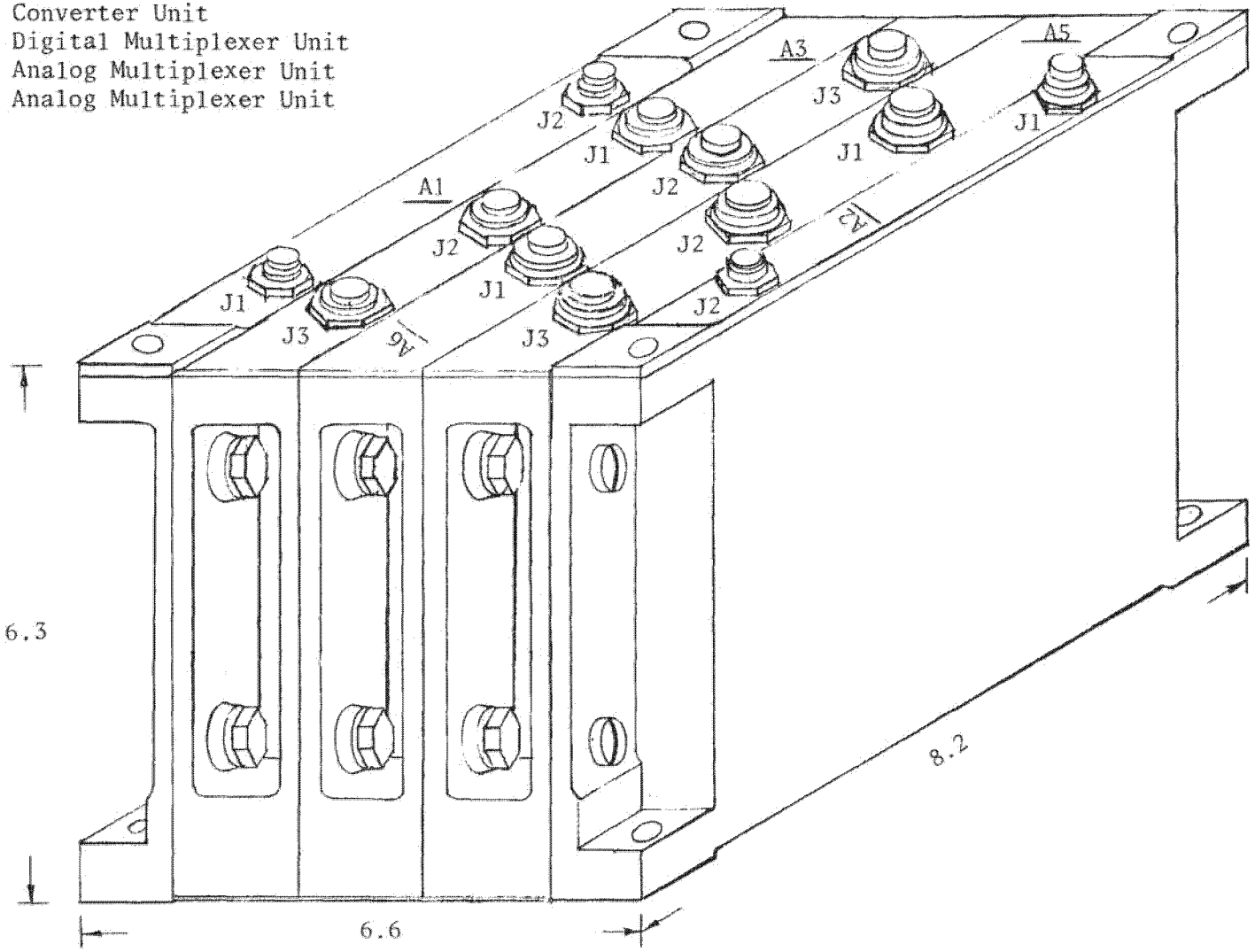


Figure 3.10-20. PPS/DP EAC Slave DTU

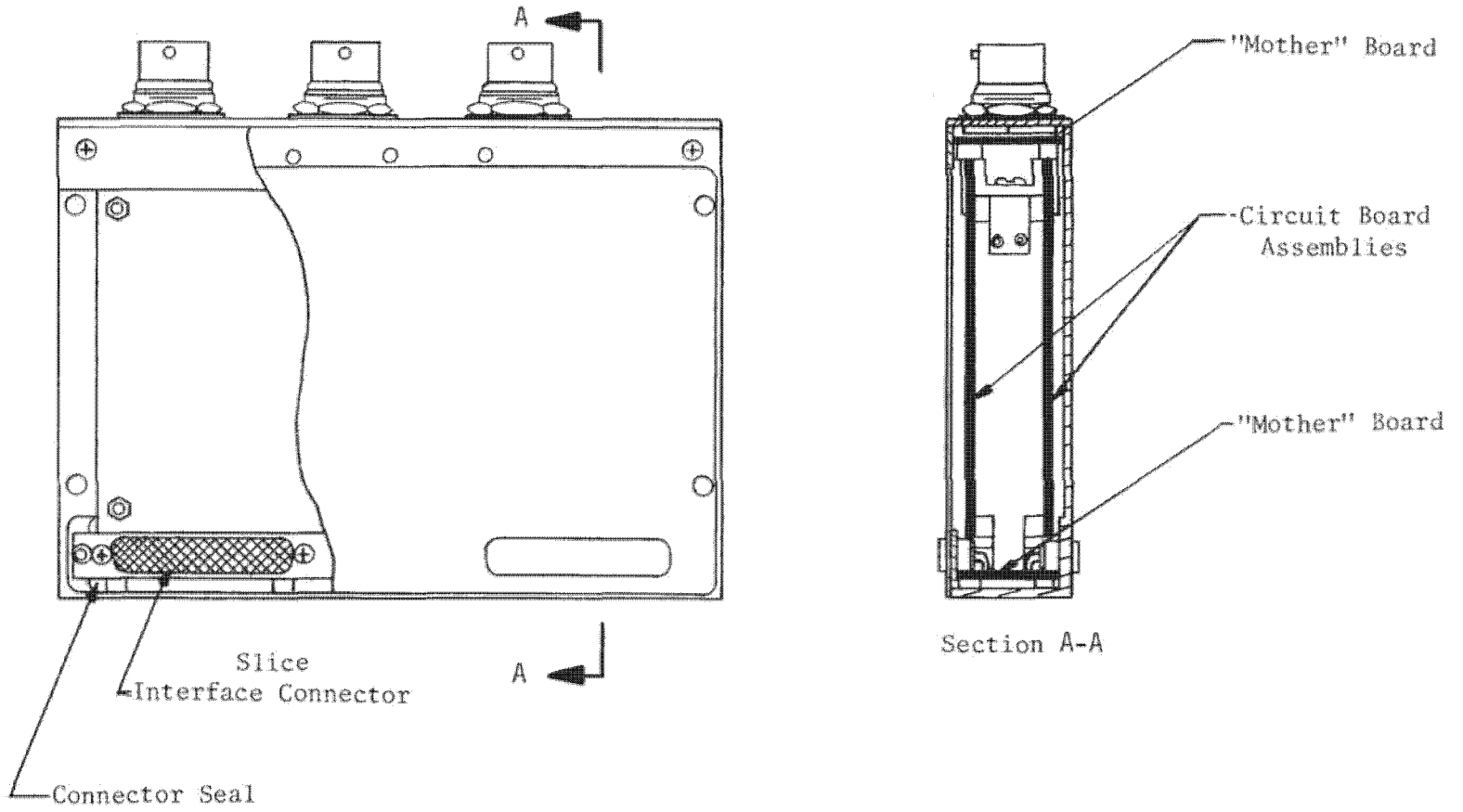


Figure 3.10-21. Typical AMU and DMU Mechanical Construction

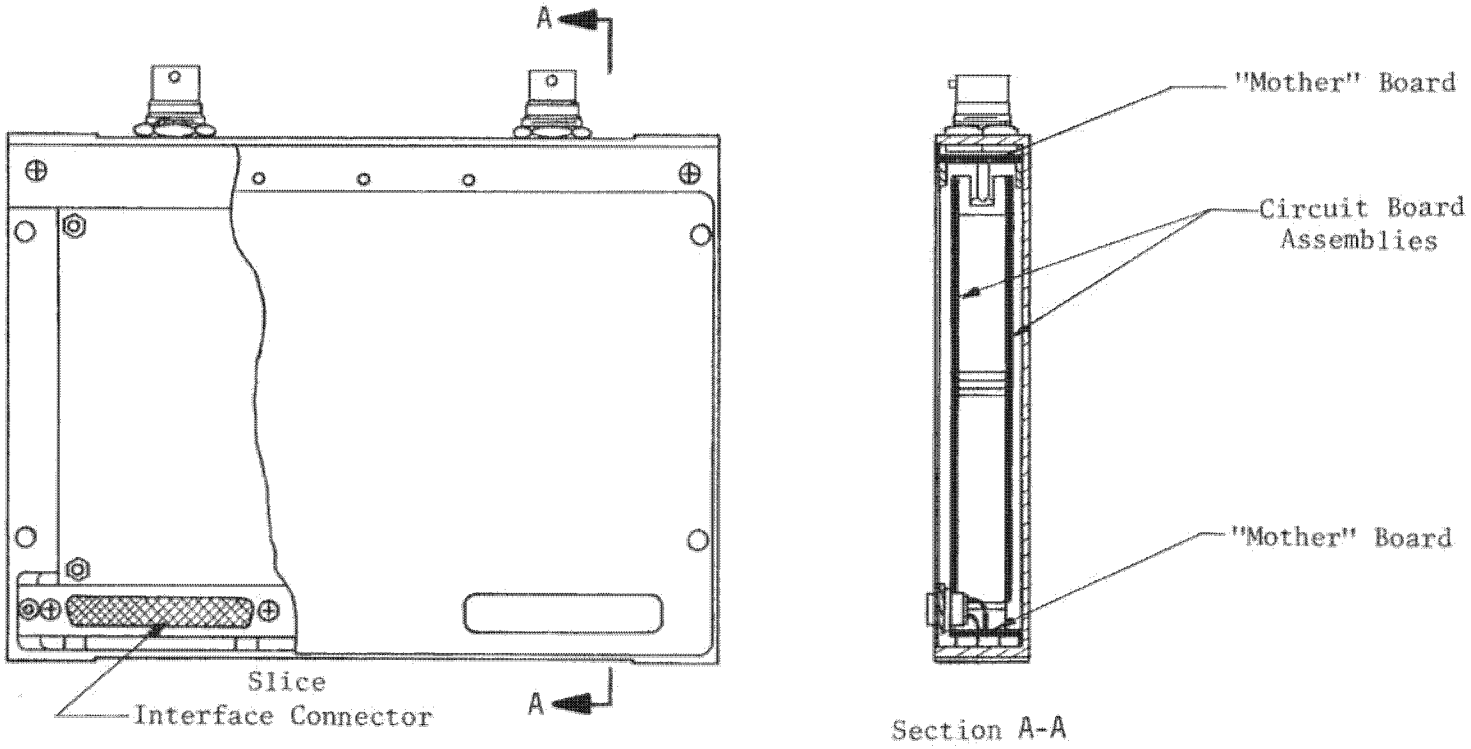
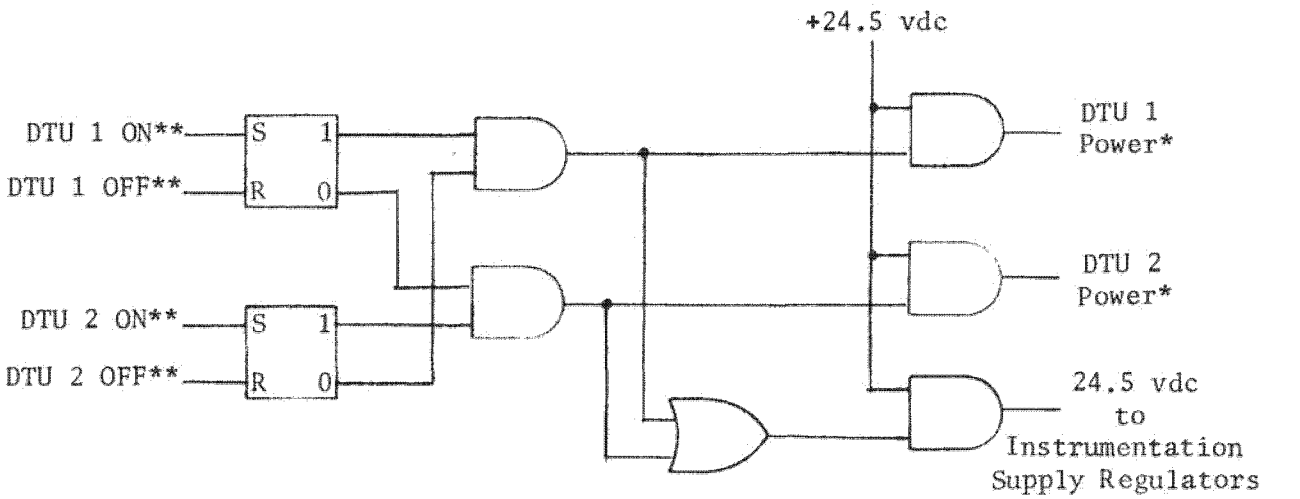


Figure 3.10-22. Converter Unit Mechanical Construction

10.3.2 Slave DTU Power Control

The telemetry system is designed such that only one half of each DTU in the system and only one MDTU are powered at any given time. If, through some failure, both halves of a slave DTU were powered simultaneously, each would reply to a valid data channel address signal for that DTU and the resultant interference between the reply signals at the MDTU would prevent accurate telemetry readings. To avoid this situation in the PPS/DP EAC, the power switches in the power monitor and control unit are interconnected as shown in Figure 3.10-23. Power is supplied to one side of the DTU only if the opposite side is off. If both sides are commanded ON, neither will receive power. However, as soon as one side is commanded OFF, power will again be provided to the opposite side (reference Part 3, Section 7).



*Fusing not shown
**For CP command logic:
Reference Part 3, Section 9.

Figure 3.10-23. DTU Power Control Logic

The DTU switches also control power for the +5 and ±15 vdc instrumentation supply regulators, as well as the pressure transducer (IMP 5019). Power is supplied to these whenever either DTU 1 or DTU 2 is on.

10.3.3 DTU Redundancy and Block Functions

As previously indicated (Section 10.3), each half of the PPS/DP EAC DTU slave is completely redundant except for common data input connectors. On the output side (the MDTU/DTU interface), each DTU half has two data channel address (DCA) and two serial pulse code reply (spc) circuits. One set is connected to MDTU A and the other to MDTU B. The circuits are designed such that either an electrical open or electrical short on any DCA or spc circuit in one side of the DTU will not prevent operation of that side, using the opposite set of DCA and spc circuits (and, necessarily, the opposite MDTU).

Internally, both sides of the DTU are powered from their associated power converters. The common input data channels are connected to electrically independent sets of processing circuitry for sides 1 and 2 (input gates, address decoders, A/D converters, etc.), and each of the two input gates for a single data source has the same DCA.

The various functions of the DTU are divided between the two basic types of building blocks in such a way as to permit easy interconnection of different combinations of blocks. The CU contains a single power supply unit and the data circuitry necessary to perform those tasks common to all processing:

(1) Power supply unit:
   a) DC-DC conversion
   b) Power switching
   c) Temperature instrumentation

(2) Data processing circuitry:

a) Address reply party line interfacing

b) Multiplexer interfacing (AMU or DMU)

c) A/D conversion

d) Data formatting

The multiplexer units decode the data channel address from the converter units and sample the proper data channel. Since each multiplexer type handles a different form of data (analog or digital), the circuitry involved is somewhat different. However, the basic purpose of either unit remains the same. The following Sections describe each of the three blocks in greater detail, beginning with the CU (Section 10.3.3.1) and followed by the AMU (Section 10.3.3.2) and DMU (Section 10.3.3.3).

10.3.3.1 Converter Unit. Figure 3.10-24 is a block diagram of the basic CU which illustrates the signal flow during operation. Since the unit is fairly complex, the major blocks will be discussed individually to illustrate the operations more clearly.

10.3.3.1.1 Power Supply. The power supply consists of a switching preregulator with a magnetically coupled load-sensing circuit for line and load regulation and a transistor chopper circuit. The output voltages from the primary transformer (+12v, -12v, and +5v) are full wave rectified and filtered (C-L-C Pi filters) to produce the necessary operating voltages. A separate series regulator generates -5 volts from the -12-volt filtered output. In the event of a high current or overvoltage condition, a shutdown circuit will inhibit the chopper and preregulator. The inhibit is removed automatically when the fault is cleared. The input power on/off control circuit and the internal power monitor of the unit are not used as the PPS/DP EAC supplies switched power to the DTU from the PM and C.

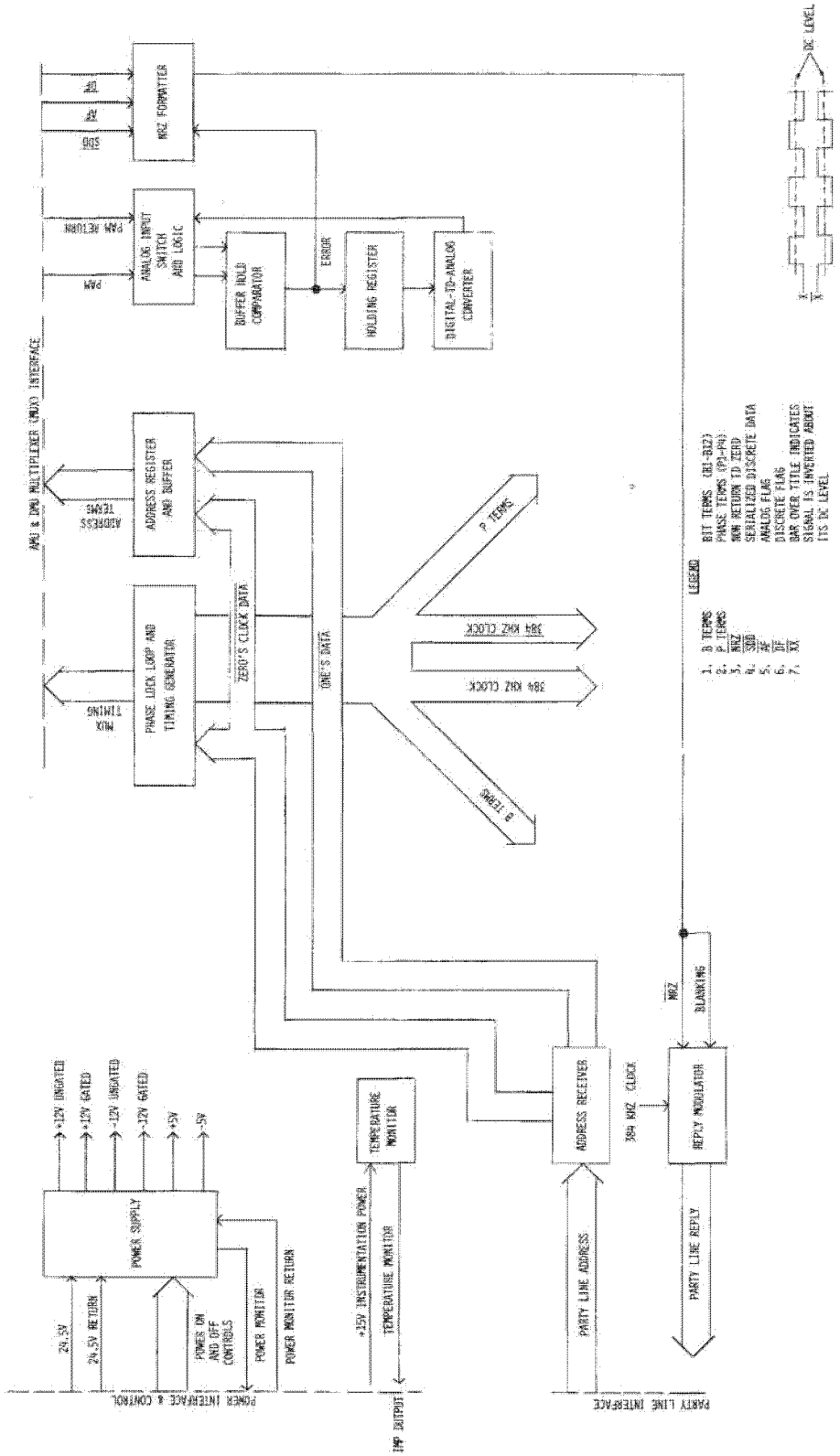


Figure 3.10-24. CU Block Diagram

To conserve power, the DTU incorporates a gated power scheme. Circuits receiving gated power are on for only a portion of the total time the DTU is powered, with the duty cycle dependent on the address/reply usage rate for the DTU.

The +5-volt gated power is supplied each time an address is received that is not a dead code (an address with bits G1 through G5* all logic zeros). Coincident with this, a signal from the converter unit turns on all +5-volt logic in the multiplexer units. Unless an analog flag (AF) or discrete flag (DF) is received from a multiplexer, signifying that the MDTU requires a reply from that slice, the 5-volt power will turn off after approximately 9 microseconds and a signal from the converter unit will turn off all multiplexer +5-volt supplies.

In the event a flag is received, the mutliplexer off signal from the CU turns off all multiplexers except the one responding with a flag. The power down command for the converter is inhibited for two-word times and the ±12-volt switches are activated for data processing and reply. If at the end of two-word times a new potentially valid address is received, the switched power remains on awaiting a flag from the multiplexers, and all +5-volt multiplexer supplies are turned on. If no flag is received, the +5-volt and ±12-volt switches are disabled.

The following circuits are those receiving gated power in the CU:

(1) Timing generator:
   a) Bit counter
   b) Multiplexer (mux) timing
   c) A/D converter timing

*Group address bits: Reference Section 10.3.3.2

(2) Address register and buffers

(3) A/D converter (D/A converter; holding register; buffer-hold comparator (BHC); analog input switch)

(4) NRZ formatter

(5) Reply modulator and cable driver

10.3.3.1.2 Address Receiver. The address receiver interfaces with the DCA party line and acquires data and clock information from received addresses.

The channel address signal is a trilevel, amplitude-modulated sinusoid with a fundamental frequency of 384 KHz. The signal length is 12 bits (or 12 cycles) with 1 bit for word synchronization, a 10-bit channel address code*, and 1-bit time for execution.

A binary zero is represented by low-level modulation and a binary one by high-level modulation with respect to the dc signal level. For further information on signal characteristics and timing, refer to Section 10.4.2.

Voltage levels for the binary values are not set at absolute levels. Instead, the system is required to maintain a minimum ratio between levels for binary one's and zero's. In order to distinguish between the two, the address receiver establishes a reference voltage based on the peak level of the incoming signal (the word synchronization bit must be a binary one for this reason) and then detects binary values by comparison with the reference. The three basic circuits of the address receiver which perform these function are:

(1) The linear amplifier

(2) The peak detector

*Group-channel code: Reference Section 10.3.3.2

(3) The "one's and "zero's" data comparators

Figure 3.10-25 is a block diagram of the address receiver.

Operation of the receiver is as follows: The DCA signal is transformer coupled into a noise suppression network and routed to a linear amplifier to boost the signal level. The amplified signal is then fed to the peak detector to provide a dc reference voltage equal to the peak ac voltage. The resistor divider networks at the output set the threshold voltages for the one's data and zero's data comparators. The output of the one's comparator provides a low-going pulse (or $\overline{\text{one's data}}$)* each time a binary one is received. The zero's comparator is set such that a low-going pulse (or $\overline{\text{zero's data}}$)* is provided each time a binary one or zero is received.

10.3.3.1.3 Timing Generator. The timing generator accepts the $\overline{\text{zero's data}}$ signal from the address receiver and generates all the basic timing signals for the DTU, locked in phase with the $\overline{\text{zero's data}}$ signal. The generator circuit, Figure 3.10-26, consists of a phase lock loop (PLL), a four term phase generator, a 384 KHz clock generator, a 12-bit counter, and timing logic for the analog and discrete multiplexers.

The PLL derives a 1536 KHz (384 KHz · 4) clock signal from the address receiver's 384 KHz $\overline{\text{zero's}}$ clock. The 1536 KHz clock is phase locked to the $\overline{\text{zero's}}$ clock and drives the phase generator.

The phase generator employs a 4-bit shift register clocked by the 1536 KHz signal with an error correction loop to generate the four-phase terms. Thus, each phase term (P1 through P4) corresponds to a specific quarter segment of a bit time (see the timing diagram on Figure 3.10-26). Phases $\overline{\text{P3}}$ and $\overline{\text{P4}}$ are

*A bar over the signal descriptor indicates the signal is inverted: i.e., the signal level drops when a pulse is output.

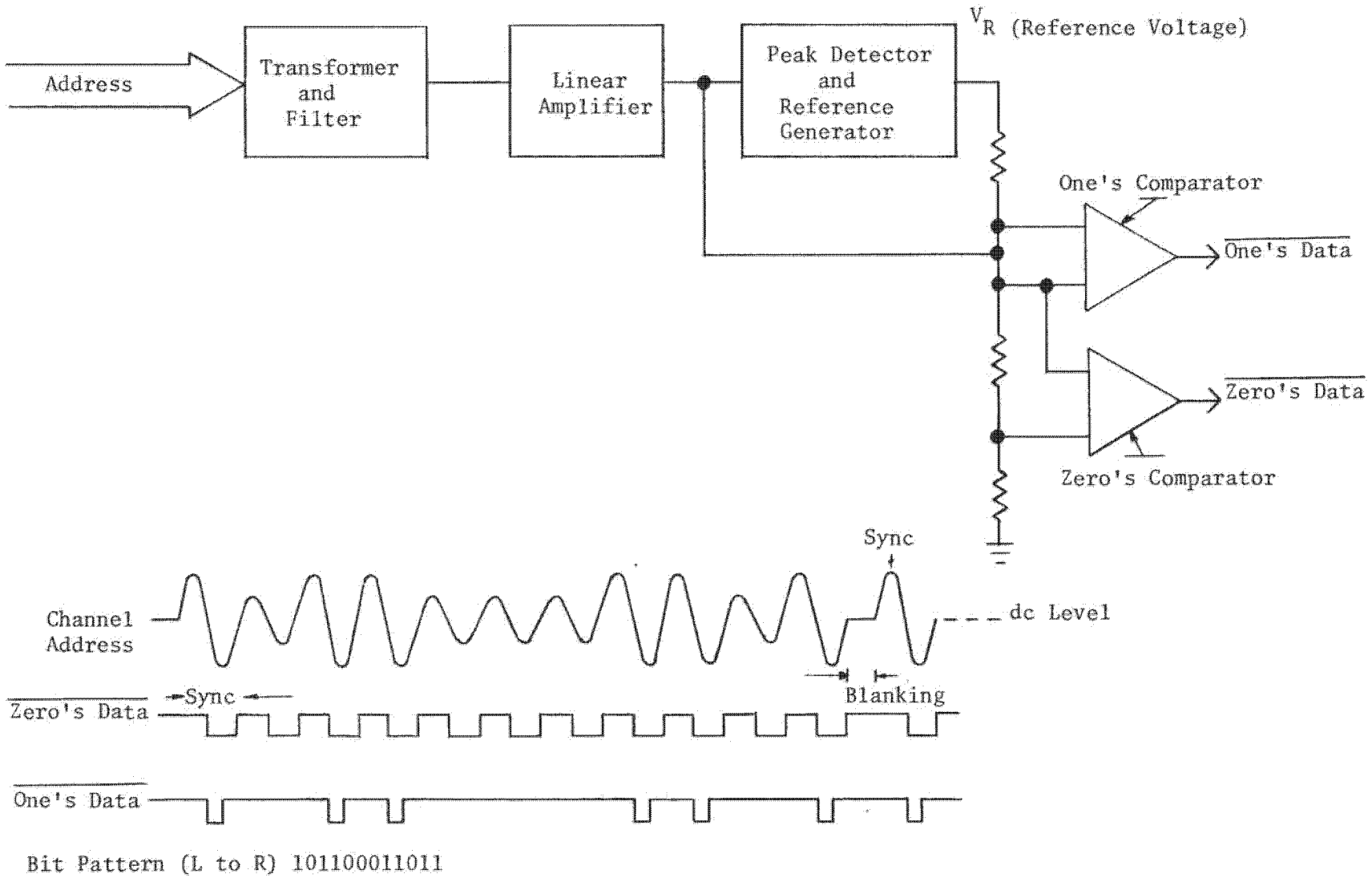
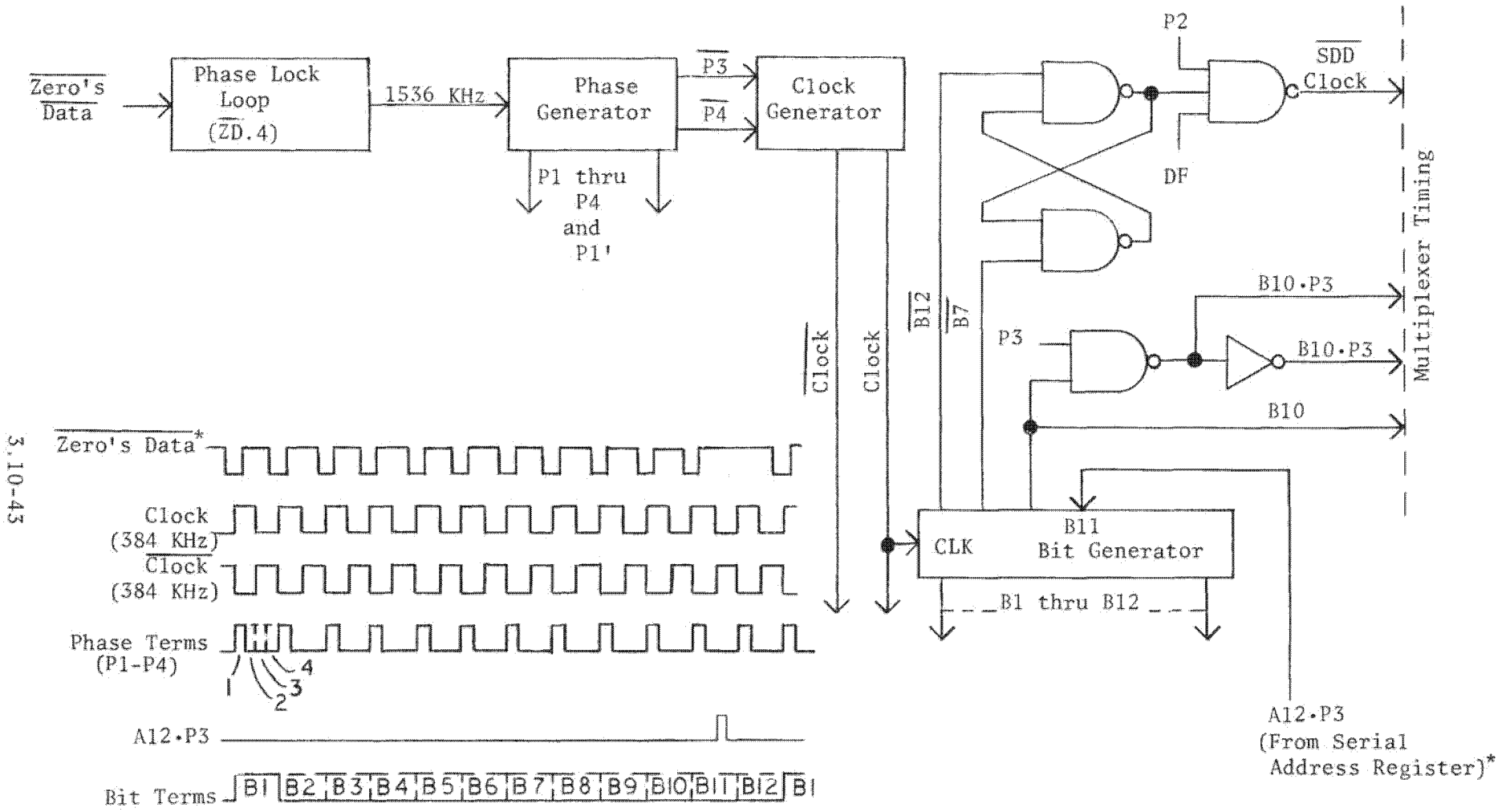


Figure 3.10-25. Address Receiver Block Diagram



*See Figure 3.10-27

Figure 3.10-26. Timing Generator Circuit

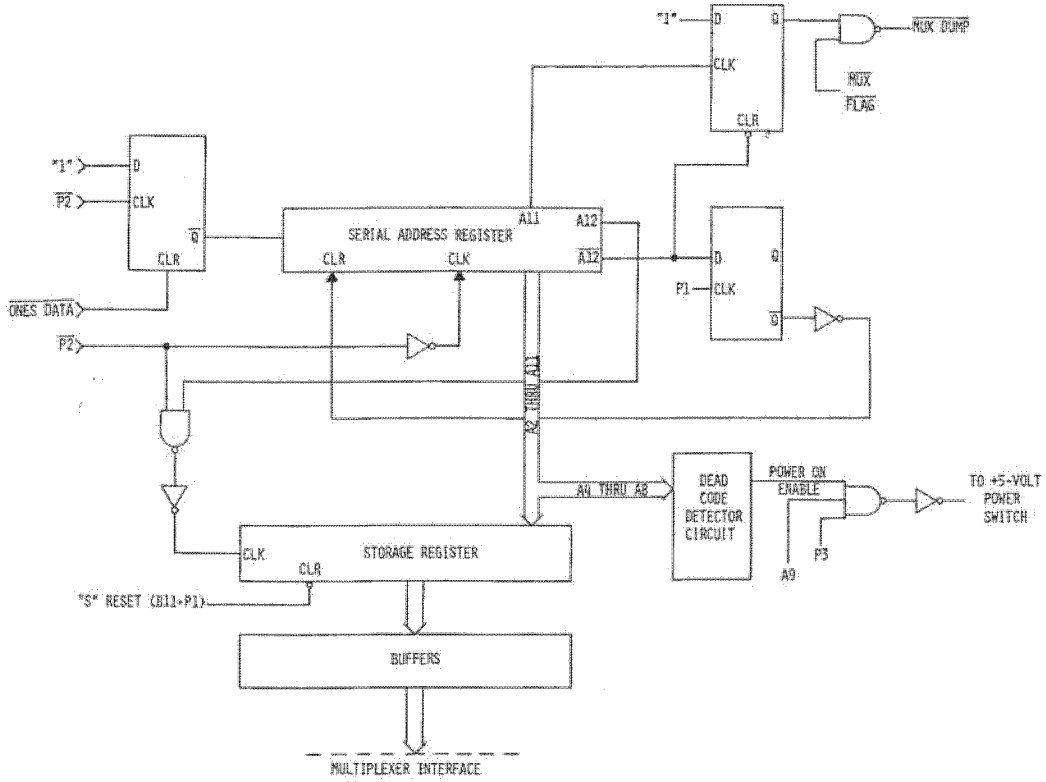
used to drive the clock circuit, ensuring that the 384 KHz clock signal is synchronized to the incoming data.

The bit generator is a 12-bit shift register clocked by the 384 KHz signal. Bit 12 is fed back to the input of the first state producing a continuous 384 KHz pulse train.

The timing logic is composed of several smaller circuits which use the bit terms and phase terms to produce the clock signals for analog and discrete multiplexer operation. The $\overline{SDD}$ clock consists of seven pulses which clock discrete data from the DMU into the converter. The remaining outputs B10, B10·P3, and $\overline{B10 \cdot P3}$ are used in various ways within the AMU and DMU slices and will be discussed in following Sections.

10.3.3.1.4 Address Register. The address register which is shown in Figure 3.10-27 receives the channel address from the address receiver and clocks it into a serial input shift register sync bit first. When the sync bit reaches stage A9, the dead code detector circuit turns on the +5-volt logic power if there is a logic 1 in any position of stages A8 through A4 which at this point contain address bits G1 through G5. When the sync bit reaches stage A12 indicating that the channel address is fully loaded, the 10-bit functional address portion is parallel loaded into the storage register and associated buffers (assuming +5-volt logic power was turned on), and the serial input register cleared. The parallel address information is then presented to the multiplexer(s) for a full-word time (12-bit times) while a new code is being clocked into the serial address register.

To aid in understanding the address register block diagram, Table 3.10-3 presents a logic chart for the "D-type" flip-flops employed. This type of device is used in several places throughout the DTU and appears on many of the following block diagrams.



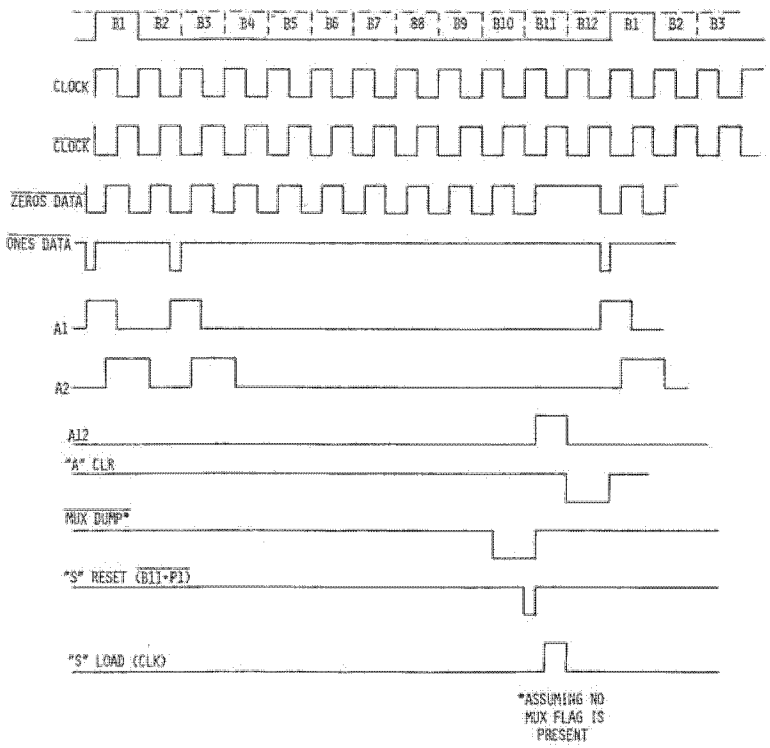


Figure 3.10-27. Address Register

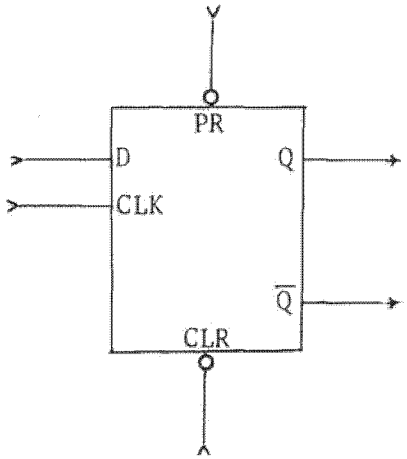
Approved for Release: 2017/02/14 C05097359

TABLE 3.10-3

D-TYPE FLIP-FLOP LOGIC TABLE

Function Table

Inputs				Outputs	
Preset	Clear	Clock	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_o	$\overline{Q}_o$



D-Type Flip-Flop Symbol

H = High level (steady state); L = Low level (steady state)

X = Irrelevant

↑ = Transition from low to high level

Q_o = The level of Q before the indicated input conditions were established.

*This configuration is nonstable. It will not persist when preset and clear inputs return to the inactive (high) level.

10.3.3.1.5 A/D Converter. The A/D converter is an eight-bit successive approximation digitizing circuit which accepts analog input signals from the multiplexer units and produces eight-bit equivalent digital signals, the least significant bit of which represents 0.02 volt. Binary codes 00000000_2 and 11111111_2 are not permitted; code 00000001_2 is used to represent either 0.00 volt or an open circuit, and code 11111110_2 represents either 5.06 volts or an overvoltage condition.

The basic elements of the A/D converter (Figure 3.10-28) include:

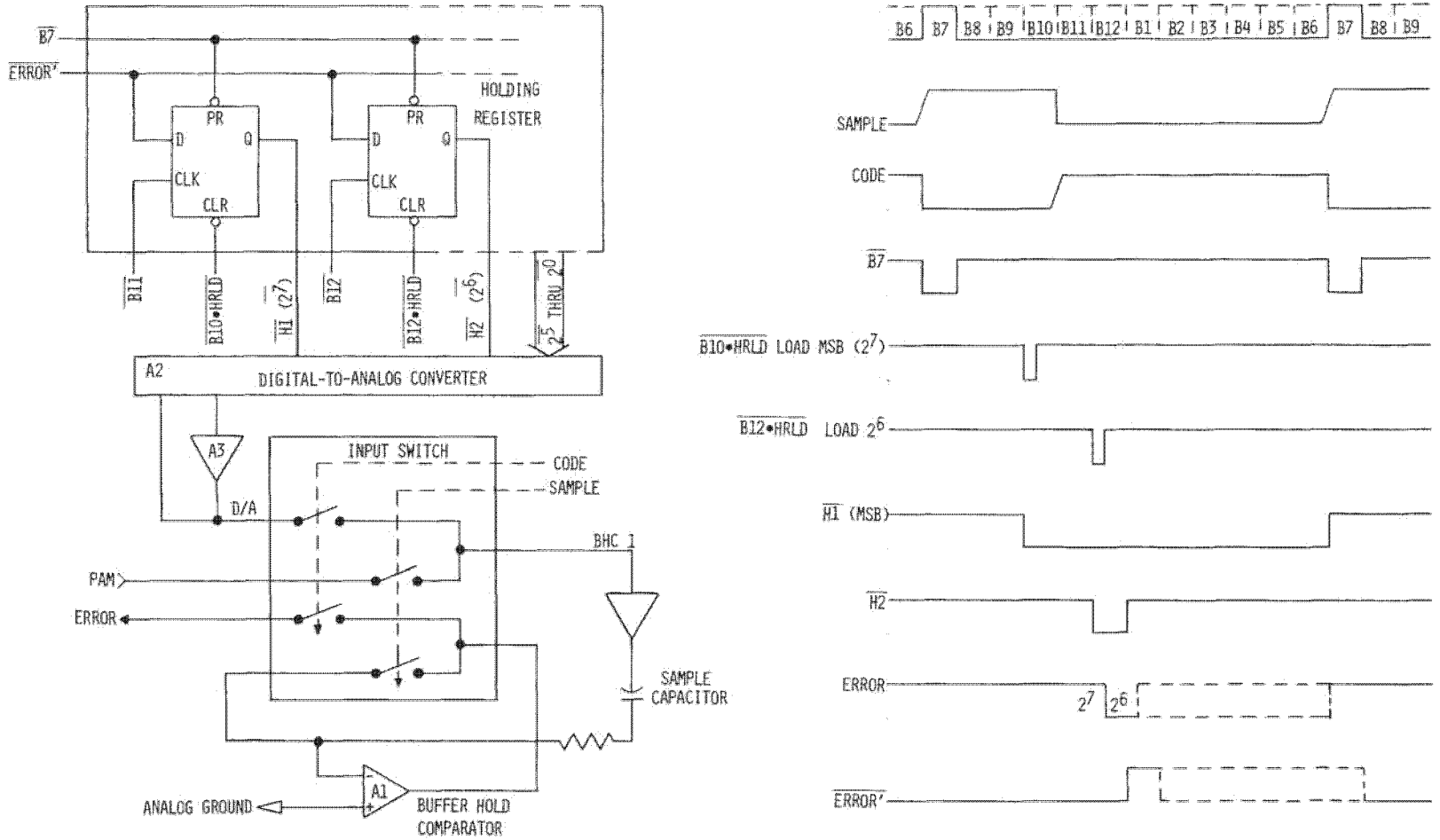
(1) An analog input switch
(2) A Buffer Hold Comparator (BHC)
(3) A holding register
(4) A digital-to-analog (D/A) converter

The analog input switch is a solid-state switch which connects either the pulse amplitude modulated (PAM) signal (the analog sample) or the D/A converter comparison voltage to the BHC.

The BHC is used to sample the analog voltage from the multiplexer unit and to hold the sample accurately during the encode (digitizing) period. During the digitizing cycle, the BHC acts as a voltage comparator.

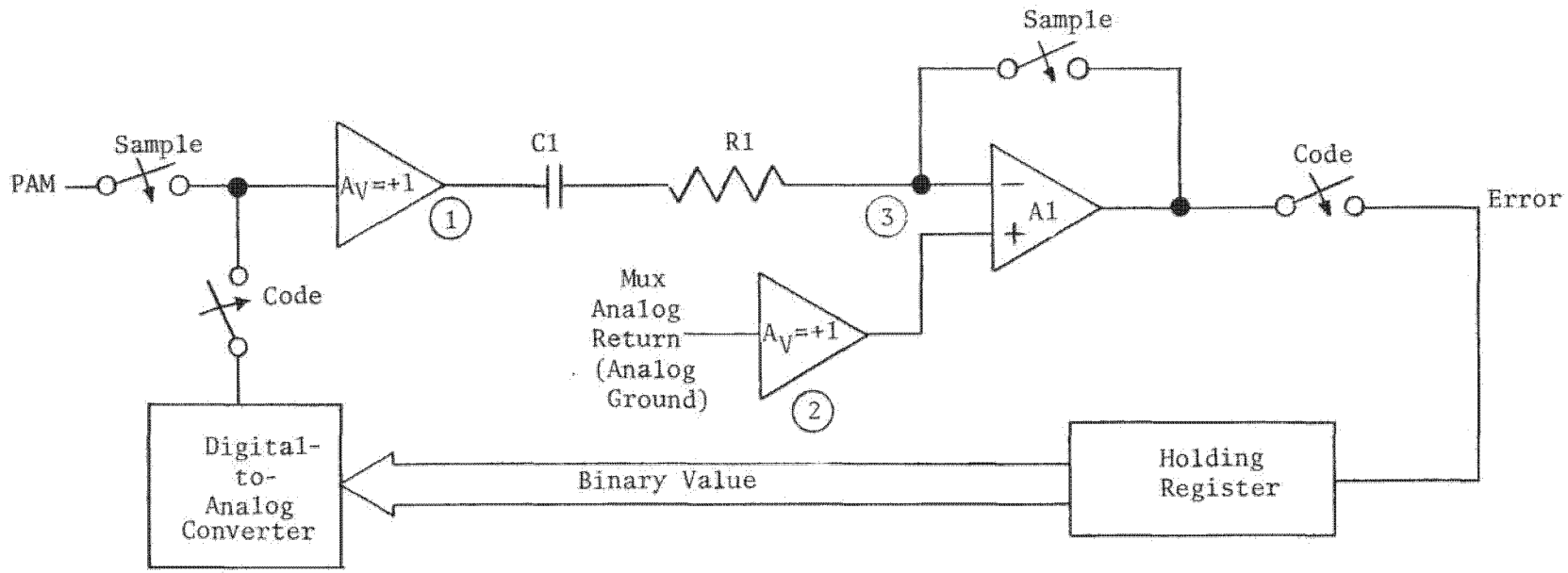
The D/A converter provides a precision analog reference voltage to the BHC for comparison purposes. The level of the reference voltage is determined by the binary value of the holding register. The components of the converter consist of a monolithic D/A converter and a current-to-voltage (C/V) converter.

A block diagram of the full A/D converter circuit is shown in Figure 3.10-29 along with the sample/encode algorithm and a typical encoding example. The



NOTES:
1. HRLD: HOLDING REGISTER LOAD
2. A "HIGH" ERROR SIGNAL INDICATES THE BIT IS TO BE RETAINED (BINARY 1)
3. FOR EXPLANATION OF TIMING SEE SECTION 10.3.3.1.5

Figure 3.10-28. Analog-to-Digital Converter - Basic Elements



Encoding Sequence for a 3-Volt Sample

	Current Voltages ①	②	③	Switch Position	Encoder Output Level
A.	3.000	0	0.000	Sample	-
B.	2.530	0	-0.470	Encode	1
C.	3.810	0	+0.810	Encode	0
D.	3.170	0	+0.170	Encode	0
E.	2.850	0	-0.150	Encode	1
F.	3.010	0	+0.010	Encode	0
G.	2.930	0	-0.070	Encode	1
H.	2.970	0	-0.030	Encode	1
I.	2.990	0	-0.010	Encode	1

Encoder Algorithm

IF $V_1 - V_{1,3} < V_2$ Encode"1"

IF $V_1 - V_{1,3} > V_2$ Encode"0"

Where:

$V_{1,3}$ represents voltage drop from ① to ③.

Figure 3.10-29. Analog-to-Digital Converter - Block Diagram, Sample/Encode Algorithm and Encoding Example

analog voltage to be sampled is connected to the input buffer amplifier of the BHC portion of the converter. This buffer exhibits extremely high input impedance and near unity gain ($A_V \approx 0.9998$) resulting in accurate sampling of the PAM signal. The output of the buffer amplifier is routed to one side of the sample capacitor (C1) with the opposite side of the capacitor tied to the inverting input of A1 and to the output of A1 through the sample switch. During the capacitor charge period (approximately 10 microseconds), the sample switch is closed, forcing A1 into a unity gain mode and causing C1 to charge to a value virtually equal to the BHC input voltage. Any common mode offset voltage will be ignored since the sample capacitor is charged differentially and both the sample and D/A reference voltage, to which the sample will be compared, will experience the same offset.

Once the sample has been acquired, the switch which forced unity gain is opened and the code switch is closed, forcing A1 into an open loop gain mode for use as a comparator. At this time, the D/A precision voltage output is presented to the BHC input. The first voltage level entering the BHC is equivalent to half scale $\left(\frac{5.060}{2} = 2.530\right)$. On the basis of the half-scale voltage being greater or less than the charge on C1, the A1 amplifier correspondingly shows high or low (the error signal). This information is presented to the holding register, and causes the holding register either to retain the half-scale bit (binary 1) or reset the bit (binary 0). This sequence is repeated for quarter scale*, eighth scale, etc. At the end of the encode time (8 bits), the information stored in the holding register is the digital equivalent of the unknown analog sample.

Timing of the comparison sequence is illustrated on the signal diagram in Figure 3.10-28 for a sample of 2.560 volts. During the sample period, the

*Approximate quarter scale. Bit 2 adds 1.28 volts, Bit 3 adds 0.64 volt,etc.

holding register is cleared (at bit-time B7) and the most significant bit set to logic 1 (during bit-time B10). The output of the D/A converter becomes 2.530 volts for the start of the coding period, reflecting the state of the holding register.

When the coding period begins, the error signal remains high which indicates the sample exceeds 2.530 volts, and the first digital bit is retained ($\overline{HI}$ remains low). The next most significant bit is set to logic 1 during bit-time B12. The converter output becomes 3.810 volts and the error signal falls to indicate the sample voltage is less than 3.810 volts. Bit H2 (2^6) is reset to zero during the remainder of bit-period B12. The process continues through all eight bits with the final comparison made during bit-time B6.

10.3.3.1.6 NRZ Formatter. The non-return-to-zero (NRZ) formatter (Figure 3.10-30) produces the $\overline{NRZ}$ and blanking signals which drive the reply modulator. $\overline{NRZ}$ is an 8-bit data word which represents either the digitized analog signal or an eight-bit discrete word. The $\overline{NRZ}$ signal is generated by accepting BHC error signals representing the digitized analog sample (most significant bit (MSB) first), or DMU $\overline{SDD}$ signals (MSB bit first) and placing each data bit in the proper time frame.

Enabling of the appropriate data multiplexer channel to accept $\overline{SDD}$ or error data is controlled by receipt of an analog or digital flag ($\overline{AF}$ or $\overline{DF}$) which sets one or the other of two flip-flops to logic 1. The flip-flop outputs then enable the appropriate gate for data transmission through the data multiplexer to produce the NRZ signal.

The least significant bit (LSB) complement decision circuit decodes the NRZ signal to detect a transition in the data reply. If no transition occurs and an analog signal is being processed, the LSB is complemented to prevent an all one's or all zero's reply.

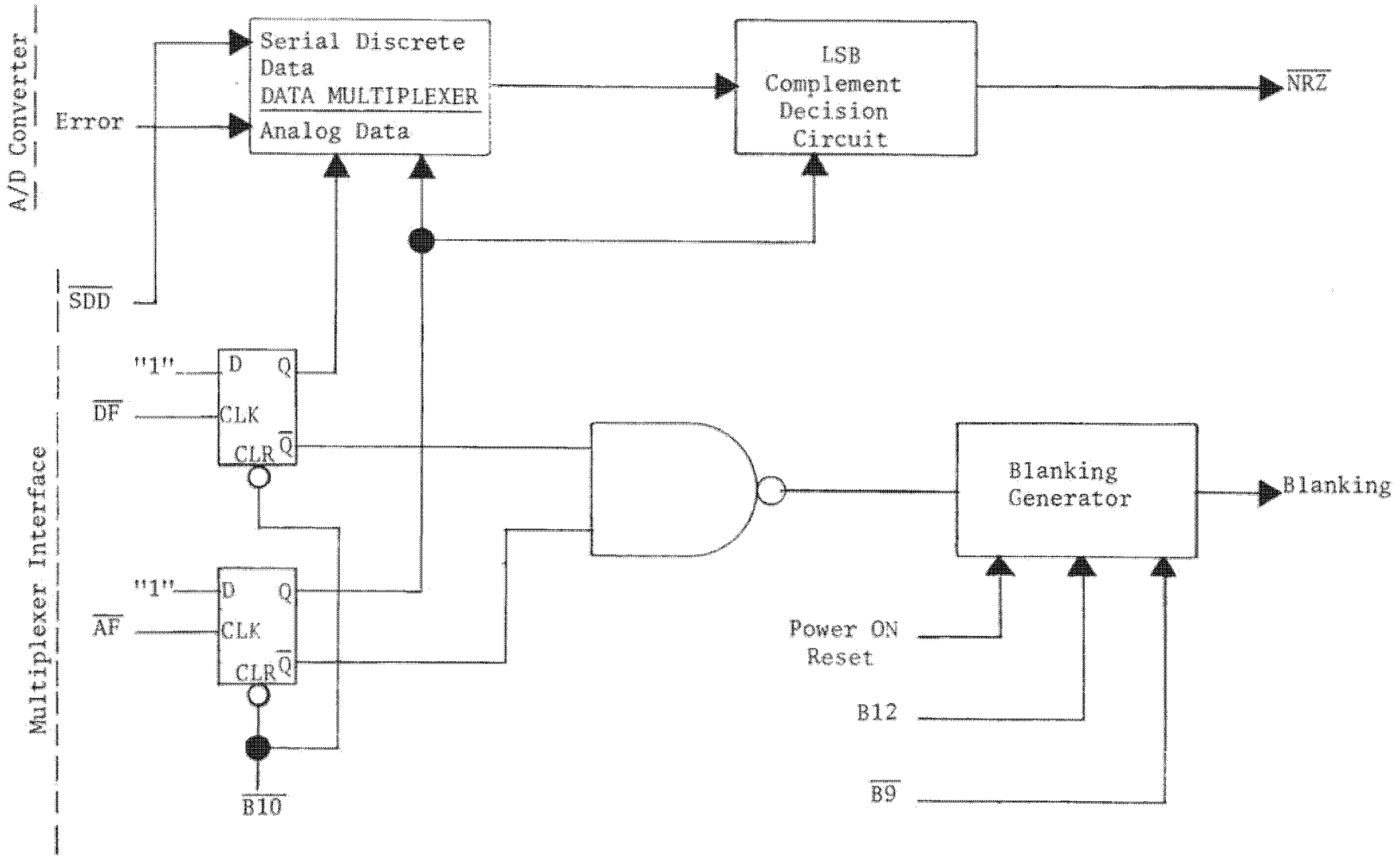


Figure 3.10-30. NRZ Formatter

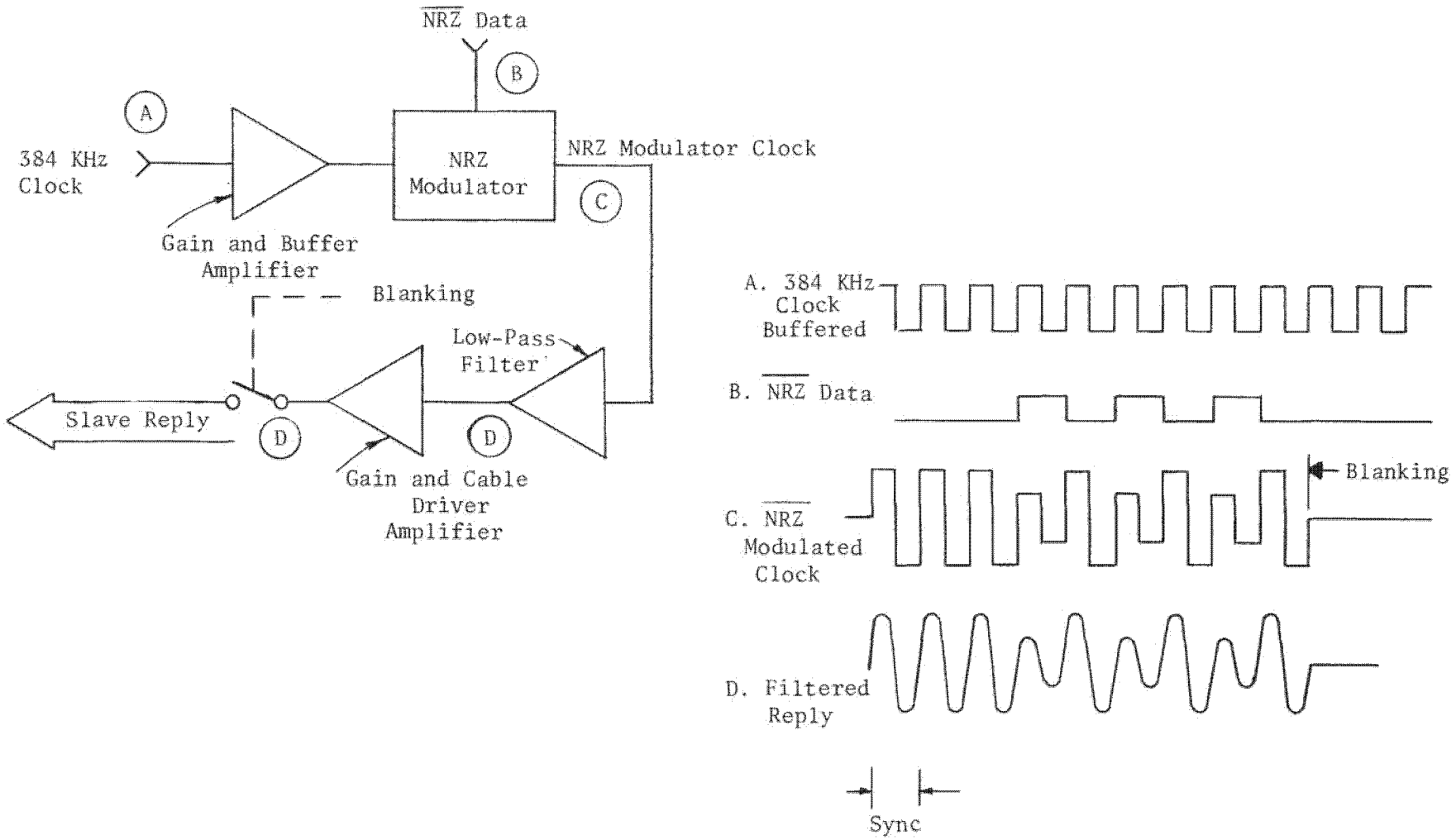
The end result of processing by the formatter is the $\overline{NRZ}$ data signal and the blank signal which enables the reply modulator output driver for transmission from Bit 12 through Bit 8 whenever an $\overline{AF}$ or $\overline{DF}$ has been received.

10.3.3.1.7 Reply Modulator. The reply modulator modulates the 384 KHz clock with the $\overline{NRZ}$ and blank signals from the NRZ formatter. After filtering, the reply is transmitted over two separate party lines, one connected to MDTU A and the other to MDTU B.

Operation of the reply modulator circuitry is illustrated by the timing signals in Figure 3.10-31. The unfiltered reply waveform is generated by modulating the 384 KHz clock with $\overline{NRZ}$ reply data. The amplitude of a modulated bit is a "one" or a "zero" depending on the $\overline{NRZ}$ bit driving the modulator at that time. The reply waveform is then filtered to produce a bilevel sinusoidal waveform. This is then amplified and buffered by the cable driver amplifier. During blanking and power off periods, a switch controlled by the blank signal from the NRZ formatter opens the primary of the reply output transformer.

In term of characteristics, the reply signal from the DTU slave is a trilevel, amplitude-modulated sinusoid at the fundamental clock frequency of 384 KHz. The signal length is 12-bit times with 1 bit for word synchronization, 8 bits for the data code (MSB first), and 3-bit times for execution. A binary zero is represented by low-level modulation and a binary one by high-level modulation. As in the case of DCA signals, bit levels are determined by the ratio between the low and high levels of the reply signal rather than absolute voltages. For further information on signal characteristics and timing, refer to Section 10.4.2.

10.3.3.2 AMU Unit. The AMU provides redundant facilities (except for input connections) for multiplexing 128 channels of 0-5-volt analog information. Each CU of the PPS/DP EAC DTU provides power to one of the redundant portions,



3.10-55

Figure 3.10-31. Reply Modulator

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resulting in independent channels for DTU 1 and DTU 2. The components for one portion are mounted on a single board and include eight 16-channel submultiplexers, a main multiplexer, and associated circuitry. Selection of a single channel out of the submultiplexers is performed by the 10-bit data channel address code, using three bits to select the AMU (or slice), three bits to select the submultiplexer, and four bits to designate a single channel on the submultiplexer. In practice, this code is divided into two 5-bit segments referred to as group and channel. Figure 3.10-32 is a typical group-channel code showing the group-channel division and the standard binary-to-octal conversion.

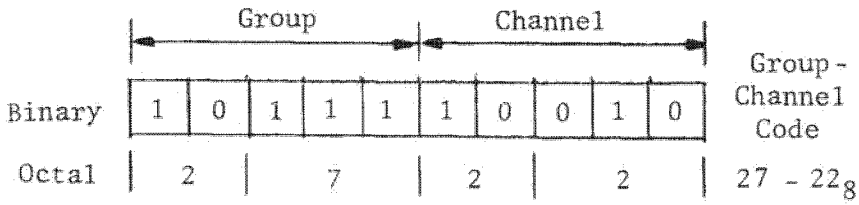


Figure 3.10-32. Group-Channel Address Code

This method of referencing data codes is based on a previous DTU design and remains the standard format although it no longer is indicative of the channel selection procedure.

Figure 3.10-33 is a block diagram of one AMU slice. The slice receives power and buffered channel address signals from the converter unit. If the address is valid, an analog flag ($\overline{AF}$) is returned to the CU, and the selected input channel voltage signal is supplied to the A/D converter. The circuitry of the AMU consists of the following:

(1) The group (slice) code detection circuit
(2) The submultiplexer decode circuit

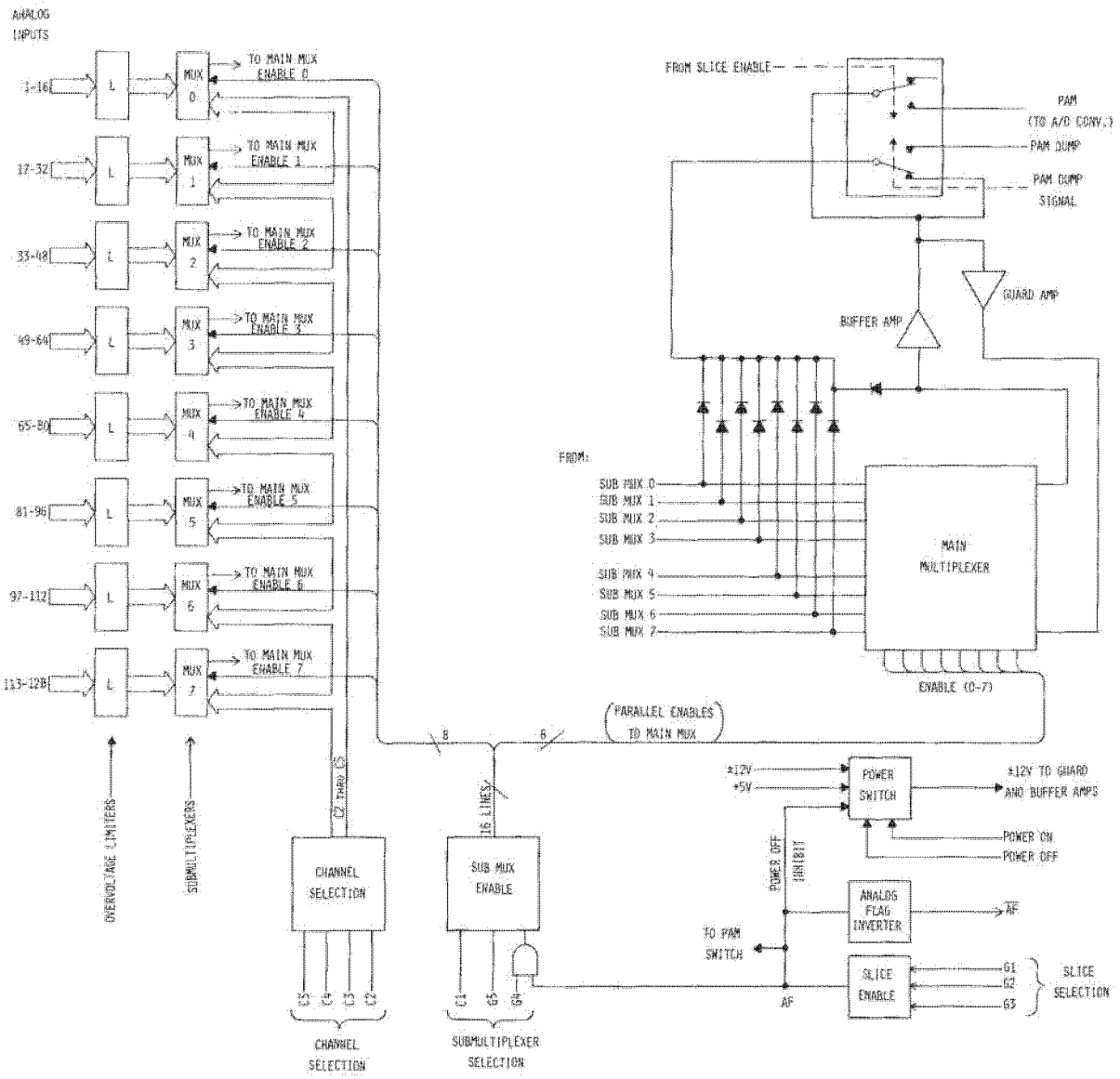


Figure 3.10-33. AMU Block Diagram

(3) The submultiplexers
(4) The main multiplexer
(5) The overvoltage protection circuits
(6) The PAM "dump"
(7) The guard amplifier
(8) Power switching circuitry

10.3.3.2.1 Group Code Detection. Each AMU is assigned a predetermined group code which is established by hardwiring of a four-bit integrated circuit comparator. This code is continuously compared with the three most significant bits (G1, G2, and G3) of the address sent from the CU. Upon successful comparison, a logic one signal (the AF is output to enable the submultiplexer decode circuit (Section 10.3.3.2.2)).

In addition, the flag keeps ±12-volt power on for the guard and buffer amplifiers, closes the PAM switch (for sample output), and is output for use in the CU.

10.3.3.2.2 Submultiplexer Decode. The next three CU address terms (G4, G5, and C1) are used by the submultiplexer decode circuit, when enabled, to generate one of eight submultiplexer enables. The selected enable activates the appropriate submultiplexer through which data is to be acquired.

10.3.3.2.3 Submultiplexers. The submultiplexers are 16-channel integrated circuit analog signal multiplexers. Address bits C2 through C5 are fed in parallel to each submultiplexer to select one out of the 16-channels. The chip enable, which is controlled by the submultiplexer decode signal, must be a logic one to select any of the channels. Table 3.10-4 summarizes the group-channel address code selection of an analog input.

TABLE 3.10-4

AMU ADDRESS RECOGNITION

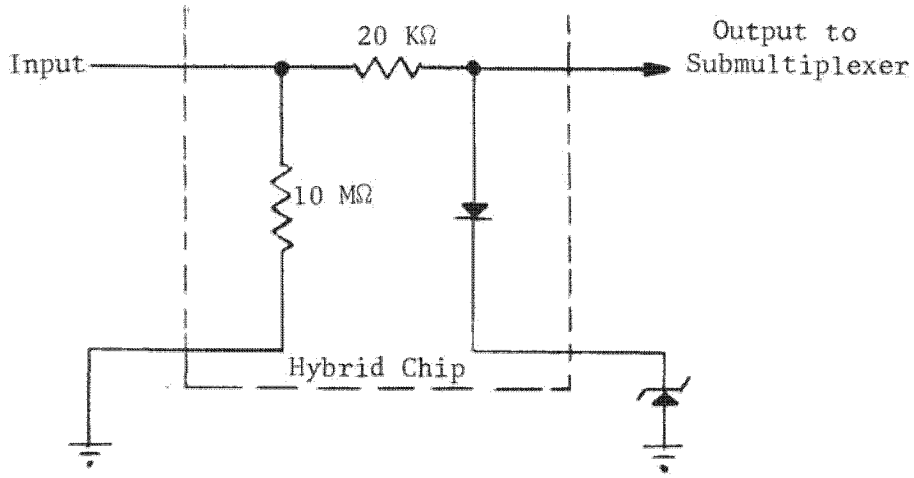
G1 G2 G3	G4 G5 C1	C2 C3 C4 C5
Slice Enable	Submux Enable	Submux Channel Code

G4	G5	C1	Submux Enable
0	0	0	EN 0
0	0	1	EN 1
0	1	0	EN 2
0	1	1	EN 3
1	0	0	EN 4
1	0	1	EN 5
1	1	0	EN 6
1	1	1	EN 7

C2	C3	C4	C5	Submux Channel
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8
1	0	0	0	9
1	0	0	1	10
1	0	1	0	11
1	0	1	1	12
1	1	0	0	13
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16

10.3.3.2.4 Main Multiplexer. The main multiplexer consists of two four-channel analog switches that are used to isolate the eight 16-channel sub-multiplexers. This isolation prevents a complete loss of data due to a defective input channel and enchances the response time of the analog sample line as a result of reduced capacitance loading. The switches are enabled by the same output lines which enable the submultiplexers, connecting the selected input to the main multiplexer output.

10.3.3.2.5 Overvoltage Protection. Each input analog channel is protected from excessive voltage through the use of a 20 KΩ resistor, a low leakage diode, and a zener diode clamp as shown in Figure 3.10-34.



NOTE: Figure illustrates
1 of 16 identical
channels per chip.

Figure 3.10-34. Typical Overvoltage Protection Network

Open channel encoding requirements are satisfied by a 10 MΩ pulldown resistor on the input side of each 5.1 KΩ input resistor. The resistors and diodes are integrated into dual-in-line ceramic packages providing 16 inputs per package. This protection network allows analog voltages in excess of 35 volts to be applied at the DTU analog inputs without damage to the submultiplexers.

10.3.3.2.6 PAM Dump. In order to satisfy the maximum feedback current requirement and enhance the charge transfer time of the analog sample lines, a dump of all submultiplexer and main multiplexer outputs is performed during periods when no sampling activity is occurring. The dump signal, which lasts approximately one-bit time, disconnects the dump line from the output of the buffer amplifier and connects it to -2 volts through a protective resistor. This effectively removes any charge accumulated in the PAM lines prior to the next sample period. After dumping, the output of the buffer amplifier is returned to the PAM and dump lines. If an AF is present during the dump period, the dump is inhibited, and the output of the buffer amplifier remains connected to the dump line, guarding the capacitance of the dump diodes for the sampling period. The sampling period lasts approximately 30 μsec and consists of a 20 μsec line charge period following selection of an input channel and a 10 μsec A/D converter sample period to charge a holding capacitor in the CU. (Reference Section 10.3.3.1.5.)

10.3.3.2.7 Guard Amplifier. The capacitance of Metal Oxide Semiconductor Field Effect Transistor (MOSFET) devices on the analog lines degrades the charge transfer characteristics of the AMU. For optimum performance, it is necessary to "guard" this capacitance by modulating the substrate voltage of the main multiplexer. A guard amplifier controlled by the PAM buffer amplifier performs this task and effectively nullifies the capacitive loading.

10.3.3.2.8 Power Switching. The power switching circuits provide a substantial savings in average power consumption by turning off all possible logic

whenever the multiplexer is not being addressed, while dissipating negligible power during power down operations. The power switching circuits are controlled by a pulse from the converter unit which turns on power whenever a group-channel address is received.

After allowing time for transients to settle, the CU provides the address to the multiplexer. If the group code is recognized (that is, matches the hardwired slice code), an AF is generated which inhibits the CU power off signal. If the group code is not recognized, the power off signal from the CU turns off the logic power switches.

10.3.3.3 Discrete Multiplexer Unit. The DMU provides redundant circuits powered by opposite CU's and capable of multiplexing 128 bilevel inputs grouped into eight-bit words. The same integrated circuit multiplexer used as a submultiplexer in the AMU is used as the multiplexing element in the DMU. Also, the group code detection, overvoltage protection, sample dump, and power switching circuits used in the DMU operate like those of the AMU and serve the same purposes.

The circuit organization shown in Figure 3.10-35 is such that bit 1 of each word (1 through 16) is fed through the same multiplexer. In a similar fashion, each of the seven remaining multiplexers receives bits 2 through 8 respectively for the 16 discrete words. The eight parallel discrete bits are checked for logic levels by eight parallel comparators. The comparator outputs are then loaded into an eight-bit shift register and clocked to the CU in a serial wave train (bit 1, or MSB first) by the serial discrete data timing signal.

10.3.3.3.1 DMU Address Recognition. The DMU employs two four-bit comparators to recognize the group code formed by the six most significant address bits sent from the converter unit (G1 through G5, and C1). The code of the DMU is established by hardwiring the terminals of the comparators to either 5

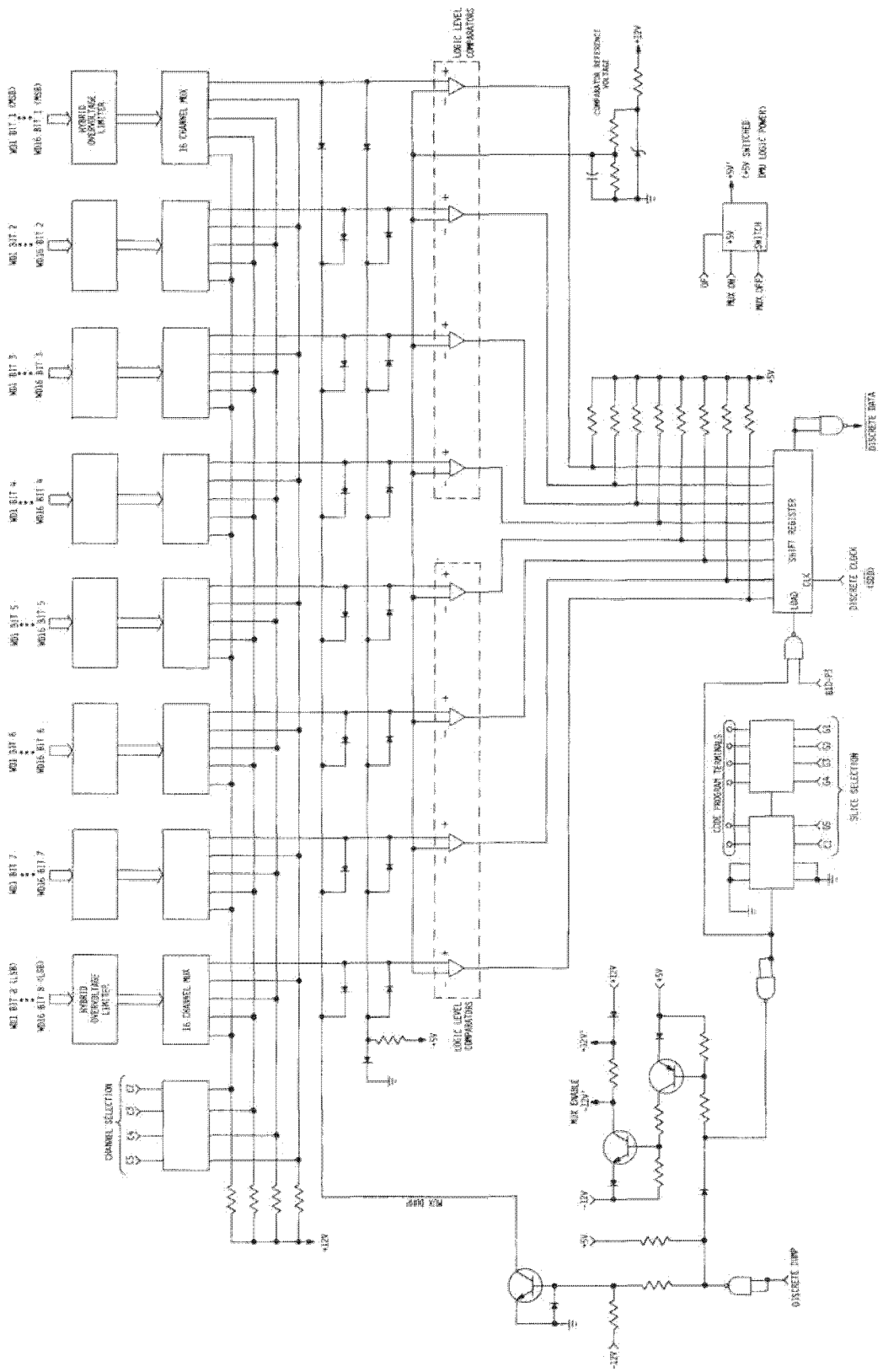


Figure 3.10-35. DMU Block Diagram

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volts or ground. Recognition of the address group code will generate a DF signal which is used to enable the eight multiplexers, and to maintain the switched power on for the DMU components, and is inverted to form the group code recognition symbol ($\overline{DF}$) for the CU.

The remaining four address terms (C2 through C5) are connected to the multiplexers through an enable circuit and used to select one of 16 data lines. The enable is controlled by the presence or absence of DF. Table 3.10-5 presents a truth table summarizing the channel (word) selection code.

10.3.3.3.2 Overvoltage Protection. Each input channel is protected by a network identical to that used for analog inputs. The zener diodes provide a voltage clamp to protect against high input levels, while the discrete diodes and resistors protect against negative-going spikes.

10.3.3.3.3 Discrete Dump. The discrete dump provides a dump of all eight multiplexer lines before they enter the comparator. The dump of the charge stored on these lines is through low leakage diodes and a transistor switch. As in the AMU, the dump signal occurs before the next address is given to the DMU.

10.3.3.3.4 Power Switching. The only power switched in the DMU is the 5-volt line. The logic involved is similar to the AMU. The converter signal turns power on prior to the address period and turns power off following it. A DF from the DMU inhibits the power off signal when an address is recognized.

10.3.4 Slave DTU Address/Reply Timing

Timing of the overall slave DTU address/reply cycle in terms of power switching, sampling, and encoding is a relatively complex process. To aid in understanding the sequence, Figures 3.10-36 and 3.10-37 present a simplified response cycle in terms of the internal DTU timing signals for analog and discrete data requests respectively.

TABLE 3.10-5

DMU ADDRESS RECOGNITION

G1	G2	G3	G4	G5	C1	C2	C3	C4	C5
		Slice Enable					Word Select		

C2	C3	C4	C5	Mux Line
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8
1	0	0	0	9
1	0	0	1	10
1	0	1	0	11
1	0	1	1	12
1	1	0	0	13
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16

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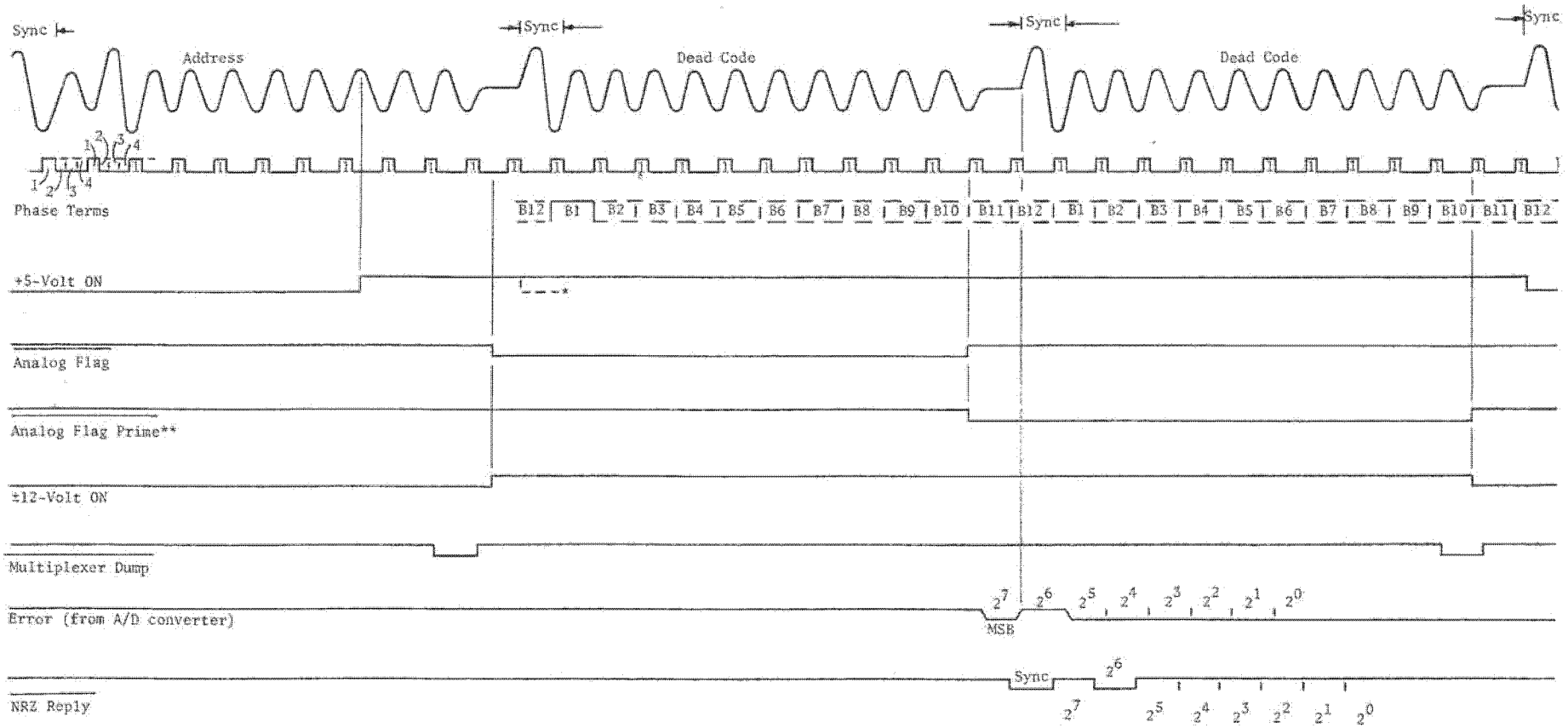

NOTE: Assumes at least three dead codes precede and follow the address ($10\text{-}00_8$). This insures the converter coming up from an unpowered condition and shutting down after reply. (A reply code of 100_8 is shown.)

* If $\overline{AF}$ is not generated, +5-volt power switches off; ±12-volt power is never turned on.

** Analog flag delayed one-word time.

Figure 3.10-36. Simplified Analog Address/Reply Timing

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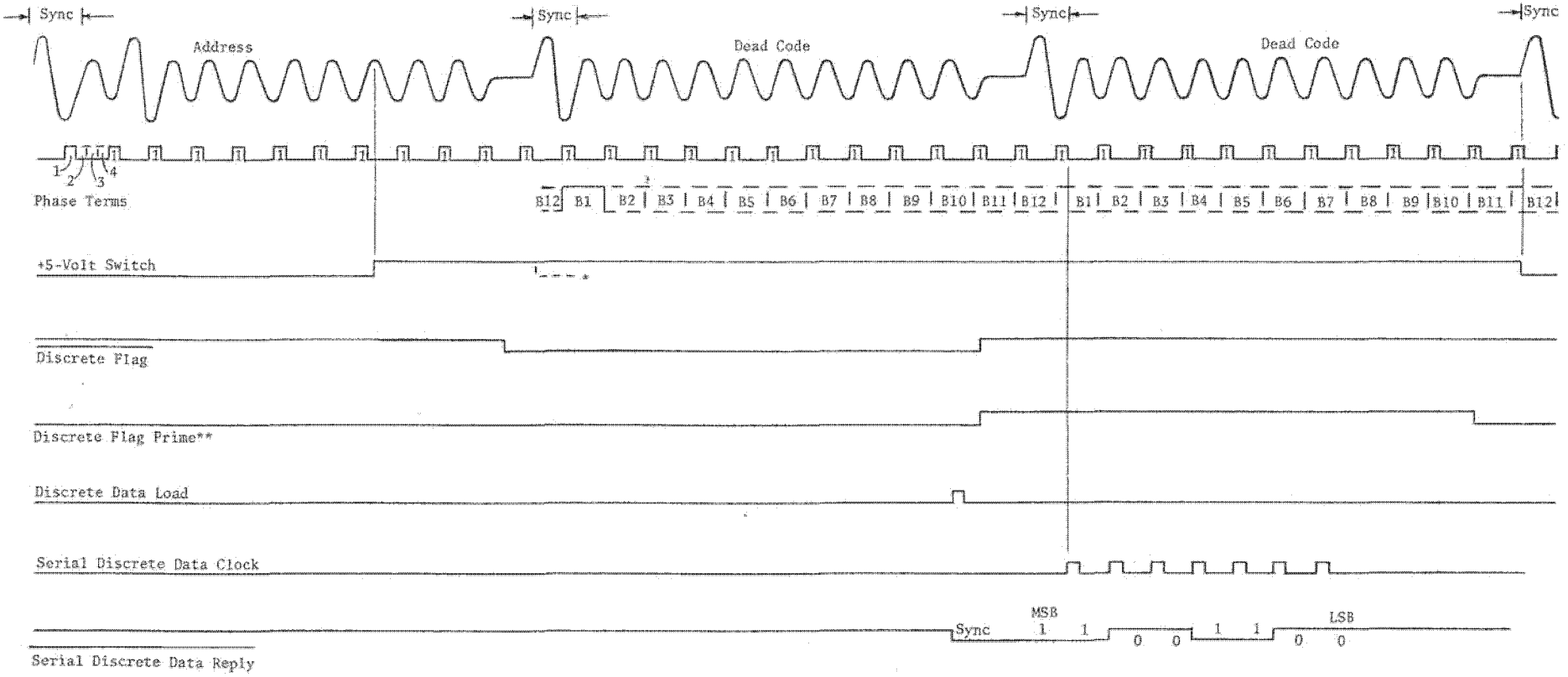

NOTE: Assumes at least three dead codes precede and follow the address ($10\text{-}00_8$). This insures the converter coming up from an unpowered condition and shutting down after reply. (A reply code of 063_8 is shown.)

* If $\overline{DF}$ is not generated, +5-volt power shuts off; ±12-volt power is controlled by analog flag signal and is not turned on.

** Discrete flag delayed one-word time

Figure 3.10-37. Simplified Discrete Address/Reply Timing

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Three-word times are required for the DTU to receive a valid address, decode it, sample and encode the requested input, and respond to the request with a spc party line reply. The number of responses (or duty cycle) required of a single slave is determined by the sampling program in the master unit. The analog and discrete timing figures show a complete power up and power down sequence. However, if the master unit transmits a second address to the slave within two-word times of the first address, the power down sequence will be inhibited for at least the address decode and compare period.

10.4 Master DTU

The MDTU serves as the controller for all telemetry subsystem operations. It generates all operating commands, with the exception of power, for the slave units, and processes all data output by the slaves. In addition, the MDTU can accept a limited number of inputs directly from instrumentation monitors in discrete format only. However, no direct inputs are assigned for use in the PPS/DP EAC.

The two SCS master units (A and B) are completely redundant. Either master can address all slave units, and can output data to either of the two vehicle tape recorders for storage, or to the vehicle transponders for transmission to the ground (reference Figure 3.10-1)*. The system also possesses the capability of recording and transmitting data simultaneously if desired. To avoid interference between data signals from the two MDTU's, only one will be powered at any given time.

10.4.1 MDTU Capabilities

The master unit can accommodate up to eight isolated, short-circuit protected outputs that may be connected in a parallel configuration if so desired. This

*The MDTU output is a pulse code modulated (PCM) signal. For this reason, the MDTU is sometimes referred to as a PCM unit, and this title is often used as an unclassified term for digital telemetry unit.

limits the subsystem to four slave DTU's when redundancy is provided in each slave. At present, the Gambit vehicle incorporates only three dual-sided slaves; two in the SCS, and one in the PPS/DP EAC (see Figure 3.10-38). A fourth slave, the RECAL unit, is used only for testing and is located in the launch pad gantry test console. It receives data from the PPS/DP EAC satellite reentry vehicles through test cables, and interfaces only with SCS master unit A through the PPS/DP EAC junction box. Although the RECAL unit in use is an older design, it is fully compatible with the current telemetry system.

To distinguish between slave units, each is assigned a "dash" number. The two SCS units are known as the -3 and -5 slaves. The PPS/DP EAC unit is -7, and the RECAL unit -9. Presently, the -3 unit consists of two CU's, two AMU's, and two DMU's. The -5 slave is composed of two CU's and only one AMU and one DMU.

In addition to being limited on the number of slave units the MDTU can address, limits are also imposed on the total number of AMU and DMU slices in the subsystem according to the maximum number of unique slice address codes. Based on this, the system can accommodate up to seven AMU slices and six DMU slices. The slice address codes for the -7 slave (PPS/DP EAC) are assigned as shown in Table 3.10-6.

TABLE 3.10-6

-7 (PPS/DP EAC) SLAVE DTU SLICE CODES

Slice	Type	Slice Code*
A3	DMU	000101
A5	AMU	110
A6	AMU	101

*Address Code Bits G1 through G3 for AMU's, and Bits G1 through G5, and C1 for DMU's.

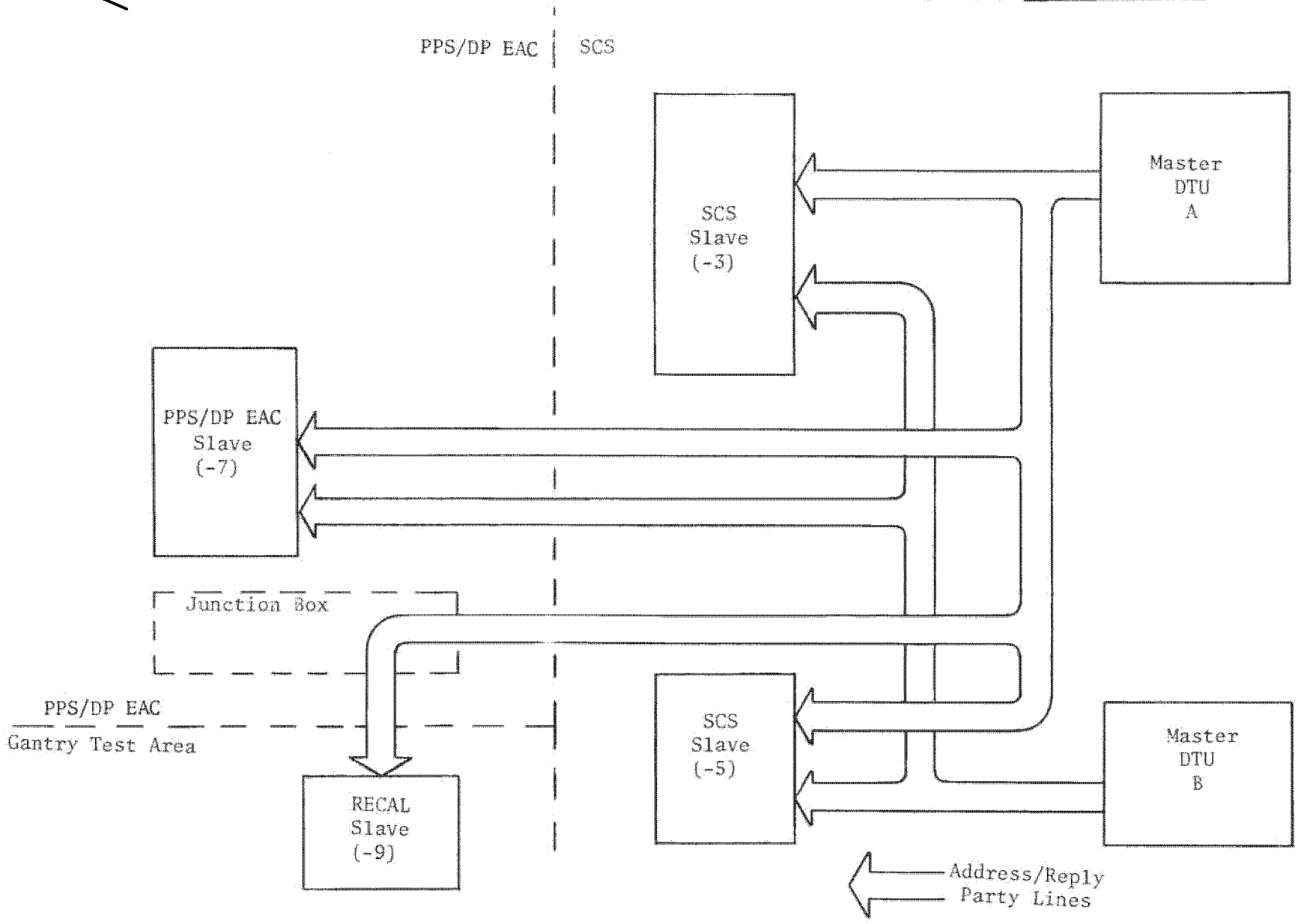


Figure 3.10-38. PSV Slave and Master Telemetry Units

Direct data inputs to the master unit (serial digital data) are limited to 16 channels, with each treated as a discrete (bilevel) signal by the master. When addressed, samples are taken serially from a channel in multiples of eight to form standard eight-bit data words.

The actual rate of data sampling and the order in which it is sampled is controlled by stored programs in the MDTU memory. This programming is accomplished prior to launch, and cannot be altered on-orbit. By using stored programs to control sampling, the telemetry system offers extreme flexibility. Most changes in instrumentation sampling rates or sequences can be made simply by reprogramming the master unit with no hardware changes necessary.

The order in which a stored program directs the MDTU to sample and output information is referred to as a telemetry format. Up to four different formats may be stored in the MDTU for use, with the selection of any particular one controlled by command. In addition, the MDTU offers the capability of generating the data in a serial bit-stream at a rate of 32, 64, or 128 kilobits/second (KBS), equivalent to 4000, 8000, or 16000 eight-bit data words each second. The bit-rate choice for a format is determined by the format program and is automatically selected when the format is commanded.

10.4.2 Slave DTU/MDTU Communication

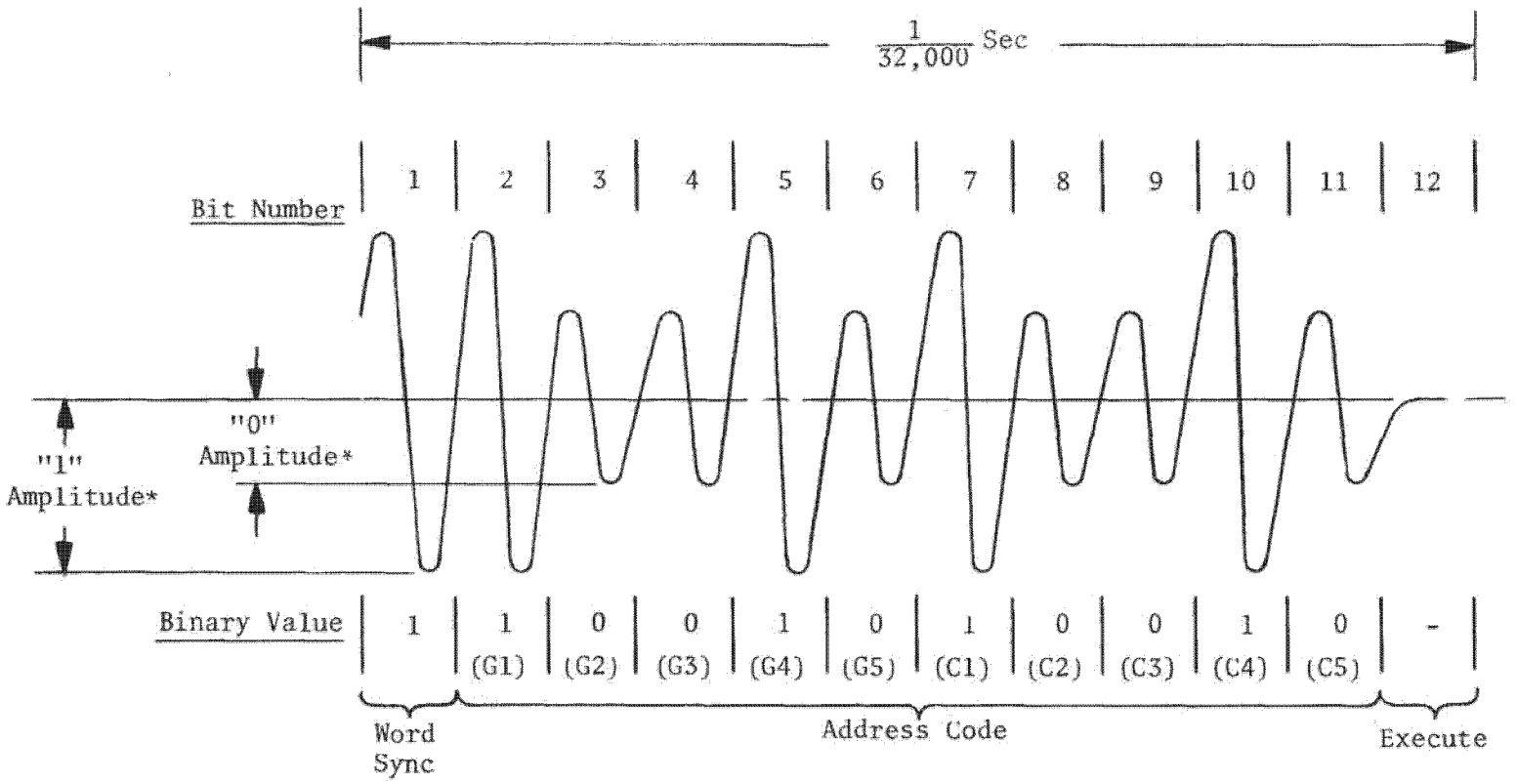
Communication between slave and master units occurs along individual party address and reply lines in the form of trilevel amplitude modulated sinusoids. A full cycle sine wave of one level represents a binary one, and a full cycle sine wave of approximately half the amplitude represents a binary zero. The third level is represented by the dc level. The signal has a fundamental frequency of 384 KHz and spectral components whose magnitude falls off at a rate of 24 decibels per octave beginning at 576 KHz.

The address and reply lines form separate, shielded pairs with their respective returns, and are transformer coupled at both the slave and master DTU's. The lines are completely isolated at the slave units, and are connected to the satellite system ground within the SCS through a center tap on the input transformer of the master unit.

10.4.2.1 Data Channel Address. The data channel address signal, or remote channel address as it is also known, consists of an 11-bit code commencing at the beginning of each party line word time (one word-time is 12 bit-times at the rate of 384 KBS). The remaining portion of the word-time is characterized by the absence of a signal. As shown in Figure 3.10-39, bit 1 is the synchronization bit (binary one) and bits 2 through 11 the 10-bit group-channel address code (G1-G5 and C1-C5 respectively*). The last bit period is allocated for execution time. The signal characteristics are controlled by interface agreement between BIF-008 and LMSC, and are as follows:

(1)	Waveform	Noncontinuous, trilevel, amplitude-modulated sinusoid
(2)	Frequency	384 KBS ± 1%
(3)	Amplitude (average to negative peak):	
	a. At master unit address output	Binary "1": 0.5 ± 0.1 volt Binary "0": 0.2 ± 0.04 volt
	b. At slave unit address input	Binary "1": 0.5 ± 0.4 volt Binary "0": 0.2 ± 0.16 volt
(4)	Voltage Amplitude Ratio	Of "0"s to "1"s: 0.4 ±0.04

*Reference Section 10.3.3.2



*For voltages, reference Section 10.4.2.1

Figure 3.10-39. Remote Channel Address Signal

10.4.2.2 Serial Pulse Code Reply. The spc reply is composed of a synchronization bit (binary one), the eight-bit data word (MSB first), and three bit-times for execution (see Figure 3.10-40). Significant characteristics of the signal are as follows:

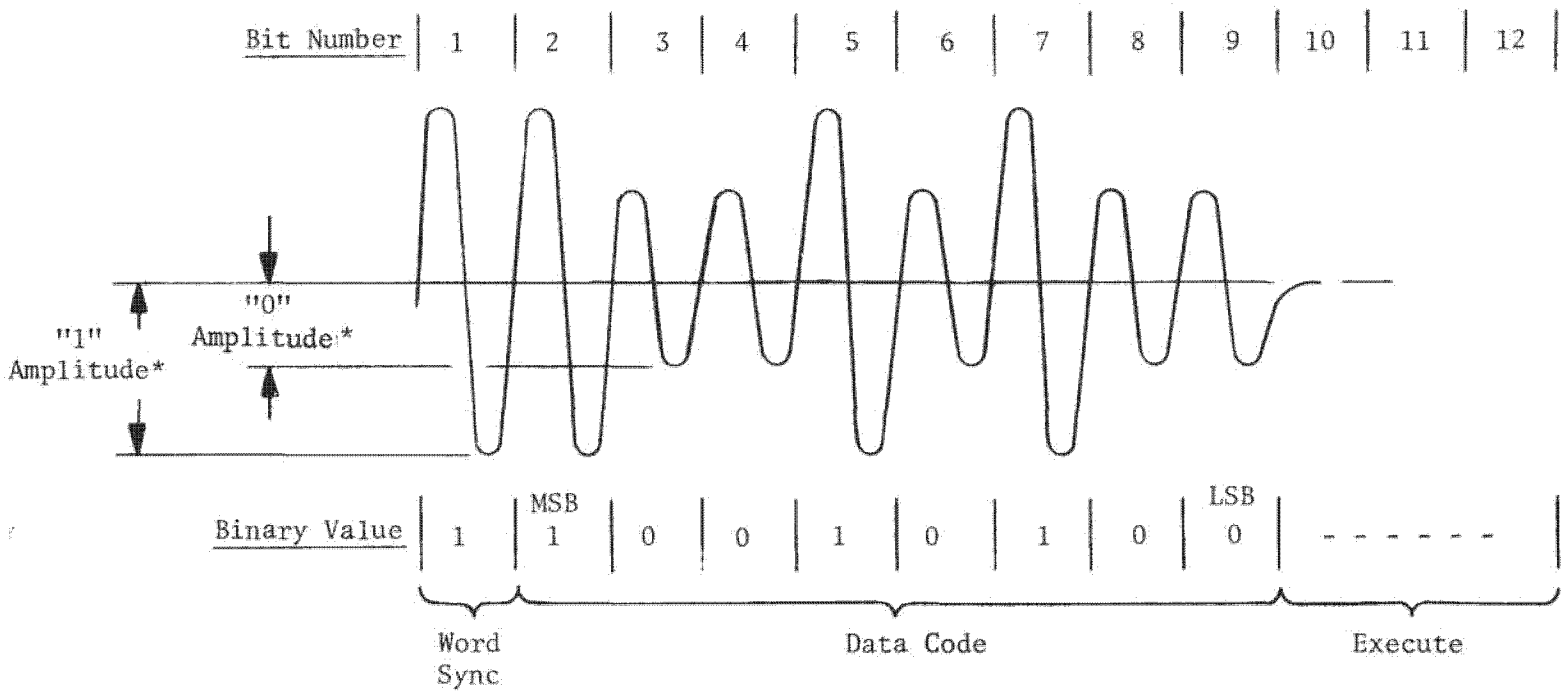
(1)	Waveform	Noncontinuous, trilevel, amplitude-modulated simusoid
(2)	Frequency	384 KBS ± 1%
(3)	Amplitude (average to negative peak):	
	a) At slave unit pulse code output	Binary "1": 0.35 to 0.6 volt Binary "0": 0.1 to 0.3 volt
	b) At master unit pulse code input	Binary "1": 0.1 to 0.9 volt Binary "0": 0.03 to 0.45 volt
(4)	Voltage Amplitude Ratio	Of "0"s to "1"s: 0.4 ± 0.1

Additional requirements levied on the spc signals, and also on the DCA signals, are beyond the scope of this document. For further information, refer to BIF-008 specification 1401-305: Telemetry Requirements - PPS/SCS (9 x 5).

10.4.2.3 Address/Reply Timing. The time from generation of a valid DCA code to return of a spc reply is controlled by the slave unit, which requires one word-time following receipt of the address for sampling and formatting the reply. Thus, a reply is not returned until the second word-time following the DCA as shown in Figure 3.10-41*.

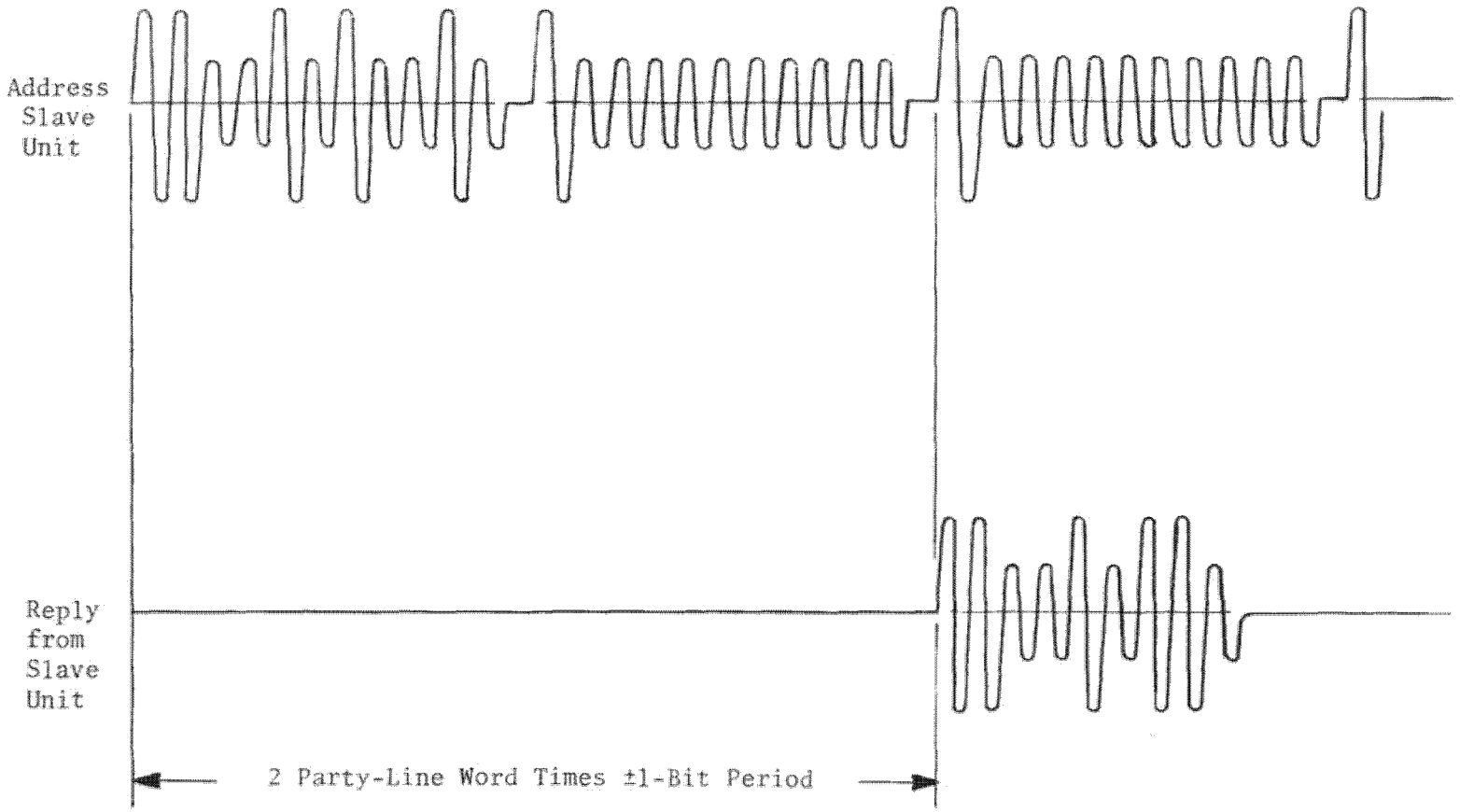
The rate of address signal generation is a function of the format bit-rate. At 128 KBS, a DCA signal is output every second word-time. At 64 KBS, the DCA signals are spaced four word-times apart, and at 32 KBS, eight word-times apart.

*Timing diagrams for slave unit encoding are presented in Section 10.3.4



* For voltages, reference Section 10.4.2.2

Figure 3.10-40. Serial Pulse Code Data Signal



3.10-79

Figure 3.10-41. Time Relationship: Remote Channel Address Code/Serial Pulse Code Data Reply

For each word time between addresses, the MDTU generates a dead code output signal to maintain slave DTU synchronization (see Figure 3.10-42).

To insure synchronization of the master unit with the command system, the master unit clock generating the DCA signals is synchronized to the vehicle command subsystem clock using timing signals from the extended command subsystem (ECS). As a result, it is possible, within reasonable limits, to monitor functions at set times with respect to vehicle command pulse timing by proper programming of the telemetry sampling sequence.

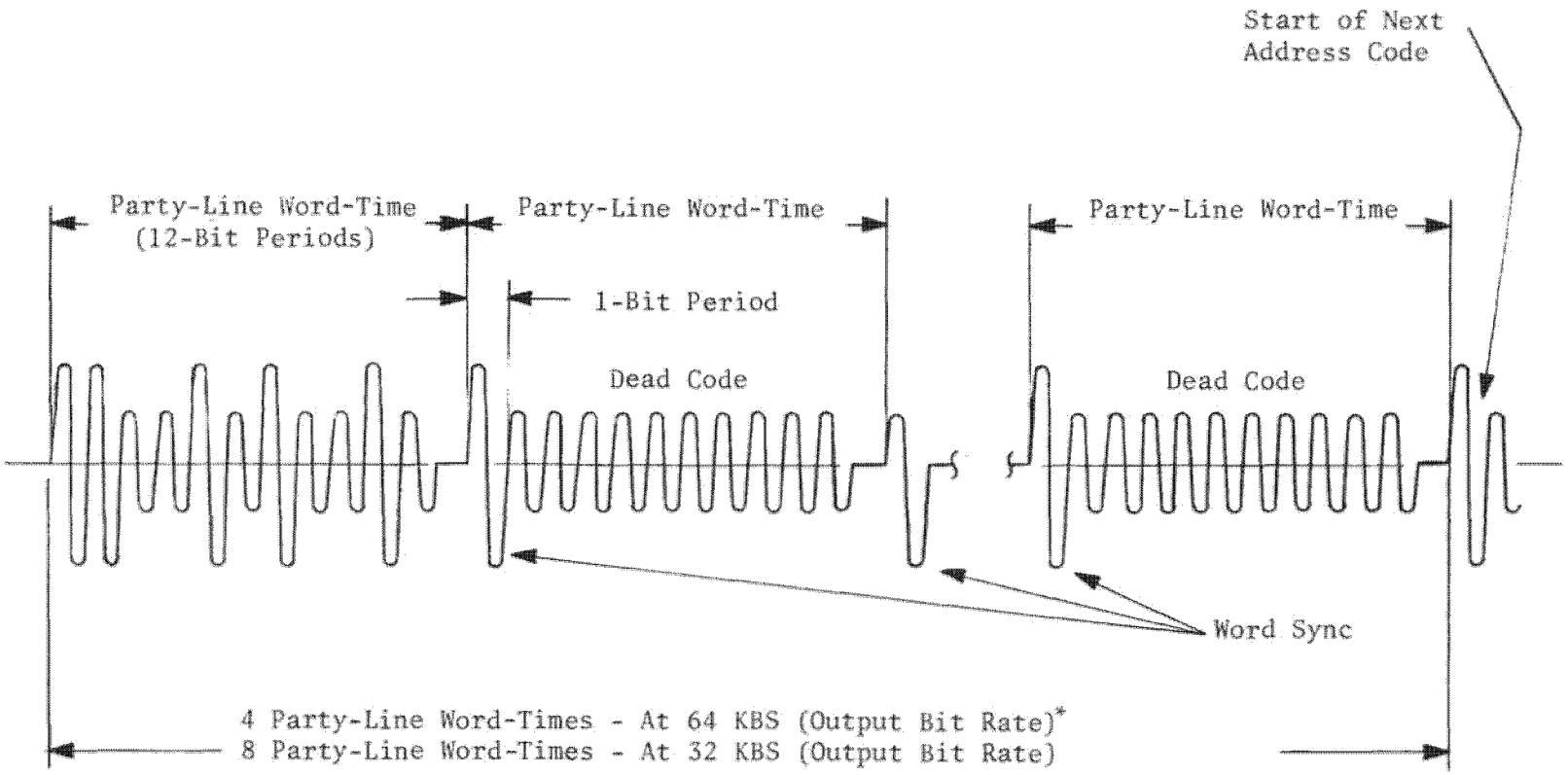
10.4.3 MDTU Telemetry Output

The MDTU reformats the return data from slave units and direct inputs from instrumentation sensors and outputs it in a continuous serial bit-stream. This output, which consists of spc data information and special codes used for data control, is either recorded on the vehicle tape recorder, transmitted to the ground in real time, or is both recorded and transmitted simultaneously.

The output waveform is a square wave non-return-to-zero level (NRZL) pulse train. A sample NRZL square wave which represents the same binary value as the incoming spc data word is illustrated in Figure 3.10-43.

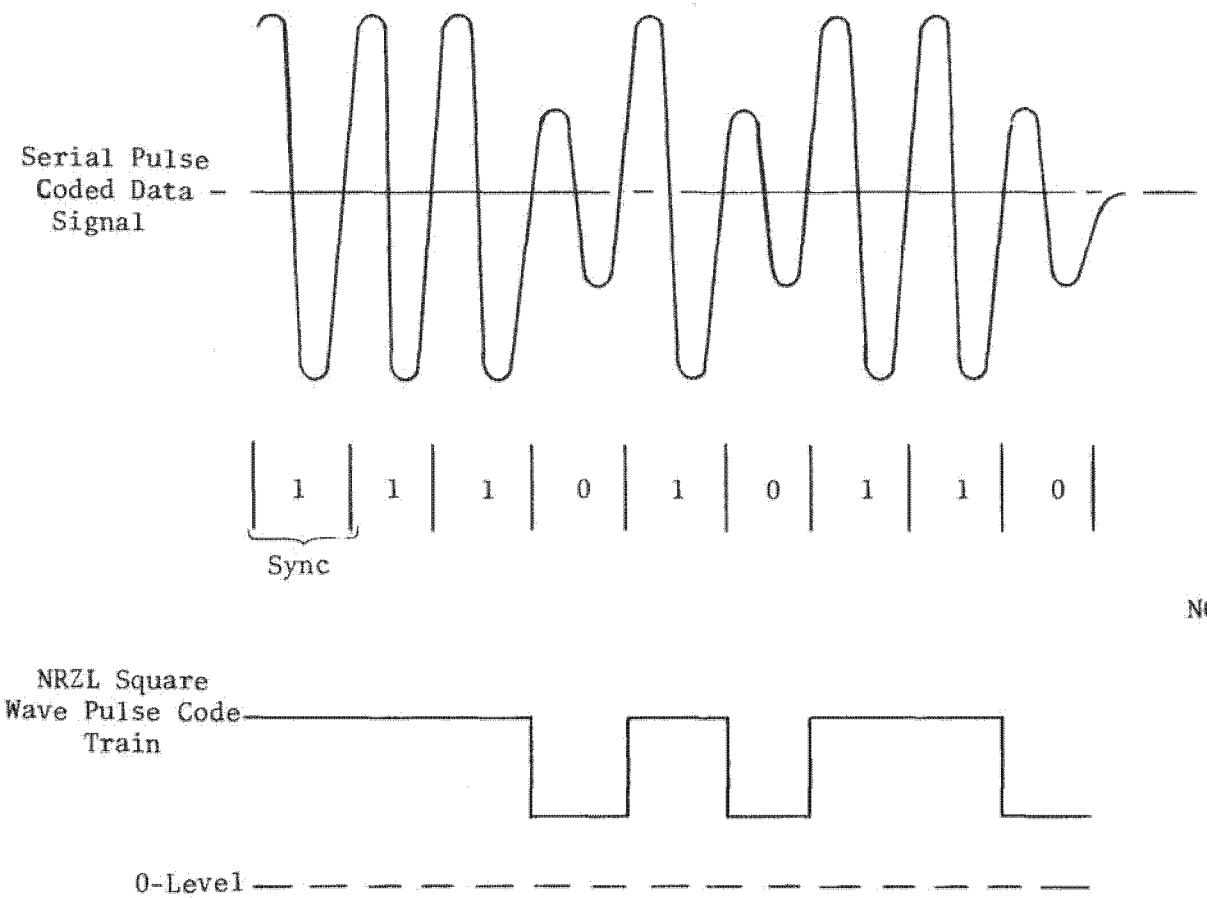
Input to the vehicle tape recorders is cross-strapped such that either tape recorder can accept data from either MDTU. The recorders are capable of operating in either a low-or high-speed record mode to accept data at 32 KBS or 64 KBS*. Upon playback, data is read out at a 256 KBS rate.

*The 128 KBS MDTU capability is not used for the Gambit vehicle. At 32 KBS, the tape recorder can store approximately 90 minutes worth of data, and at 64 KBS, approximately 45 minutes worth.



* At 128 KBS, the next address code begins following one dead code address.

Figure 3.10-42. Remote Channel Address Generation Rate



3.10-82

NOTE: This diagram does not accurately represent timing between signals.

Figure 3.10-43. Binary Coded Square Wave NRZL Pulse Code Train

10.4.4 Telemetry Transmission and Processing

Upon command, data is transmitted to the ground through either of the two space ground link subsystem (SGLS) transmitters. Both real-time and playback data can be transmitted simultaneously through the use of separate subcarrier frequencies. However, the order of data in the bit-stream differs from real time to playback. Real-time data is received at the tracking station, MSB first. Stored data is received LSB first due to the behavior of the tape recorders, which play back in the opposite direction from that in which information was recorded. Therefore, this information is first recorded by the tracking station, and, when desired, read out in the reverse direction to return to the normal bit sequence.

Reporting of the eight-bit data code can be done in several different ways. The most obvious of these, and also the longest in terms of character length, is simply to report the binary number. However, to save space, the binary value is often presented in octal or decimal. The decimal system is used most commonly and the values are referred to as PCM counts. An alternative to this method is the percent bandwidth figure, which is less accurate but has the advantage of requiring only two characters for the full telemetry scale, a prime consideration when space is limited. Based on the 0-volt to 5-volt instrumentation input scale rather than the 0-to 5.06-volt DTU range, this figure represents what percent the telemetry voltage reading (based on the binary signal) is of 5 volts, rounded to the nearest whole number. For comparison, Table 3.10-7 lists the octal and decimal codes, telemetry volts (TMV), and percent bandwidth figures over the full 0.00-to 5.06-volt range.

While these methods are convenient, it is often more advantageous to report information in terms of the actual units being measured. For discrete data, the outputs can be converted back to the eight individual responses composing the word and indicate the state of each function. For analog points, the out-

TABLE 3.10-7

OCTAL COUNT, DECIMAL COUNT, TM VOLTS, AND PERCENT BANDWIDTH CONVERSION

OCT	PCM* DEC CTS	TMV	BW	OCT	PCM* DEC CTS	TMV	BW	OCT	PCM* DEC CTS	TMV	BW	OCT	PCM* DEC CTS	TMV	BW	OCT	PCM* DEC CTS	TMV	BW
001	001	0.00	00	064	052	1.02	20	147	103	2.04	41	232	154	3.06	61	315	205	4.08	82
002	002	0.02	00	065	053	1.04	21	150	104	2.06	41	233	155	3.08	62	316	206	4.10	82
003	003	0.04	01	066	054	1.06	21	151	105	2.08	42	234	156	3.10	62	317	207	4.12	82
004	004	0.06	01	067	055	1.08	22	152	106	2.10	42	235	157	3.12	62	320	208	4.14	83
005	005	0.08	02	070	056	1.10	22	153	107	2.12	42	236	158	3.14	63	321	209	4.16	83
006	006	0.10	02	071	057	1.12	22	154	108	2.14	43	237	159	3.16	63	322	210	4.18	84
007	007	0.12	02	072	058	1.14	23	155	109	2.16	43	240	160	3.18	64	323	211	4.20	84
010	008	0.14	03	073	059	1.16	23	156	110	2.18	44	241	161	3.20	64	324	212	4.22	84
011	009	0.16	03	074	060	1.18	24	157	111	2.20	44	242	162	3.22	64	325	213	4.24	85
012	010	0.18	04	075	061	1.20	24	160	112	2.22	44	243	163	3.24	65	326	214	4.26	85
013	011	0.20	04	076	062	1.22	24	161	113	2.24	45	244	164	3.26	65	327	215	4.28	86
014	012	0.22	04	077	063	1.24	25	162	114	2.26	45	245	165	3.28	66	330	216	4.30	86
015	013	0.24	05	100	064	1.26	25	163	115	2.28	46	246	166	3.30	66	331	217	4.32	86
016	014	0.26	05	101	065	1.28	26	164	116	2.30	46	247	167	3.32	66	332	218	4.34	87
017	015	0.28	06	102	066	1.30	26	165	117	2.32	46	250	168	3.34	67	333	219	4.36	87
020	016	0.30	06	103	067	1.32	26	166	118	2.34	47	251	169	3.36	67	334	220	4.38	88
021	017	0.32	06	104	068	1.34	27	167	119	2.36	47	252	170	3.38	68	335	221	4.40	88
022	018	0.34	07	105	069	1.36	27	170	120	2.38	48	253	171	3.40	68	336	222	4.42	88
023	019	0.36	07	106	070	1.38	28	171	121	2.40	48	254	172	3.42	68	337	223	4.44	89
024	020	0.38	08	107	071	1.40	28	172	122	2.42	48	255	173	3.44	69	340	224	4.46	89
025	021	0.40	08	110	072	1.42	28	173	123	2.44	49	256	174	3.46	69	341	225	4.48	90
026	022	0.42	08	111	073	1.44	29	174	124	2.46	49	257	175	3.48	70	342	226	4.50	90
027	023	0.44	09	112	074	1.46	29	175	125	2.48	50	260	176	3.50	70	343	227	4.52	90
030	024	0.46	09	113	075	1.48	30	176	126	2.50	50	261	177	3.52	70	344	228	4.54	91
031	025	0.48	10	114	076	1.50	30	177	127	2.52	50	262	178	3.54	71	345	229	4.56	91
032	026	0.50	10	115	077	1.52	30	200	128	2.54	51	263	179	3.56	71	346	230	4.58	92
033	027	0.52	10	116	078	1.54	31	201	129	2.56	51	264	180	3.58	72	347	231	4.60	92
034	028	0.54	11	117	079	1.56	31	202	130	2.58	52	265	181	3.60	72	350	232	4.62	92
035	029	0.56	11	120	080	1.58	32	203	131	2.60	52	266	182	3.62	72	351	233	4.64	93
036	030	0.58	12	121	081	1.60	32	204	132	2.62	52	267	183	3.64	73	352	234	4.66	93
037	031	0.60	12	122	082	1.62	32	205	133	2.64	53	270	184	3.66	73	353	235	4.68	94
040	032	0.62	12	123	083	1.64	33	206	134	2.66	53	271	185	3.68	74	354	236	4.70	94
041	033	0.64	13	124	084	1.66	33	207	135	2.68	54	272	186	3.70	74	355	237	4.72	94
042	034	0.66	13	125	085	1.68	34	210	136	2.70	54	273	187	3.72	74	356	238	4.74	95
043	035	0.68	14	126	086	1.70	34	211	137	2.72	54	274	188	3.74	75	357	239	4.76	95
044	036	0.70	14	127	087	1.72	34	212	138	2.74	55	275	189	3.76	75	360	240	4.78	96
045	037	0.72	14	130	088	1.74	35	213	139	2.76	55	276	190	3.78	76	361	241	4.80	96
046	038	0.74	15	131	089	1.76	35	214	140	2.78	56	277	191	3.80	76	362	242	4.82	96
047	039	0.76	15	132	090	1.78	36	215	141	2.80	56	300	192	3.82	76	363	243	4.84	97
050	040	0.78	16	133	091	1.80	36	216	142	2.82	56	301	193	3.84	77	364	244	4.86	97
051	041	0.80	16	134	092	1.82	36	217	143	2.84	57	302	194	3.86	77	365	245	4.88	98
052	042	0.82	16	135	093	1.84	37	220	144	2.86	57	303	195	3.88	78	366	246	4.90	98
053	043	0.84	17	136	094	1.86	37	221	145	2.88	58	304	196	3.90	78	367	247	4.92	98
054	044	0.86	17	137	095	1.88	38	222	146	2.90	58	305	197	3.92	78	370	248	4.94	99
055	045	0.88	18	140	096	1.90	38	223	147	2.92	58	306	198	3.94	79	371	249	4.96	99
056	046	0.90	18	141	097	1.92	38	224	148	2.94	59	307	199	3.96	79	372	250	4.98	0H
057	047	0.92	18	142	098	1.94	39	225	149	2.96	59	310	200	3.98	80	373	251	5.00	0H
060	048	0.94	19	143	099	1.96	39	226	150	2.98	60	311	201	4.00	80	374	252	5.02	0H
061	049	0.96	19	144	100	1.98	40	227	151	3.00	60	312	202	4.02	80	375	253	5.04	1H
062	050	0.98	20	145	101	2.00	40	230	152	3.02	60	313	203	4.04	81	376	254	5.06	1H
063	051	1.00	20	146	102	2.02	40	231	153	3.04	61	314	204	4.06	81				

*PCM Counts

puts can be converted back to "engineering units" using the response curves for the individual monitors. Thus, a temperature monitor response would be reported in terms of degrees Fahrenheit rather than volts.

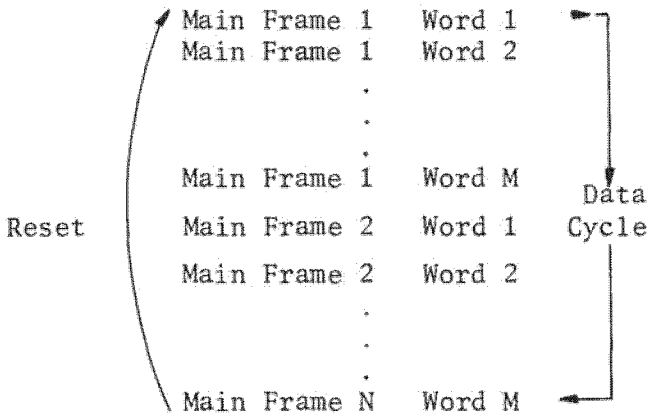
Computer programs have been developed to accomplish these conversion tasks as required. Special programs have also been developed which predict readings for important instrumentation sensors based on commands sent to the vehicle and then compare the predicted and actual results for a rapid check of vehicle "health". Details on the telemetry prediction package are presented in Part 4, Section 7.

10.5 Telemetry Formats

Telemetry format programs determine the sequence in which data is sampled by defining the sample order for a predetermined cycle length. This cycle is then continuously repeated to produce the telemetry output.

The data cycle is one second in length and is composed of eight-bit data words. While the time duration of the cycle is fixed for all formats, the number of words varies as a function of the data rate and is equal to the data rate divided by eight. For example, at a 32 KBS rate, there are 4000 words per data cycle.

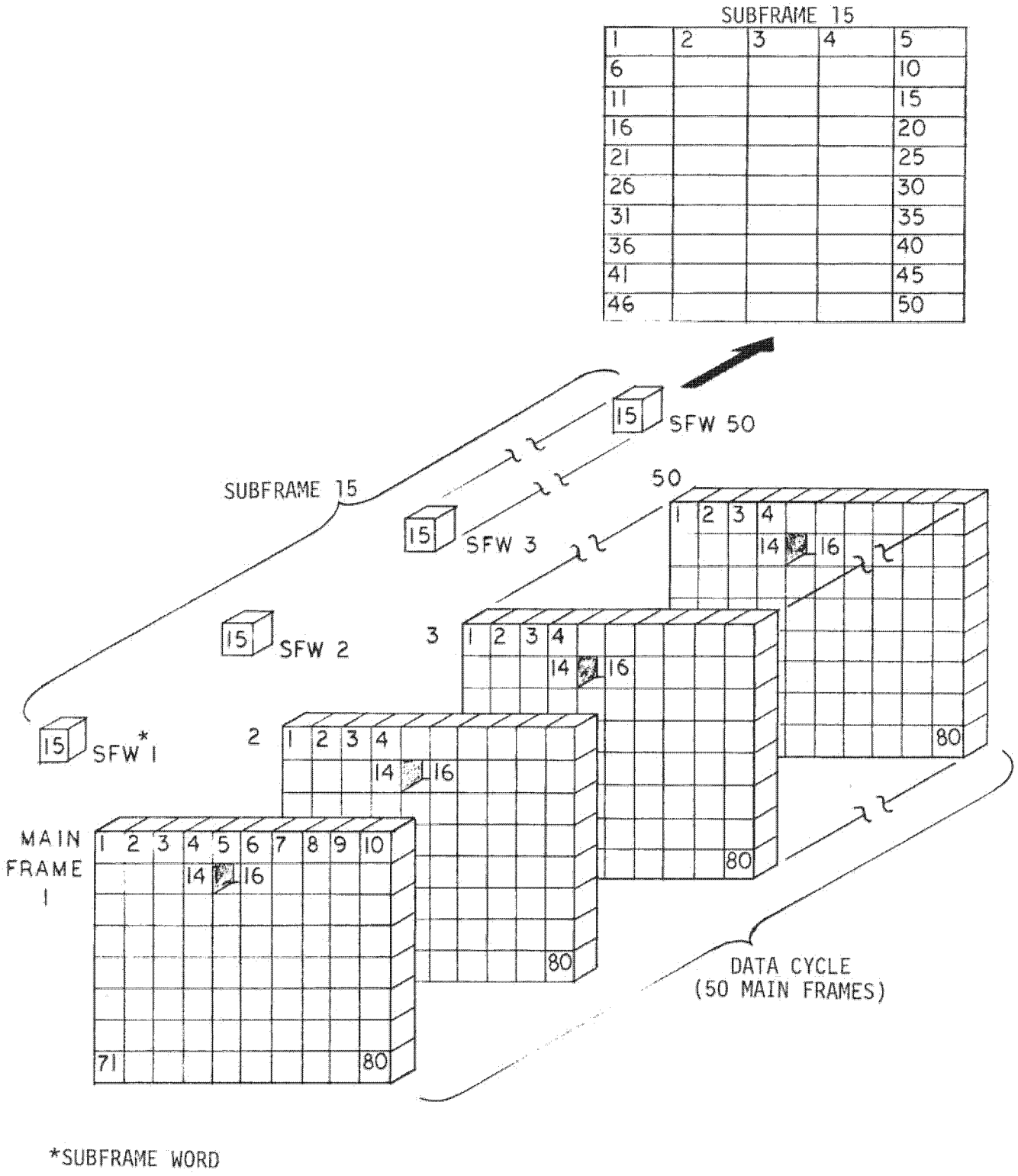
To enable correlation of the data stream, the data cycle is divided into sequential groups of equal numbers of words known as main frames. Each main frame begins with a three-word (24-bit) synchronization code followed by a main-frame code word indicating the main-frame number (its position in the data cycle). The frame number increases by one each time a frame is read out until it reaches the number of frames in the data cycle and resets. Using main-frame notation, the order of information in the data cycle appears as follows:



Where: M = Number of words per main frame

N = Number of main frames per data cycle

In practice, main-frame notation is not always the most useful method of handling data. When establishing a format program, the data cycle is generally grouped in subframes, which simply represent the data sequence in an alternate way that is more convenient for programming purposes. A subframe is that group of words formed by taking the same specific word from each main frame in the data cycle (that is, a word at the same position in each main frame). Thus, the number of words in a subframe corresponds to the number of main frames in the data cycle. Main frames are numbered 1 through N according to the total number of frames in the cycle, and each word in a main frame is numbered 1 through M up to the total number of words per main frame. The subframe number corresponds to the number of the main-frame word from which the subframe words are derived, and the number of the subframe word corresponds to the main-frame number in which it is located. For example, subframe 5 consists of word 5 from main-frame 1 (subframe word 1), word 5 from main-frame 2 (subframe word 2), . . ., and word 5 from main-frame N (subframe word N). Construction of a subframe from the main frame listing is illustrated pictorially in Figure 3.10-44 for a data cycle having 50 main frames.



*SUBFRAME WORD

Figure 3.10-44. Subframe Construction

Handle via BYEMAN
Control System Only

10.5.1 Format Selection

The MDTU is capable of handling a wide range of format options in terms of the number of main frames per data cycle and the number of words per main frame. A summary of these options is presented in Table 3.10-8.

The configuration for any one format is generally chosen on the basis of desired sampling rates for monitors, and limits imposed by the capacity of the MDTU memory. Since the number of main frames in the cycle limits the symmetric sampling rates that are available (symmetric meaning that the samples are equally spaced in the data cycle), the desired sampling rates determine the number of main frames for the cycle. Selection of a data rate (32, 64, or 128 KBS) then establishes the number of words per main frame as each must be of equal length.

10.5.2 Photographic Satellite Vehicle Telemetry Formats

For the Gambit vehicle, the maximum capability of four formats is employed. All four have fifty main frames per data cycle, resulting in symmetrical sampling rates that are factors of fifty; that is, rates of 1, 2, 5, 10, 25, and 50 samples per second. Sampling rates greater than 50, achieved by sampling the monitor on every word of multiple subframes, depend on the number of subframes in the format; in other words, the number of words per main frame. The data rate for format A is set at 32 KBS, resulting in 80 words per main frame. The rates for formats B, C, and D are set at 64 KBS, yielding 160 words per main frame.

Symmetrical sampling rates available above 50 samples/second are speeds of 50 times N, where N is a factor of the number of words per main frame. Thus, at 80 words per main frame, rates of 100, 200, 250, 400, 500, and 800 sps

TABLE 3.10-8

OVERALL MDTU TELEMETER, DATA CAPABILITIES

Function	Capability
Stored formats	4
Bit rates, KBS	32, 64, 128
Analog channels	896
Discrete channels	768
Serial digital channels	16
Main-frame word length	5-256
Data cycle length (frames)	1-128
Channel sample rates (sps)*	1.000 to 15,750
Frame synchronization code (bits pseudorandom)	24
Word length (bits)	8

*sps: samples per second

are possible. Symmetrical rates greater than 800 sps are not possible due to the presence of the synchronization and main-frame identification codes.

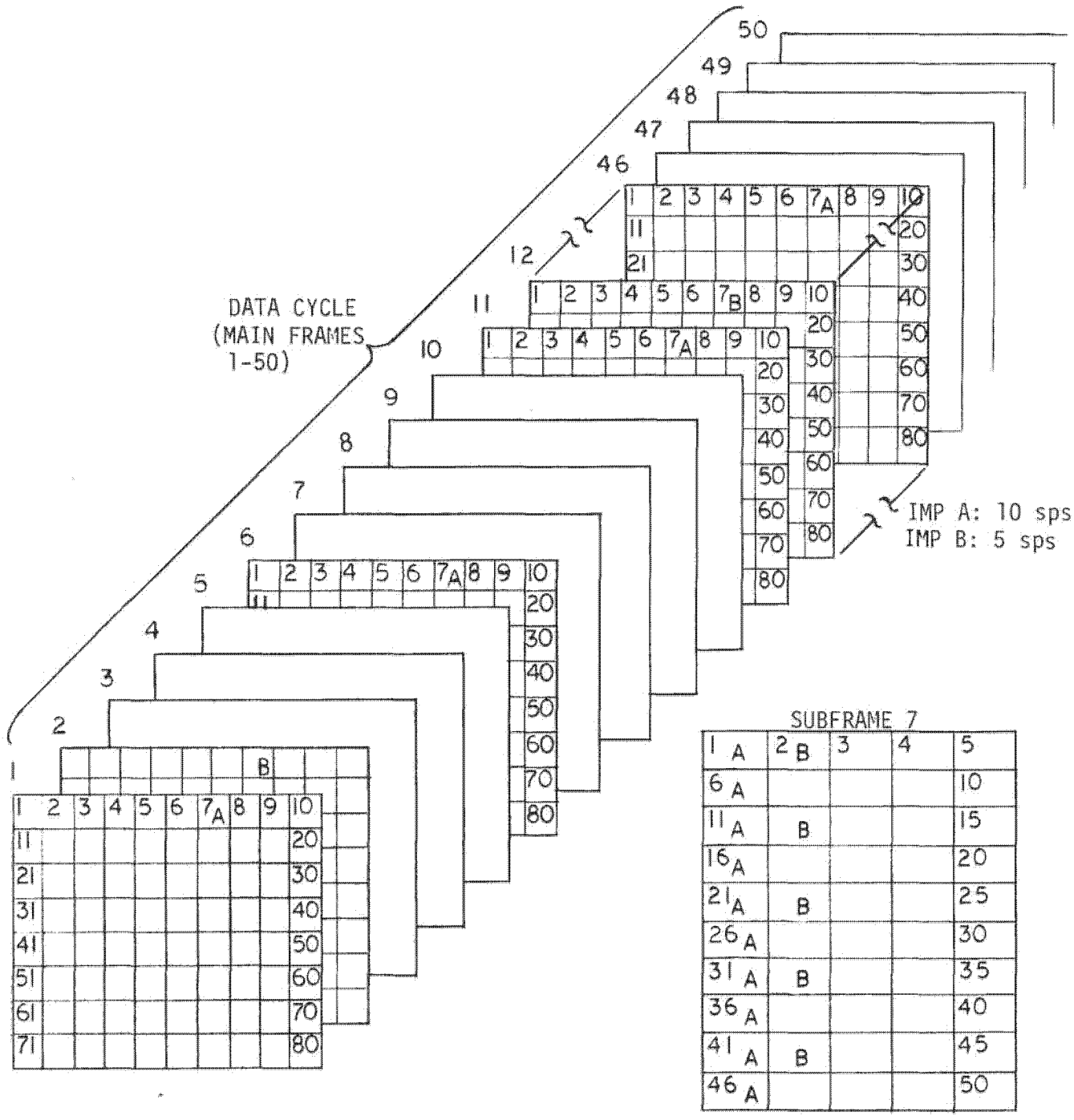
At this point, the advantage of subframe notation becomes apparent. Since each word of a subframe is equally spaced through the data cycle, symmetric sampling of a monitor at 50 sps or less can be obtained by spacing the monitor samples equally throughout the subframe (that is, the monitor is "symmetrically supercommutated" on a subframe). Figure 3.10-45 illustrates the spacing for a point monitored at 10 sps, and for one monitored at 5 sps. To achieve rates greater than 50 sps, the instrumentation point is monitored in each word of multiple subframes which are equally spaced in the main frame as illustrated in Figure 3.10-46. Known as symmetrical supercommutation in the main frame, data rates exceeding 50 sps are used only on selected points in the PPS/DP EAC such as the main current sensor, and the film drive frequency phase lock loop phase error monitors.

10.5.3 Data Position Coding

To designate data positions in the data frame structure, a coding system is used which accommodates the three types of instrumentation signals: Analog, discrete, and serial digital. The code consists of a combination of numbers and a vocabulary of five symbols. The numbers are in the decimal system and the symbols are "slash" (/), "period" (.), "dash" (-), "colon" (:), and "comma" (,). For simplification, the following explanations and examples are based on a format with 50 main frames per data cycle, and 160 words per main frame:

(1) The first number in the designator identifies the main frame word.

Example: "27" indicates that the information is located in the twenty-seventh word of the main frame, or subframe 27.



1 A	2 B	3	4	5
6 A				10
11 A	B			15
16 A				20
21 A	B			25
26 A				30
31 A	B			35
36 A				40
41 A	B			45
46 A				50

Figure 3.10-45. Format Example: 10 sps and 5 sps Monitors

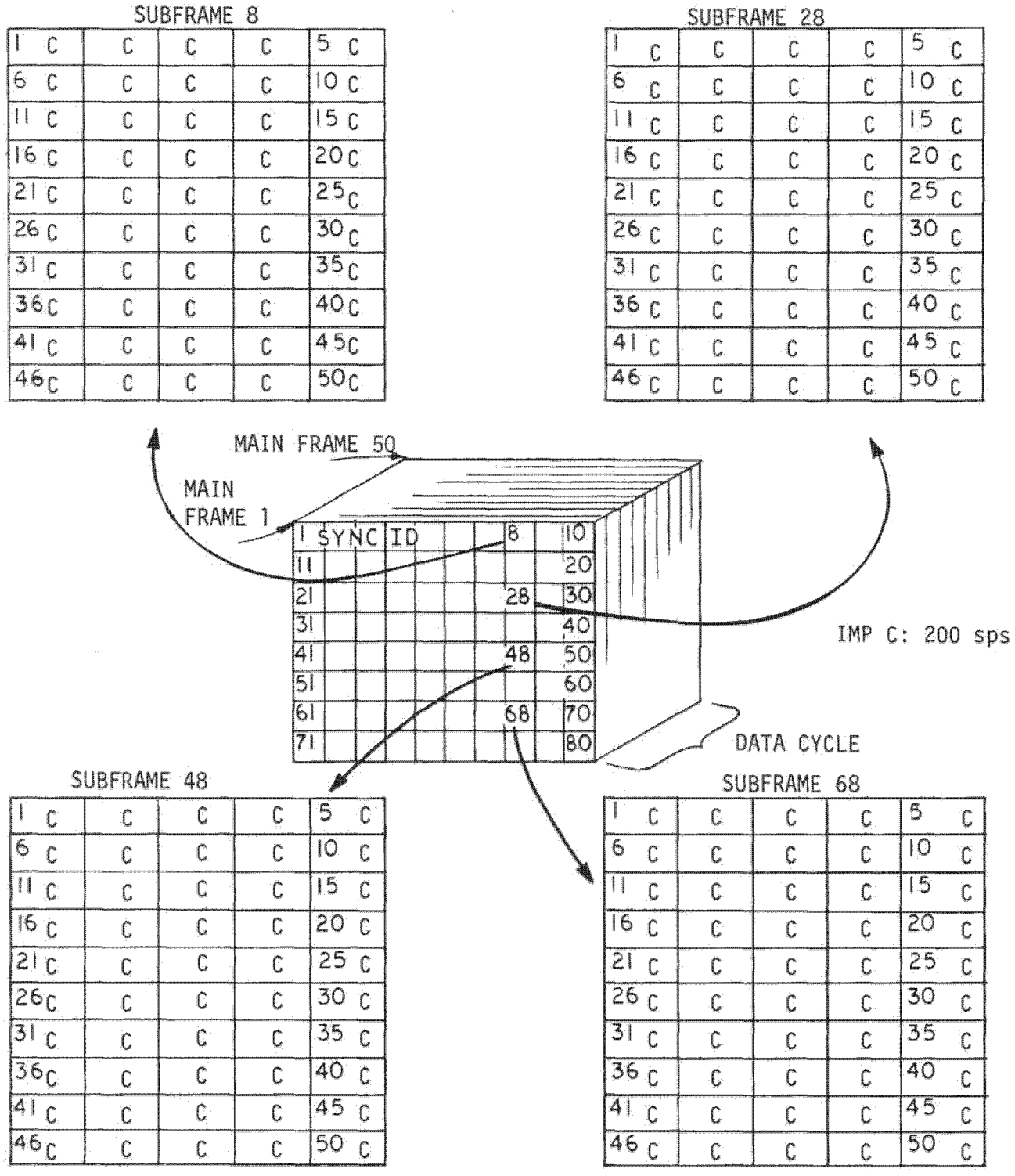


Figure 3.10-46. Format Example: 200 sps Monitor

Handle via BYEMAN Control System Only

(2) A period indicates that the information is symmetrically supercommutated in the main frame (sample rates greater than or equal to 50 sps). The number on the left of the period identifies the first occurrence of the supercommutation. The number to the right of the period identifies the number of times the information is symmetrically supercommutated.

Example: "6.5" indicates that the information is symmetrically supercommutated in the main frame five times; that is, the monitor is sampled in every word of 5 subframes for a rate of 250 sps. The first occurrence is in the sixth word of the main frame (subframe 6) and it appears every "160 divided by five" words thereafter (words 38, 70, 102, and 134).

(3) A comma indicates that the information is nonsymmetrically supercommutated. The number on the left of the comma identifies the first (or previous) occurrence and the number on the right of the comma indicates the next occurrence.

Example: "7, 12, 38, 47" indicates that the information is in the seventh, twelfth, thirty-eighth and forty-seventh words as nonsymmetrical supercommutation. Thus, the monitor is sampled nonsymmetrically at 200 times per data cycle.

(4) A slash signifies that the information is on a subframe. The number to the left of the slash identifies the subframe (the main frame word number) which contains the monitor. The number to the right indicates the word on the subframe which contains the information of interest.

Example: "33/2.5" indicates that the information is located in subframe 33, and is symmetrically supercommutated five

times or every "50 divided by 5" words for a sample rate of 5 sps (subframe words 2, 12, 22, 32, and 42).

Example: "33/19" indicates that the information is located in the nineteenth word of subframe 33.

(5) The dash indicates that the information is in serial digital form. The number on the left identifies the main-frame word which contains the beginning of the serial digital expression and the number on the right indicates the main-frame word which contains the end of this expression.

Example: "7 - 12" indicates that the information is located in the main frame in a serial digital expression which is six main-frame words long beginning with main-frame word seven and ending with main-frame word twelve.

(6) The colon indicates that the information is discrete (bilevel). The number to the left of the colon identifies the word in which the discrete information is located and the number to the right indicates the bit position which contains the discrete information (the MSB is position number one).

Example: "35/46:6" indicates that the information is a discrete point located in the sixth bit of the forty-sixth word of the subframe in main-frame word number thirty five.

To fully indicate the data positions, various combinations of symbols may be used. The following examples help to illustrate this.

Example: "10" signifies the information is symmetrically super-commutated once in main-frame word 10 for a sample rate of 50 sps.

Example: "113-116/1.5" indicates the information is serial digital data located in subframes (main-frame words) 113 through

116 and symmetrically supercommutated on each subframe (subframe words 1, 11, 21, 31, and 41). The first occurrence is subframe 113, word 1, and the last occurrence is subframe 116, word 41.

Example: "157/4:1.5" indicates the information is discrete, and is symmetrically supercommutated on subframe 157. The information occurs on bit 1 of subframe words 4, 14, 24, 34, and 44 for a sample rate of 5 sps.

Example: "15:4.2" signifies the information is discrete data and is symmetrically supercommutated twice in the main frame on the fourth bit of main-frame words 15 and 95. In other words, the point is sampled on the fourth bit of every word in subframes 15 and 95 for a sample rate of 100 sps.

10.5.4 Photographic Satellite Vehicle (PSV) Telemetry Modes

The term mode is used to describe the operational state of the telemetry subsystem: Whether data is being recorded, if data is being transmitted, what format(s) can be used, etc. Five basic modes have been defined for the PSV, each of which serves a special purpose. Four of the modes (low-speed record, normal, diagnostic 1, and diagnostic 2) use distinct data formats for operation, while the fifth (high-speed record) can operate using any one of the three 64 KBS formats. On-orbit, the choice of which modes and formats are to be used at any given time is based on the availability of the mode and the data that will be recovered from the format.

Mode availability is limited by the state of the vehicle. For instance, real-time transmission cannot occur except during periods when the vehicle is in contact with a tracking station.

In terms of formats, the amount of data provided is determined by the percentage of bit-rate allocated to BIF-008 for PPS/DP EAC monitoring. This allocation, established by the number of main-frame words or subframes assigned for BIF-008 use, is illustrated for each format in Figures 3.10-47 through 3.10-50.

Format names indicate the telemetry mode for which they are normally used. The record format is used for the low-speed (32 KBS) record mode in which instrumentation data is stored by the vehicle tape recorder. This mode is intended for use basically during periods when the vehicle is not in contact with a tracking station. This is the only mode the record format can be used for since selecting this format automatically turns on the tape recorder. Additionally, there are no ground facilities available to process 32 KBS real-time data.

The normal format, or real-time format as it is often called, is generally used for real-time readout when the vehicle is in contact with a station. In this mode, instrumentation data from the MDTU is transmitted in real time, and, at the same time, data from the vehicle recorders can be played back for transmission if desired. The normal format is also employed during ascent when data is being both transmitted and recorded simultaneously.

The two diagnostic formats (diagnostic 1 and diagnostic 2) contain many instrumentation points sampled at higher rates than either the record or normal formats provide to aid in analyzing performance of the vehicle. A large portion of diagnostic 1 is assigned to BIF-008 and General Electric Aerospace and Electronic Systems Division* (GE AESD) for high rate sampling, while Lockheed Missiles and Space Company (LMSC) receives a minimal amount of data to adequately monitor operation of the SCS. For diagnostic 2, the situation is reversed. LMSC controls the majority of the format while BIF-008 and GE AESD receive sufficient information to operate in a normal manner.

In use, the diagnostic formats are normally regarded as distinct modes function-

*Manufacturer of the extended and minimal command subsystem hardware.

1 SYNC	2 SYNC	3 SYNC	4 ID	5 PPS	6 PPS		8 PPS
9					14 PPS		16
17					22 PPS		24
25 PPS			28 PPS		30 PPS	31 PPS	32
33					38 PPS	39 PPS	40
41 PPS	42 PPS	43 PPS	44 PPS	45 PPS	46 PPS	47 PPS	48 PPS
49					54 PPS		56
57					62 PPS		64
65 PPS			68 PPS		70 PPS	71 PPS	72
73				77 PPS		79 PPS	80

Record Format

32 KBS
Data Cycle = 1 Second
BIF-008 Allocation = 10.8 KBS

80 Main-Frame Words
50 Main Frames per Data Cycle

Figure 3.10-47. Record Main Frame Format: PPS/DP EAC Allocation

1 SYNC	2 SYNC	3 SYNC	4 ID								12 PPS	13 RECAL			16
17											28 PPS	29 RECAL			32
33											44 PPS				48
49						55 RECAL					60 PPS	61 PPS			64
65															80
81 PPS	82 PPS	83 PPS	84 PPS								92 PPS	93 PPS			96
97											108 PPS	109 PPS			112
113											124 PPS				128
129											140 PPS	141 PPS		143 PPS	144
145				149 PPS							156 PPS	157 PPS			160

3.10-98

Normal (Real-Time) Format

64 KBS
Data Cycle = 1 Second
BIF-008 Allocation = 8 KBS
RECAL = 1.2 KBS

160 Main Frame Words
50 Main Frames per Data Cycle

Figure 3.10-48. Normal (Real Time) Format: PPS/DP EAC Allocation

1 SYNC	2 SYNC	3 SYNC	4 ID	5 PPS		7 PPS					12 PPS	13 PPS			16
17												29 PPS	30 PPS	31 PPS	32
33		35 PPS	36 PPS	37 PPS					42 PPS	43 PPS		45 PPS		47 PPS	48
49 PPS						55 PPS			58 PPS	59 PPS	60 PPS	61 PPS	62 PPS		64
65									74 PPS	75 PPS	76 PPS	77 PPS			80
81 PPS	82 PPS	83 PPS		85 PPS		87 PPS					92 PPS	93 PPS			96
97	98 PPS	99 PPS	100 PPS	101 PPS	102 PPS	103 PPS						109 PPS	110 PPS	111 PPS	112
113		115 PPS	116 PPS	117 PPS					122 PPS			125 PPS		127 PPS	128
129 PPS									138 PPS	139 PPS	140 PPS	141 PPS	142 PPS		144
145			148 PPS	149 PPS		151 PPS			154 PPS	155 PPS	156 PPS	157 PPS			160

Diagnostic 1 Format

64 KBS
Data Cycle = 1 Second
BIF-008 Allocation = 24 KBS

160 Main Frame Words
50 Main Frames per Data Cycle

Figure 3.10-49. Diagnostic 1 Main-Frame Format: PPS/DP EAC Allocation

1 SYNC	2 SYNC	3 SYNC	4 ID								12 PPS				16
17											28 PPS				32
33											44 PPS				48
49											60 PPS	61 PPS			64
65															80
81 PPS	82 PPS	83 PPS	84 PPS								92 PPS	93 PPS			96
97											108 PPS	109 PPS			112
113											124 PPS				128
129											140 PPS	141 PPS			144
145				149 PPS							156 PPS	157 PPS			160

Diagnostic 2 Format

64 KBS
Data Cycle = 1 Second
BIF-008 Allocation = 7.6 KBS

160 Main Frame Words
50 Main Frames per Data Cycle

Figure 3.10-50. Diagnostic 2 Main-Frame Format: PPS/DP EAC Allocation

ing in the same fashion as the normal mode. That is, they are selected for real-time data transmission during station contact periods. However, they also may be used in the high-speed (64 KBS) record mode. To illustrate this, Table 3.10-9 summarizes the various operational modes and indicates which formats may be used for them.

10.6 MDTU Programming

Programming of the MDTU makes use of certain techniques which increase the effective capacity of the memory by requiring fewer instruction words to control the sample formats. The most significant of these techniques, and the one which most affects data arrangement in the formats, is subroutine programming. This procedure greatly enhances programming efficiency, and makes it desirable to create subframes containing monitors of all the same sampling rate. Although programming is not the responsibility of BIF-008, the subroutine technique is discussed here in simplified fashion as it does influence the way in which those portions of the telemetry formats assigned to BIF-008 are used.

10.6.1 MDTU Memory Organization

The master unit memory can be segmented into a maximum of four formats (A,B, C, and D) with seven memory subsections for each format. The first subsection stores initialization instructions for the memory. The second subsection, the main frame instruction memory (IM) routine, contains as many memory words as there are words in each main frame of the particular format (the maximum allowable is 256 words). The remaining five subsections are subroutines which store the specific data channel address.

To generate the DCA sequence, the MDTU steps through the instruction memory at the main-frame rate, repeating the IM cycle as many times as there are main frames in the format data cycle. Each word of the IM subsection, (excluding the syn-

TABLE 3.10-9

FORMAT AND MODE CAPABILITY

	Format Selection			
Mode	Record	Normal (Real Time)	Diagnostic 1	Diagnostic 2
Normal		X		
Low-speed record	X			
High-speed record		X	X	X
Diagnostic 1			X	
Diagnostic 2				X

Note: During ascent, a combination of the normal and high-speed record modes is used, employing the normal (real time) format and is often referred to as the "ascent mode".

chronization and main-frame codes) addresses one of the five subroutines which contain the addresses of the data points. These are stored in the subroutine group-channel section in the proper sequence for the format. Each time a subroutine is accessed, it steps to the next memory location in its subsection. The group-channel address stored there is then output to the slave DTU's (unless the address applies to serial digital data) and the addressed DTU generates an spc reply which becomes the next word in the PCM data stream. When the end of a subroutine is reached, it returns to step 1 and repeats.

For the PSV, the four IM subsections are not all of equal length. The diagnostic 1, diagnostic 2, and normal format IM routines are each 160 words long (since there are 160 words per main frame in these formats) and repeat at the rate of 50 times per second to produce 50 main frames per data cycle. The record format contains only 80 words per main frame resulting in an IM subsection that is 80 words long. However, this format still contains 50 main frames in a data cycle, and thus its IM routine is also repeated 50 times per second.

To illustrate the operation of the MDTU program, an example format has been chosen in which the IM routine addresses subroutine X only twice, once in word 6 and once in word 8. The first pass through the IM routine generates main frame 1 of the programmed format and addresses words 1 and 2 of subroutine X, word 1 at IM word 6, and word 2 at IM word 8. The second time through the IM routine (generating main frame 2) words 3 and 4 of the subroutine are accessed. This procedure continues up to the number of main frames in the data cycle and repeats. Thus, subroutine X contains the group-channel addresses for main frame word 6 in its odd numbered steps, and the addresses for main frame word 8 in its even numbered steps, and the addresses for main frame word 8 in its even numbered steps. Put in terms of subframes, the odd numbered positions of subroutine X contain subframe 6 of the format, and the even-numbered positions contain subframe 8.

Assuming subframes 6 and 8 consist of instrumentation monitors that are all sampled at the rate of 5 sps, the same sequence of group-channel addresses is repeated 5 times in the data cycle. Therefore, the address sequence can be stored in the subroutine memory location once, and the subroutine repeated five times for each data cycle.

10.6.2 Subroutine Construction

As illustrated in the preceding example, the order of addresses in the subroutines is programmed according to the subframes for the format and the arrangement of subframes in the main frame. Each subroutine is assigned a particular sample rate. Therefore, all subframes of the same "length" can be combined into one subroutine. The "length" of a subframe for programming purposes is determined by the lowest sampling rate found in the subframe, and the subroutine rates available. For the PSV formats which have 50 words per subframe, a subframe containing two 25-sample/second monitors is said to have a length of two; that is, only two different addresses must be stored in a subroutine of the MDTU memory and the subroutine repeated at a rate of 25 times/second.

Problems arise, however, when different data rates are mixed in the subframe, or subroutines of a matching rate are not available. Of the five subroutines, two are at fixed rates. The "high-speed address memory" (HSAM) subroutine runs at the main frame rate; in this case, 50 times/second*. The "data cycle memory" (DCM) subroutine runs at the data cycle rate, which for the PSV is one time/second. The three remaining subroutines, 1, 2, and 3 can be set at any symmetric rate between 1 and 50, and rates of 5, 10, and 25 times/second have been chosen.

*Monitors at rates exceeding 50 samples/second (contained in multiple subframes) are programmed as individual subframes in the HSAM subroutine.

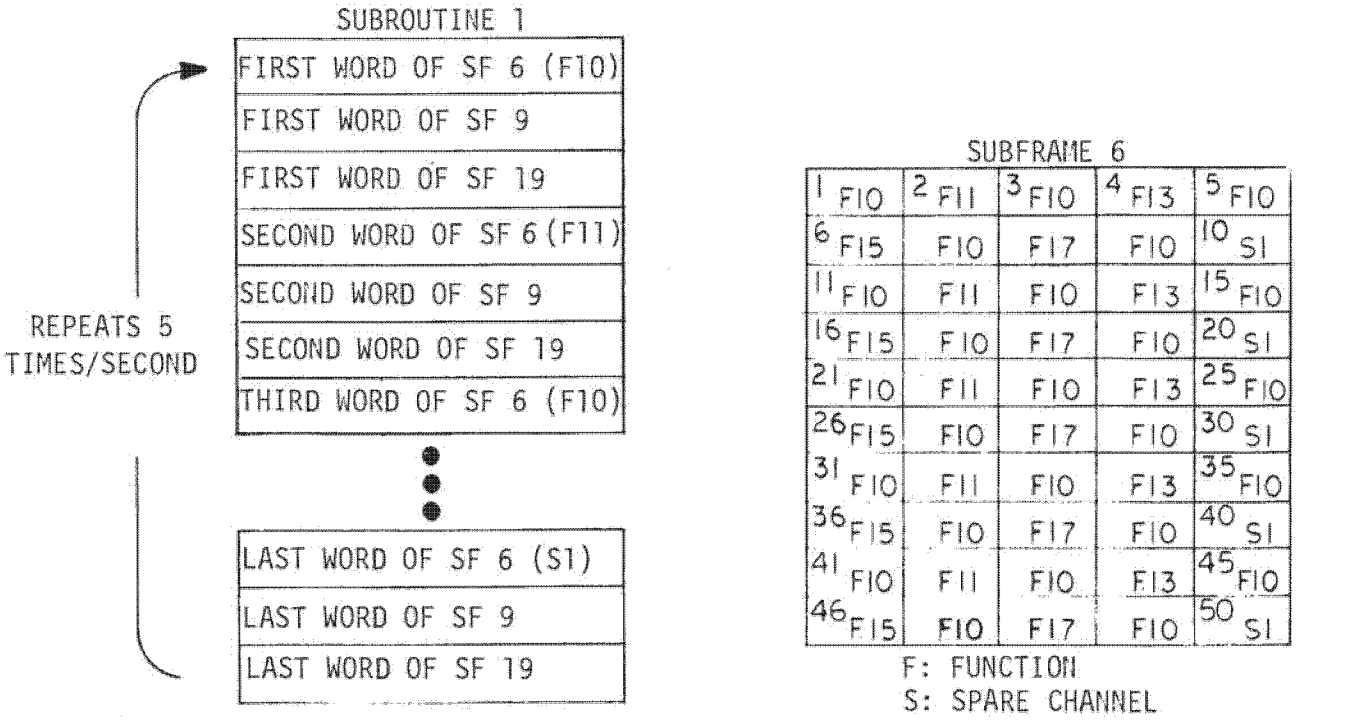
Given a subframe with eight 5-sample/second monitors and five 2-sample/second monitors, the initial subframe length would be 25 (50 words divided by the lowest rate: 2). But with no subroutine available at the rate of two times/second, this subframe must be programmed into the DCM subroutine at a one sample/second rate, requiring 50 individual addresses to be stored in memory.

The effect of the format arrangement on MDTU programming is apparent. While it is not always possible to do so, moving five two-sps monitors to unused positions in other subframes that must be programmed at the DCM rate, would allow the remainder of the subframe to fit into the five sps subroutine. This would then require only 10 address positions in memory rather than 50 (addresses must be supplied for the unused portion of the subframe as well as the eight monitors).

Given the savings possible, it is desirable when constructing formats to limit the subframe "lengths" by placing monitors according to their sampling rates. This consideration may be ignored if there is a need to have functions at certain positions in the data cycle in order to monitor them in time with respect to other functions, or with respect to the vehicle command clock. In fact, restrictions have been placed on the number of subframes used in a format by BIF-008 that must be programmed at the DCM rate (one sps)*.

To summarize, Figure 3.10-51 illustrates the construction of a 5-time/second subroutine for a format containing three subframes of length 10 (5 sps, or greater), including the image memory routine and the monitor arrange-

*Currently BIF-008 may have no more than ten of its assigned subframes in each format at the DCM rate by interface agreement with LMSC.



NOTE: EXAMPLE IS FOR 80 WORDS PER MAIN FRAME, 50 MAIN FRAMES PER DATA CYCLE. SUBROUTINE 1 ADDRESSED ONLY IN WORDS 6, 9, AND 19.

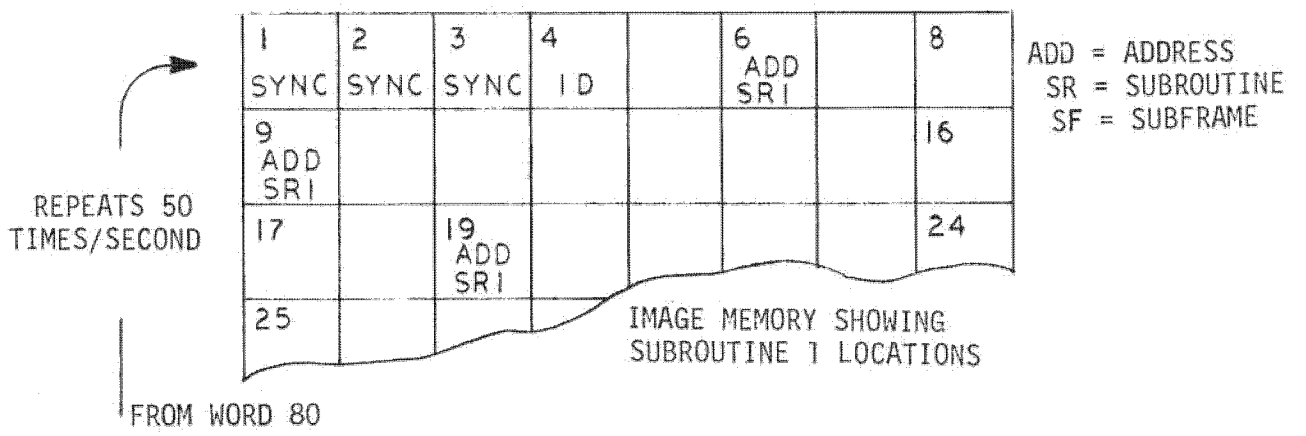


Figure 3.10-51. Subroutine Construction

ment for one of the subframes. Although the illustrated subframe contains a monitor at 25 sps, the presence of monitors at 5 sps requires the subframe to be programmed as if all monitors were 5 sps.

10.7 End-to-End Telemetry Accuracy

The accuracy of the encoded telemetry data from sampling to ground display is dependent on a number of parameters which differ for analog and discrete data. The following analysis is taken from a report published by Aerospace Corporation*.

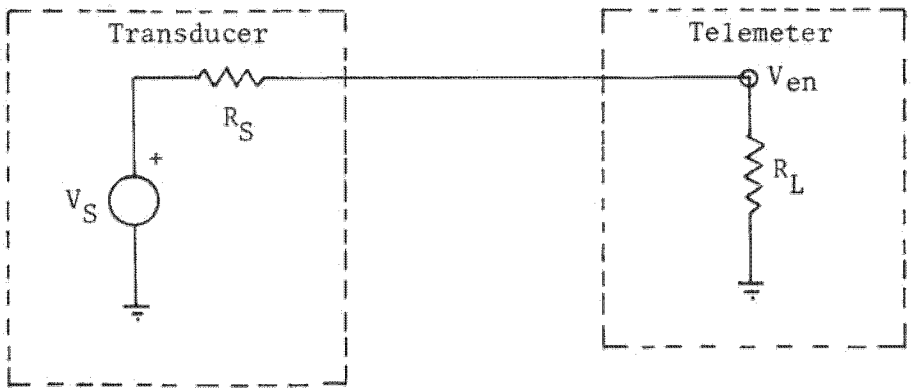
10.7.1 Analog Instrumentation Error

The parameters which affect the end-to-end telemetry accuracy of the encoded analog data signal, with the exception of error in the transducer itself, are as follows:

(1) DC offset
(2) Sampling transient
(3) Digitizing error
(4) Analog-to-digital conversion error
(5) Bit error (transmission)
(6) Digital-to-analog conversion error
(7) Display equipment error

10.7.1.1 DC Offset. The error resulting from dc offset is caused by the telemeter loading the transducer source (see Figure 3.10-52). The analog voltage to be encoded is V_S, but, due to the voltage drop across R_S, the actual encoded voltage, V_{en}, is instead somewhat less.

*Reference BIF-008 document W-N-010019-IH-73.



$$Ven = \frac{R_L}{R_L + R_S} V_S$$

Where: R_L is the load impedance of the Telemeter and R_S is the source impedance of the Transducer.

Figure 3.10-52. DC Offset Error Source

The error is greatest when the transducer source impedance is large. As R_S approaches zero and R_L approaches infinity, the encoded voltage approaches the true analog voltage. The value of R_L is specified to be greater than 2 MΩ at source voltages from 0.0 volts to 5.06 volts. However, a more typical value is 4 MΩ for the slave DTU. The value of R_S is restricted to less than 10 KΩ. The maximum error using the worst case source resistance, and typical slave input resistance is calculated to be 0.25%.

10.7.1.2 Sampling Transient

This error is caused by the input capacitance in the telemeter when the sampling gate is closed (see Figure 3.10-53).

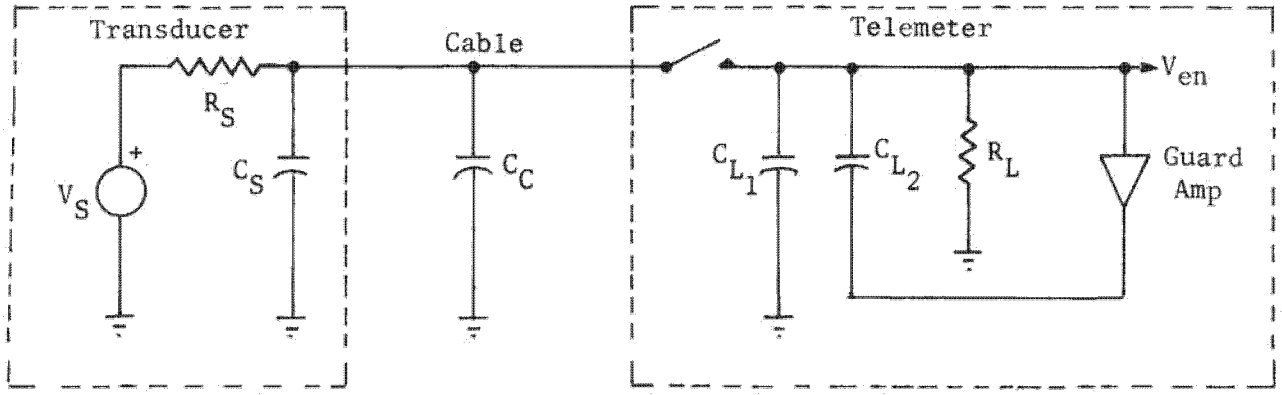


Figure 3.10-53. Sampling Transient Error Source

In this case, the total source capacitance is considered as $C_T = C_S$ (source capacitance) + C_C (cable capacitance). The telemeter input capacitance, C_L, is entirely parasitic and is divided into two portions, C_{L_1} and C_{L_2}. C_{L_1} is called the unguarded capacitance and is the cause for the charge transfer sampling error. C_{L_2} is called the guarded capacitance and reduces the error caused by C_L. This results from the guard amplifier which acts to maintain an equal charge on both sides of C_{L_2}. Thus, the transducer is not required to charge C_{L_2}.

When the sampling gate closes, the charge that exists on C_S and C_C will redistribute itself to create an equal voltage on C_{S_1}, C_C, and C_{L_1} given by:

$$V_{en} = \frac{C_S + C_C}{C_S + C_C + C_{L_1}} V_S$$

The source capacitance is required to be less than 2000 pf or greater than 0.1 μf. The total capacitance (C_T) is worst case in terms of error induced at approximately 2000 pf. The initial error will decrease and approach zero with a time constant of $R_S (C_S + C_C + C_{L_1})$. The settling time provided for this is a maximum of 30 μsec (20 μsec for line charge time within the multiplexer and 10 μsec additional while the sample/hold capacitor is charged).

For smaller values of C_T, the initial error is larger since there is less total charge to be shared with the load capacitance, but the time constant is reduced resulting in a smaller final error. For large values of C_T (greater than 0.1 μf), the amount of charge stored reduces the initial error enough to overcome the effect of the longer time constant.

It is difficult to determine an error figure since the exact ratio of guarded to unguarded capacitance is not known. (Total parasitic capacitance without the guard amplifier would be less than 100 pf.) Experimental data, however, indicates that the error is approximately 0.80% for a worst case source capacitance of 2000 pf and source resistance of 10,000 ohms.

10.7.1.3 Digitizing Error. The analog sample is encoded by a series of eight successive approximations. Each approximation decreases the digitizing error by one-half. Prior to the start of the encoding process, the sample voltage is known to be between 0.0 and 5.06 volts. After the first approximation, it is known that the sample is greater than or less than 2.53 volts, resulting in a first step accuracy of ±1.265 volts. This 1.265-volt

error is called the digitizing error and is reduced during each approximation until, at the conclusion of the eight steps, the digitizing error is less than ±10 millivolts.

10.7.1.4 A/D Conversion Error. The gain, offset, and linearity of the amplifier in the A/D converter lead to additional errors in the encoding process. These errors are unpredictable over the temperature range but are estimated to be less than ±5 millivolts.

10.7.1.5 Bit Error (Transmission). The encoded data is recorded for playback and transmission to the ground stations at a later time and/or transmitted in real time. In either case, the data is affected only by the bit-error rates of the equipment involved. A conservative figure for the overall bit-error rate from the vehicle to the ground tracking station to the satellite test center is 2×10^{-5}. The significance of this error in the end-to-end telemetry accuracy is difficult to determine since the error rate is a probability that any bit (not a particular bit) will be incorrect. Therefore, its contribution is negligible.

10.7.1.6 D/A conversion Error. Data that is maintained in digital form, either in binary, or equivalent PCM counts, does not incur any additional inaccuracy. However, data converted to analog values and reported in terms of percent bandwidth can be in error by as much as ±40 millivolts since a single percent bandwidth represents two to three binary levels (reference Section 10.4.4).

10.7.1.7 Display Equipment Error. Once data has been received, it can be displayed either in numerical form on printers or cathode ray screens, or plotted on a chart recorder. Of the two display methods, only the recorder will add to the error of the data except for major equipment failures. In the past, the recorder error has been shown to be less than 3% by comparison with other forms of data representation.

10.7.2 End-to-End Analog Accuracy Summary

Of the major sources of error for analog telemetry, two are dependent on the output impedance of the transducer, and the remainder are independent of the transducer.

The digitizing error, and A/D conversion error contribute a maximum of ±15 mv inaccuracy. Conversion to percent bandwidth, if performed, results in an additional ±40 mv worst case.

The errors caused by the dc offset and sampling transient are significant when transducers with large source impedances are used. The error caused by the dc offset is approximately -0.25% worst case. The error caused by charge transfer during the sampling period is affected by source capacitance and, under worst case conditions of 10 KΩ and 2000 pf, is approximately -0.80%. The resultant total error due to transducer dependent sources is approximately -1.05%.

Therefore, the worst case end-to-end accuracy of any encoded analog voltage displayed as a digital reading is approximately +0% ±15 mv, -1.05% ±15 mv. Thus, for a 5-volt signal, the maximum error will be +15 mv, -67.5 mv. Data converted to percent bandwidth adds an additional ±40 mv inaccuracy, and, for data recorded on a chart recorder, ±3% maximum inaccuracy is added.

Although there is a large margin of error for the worst case source impedance, very few sensors fit in this range. Typical transducers, exhibiting source impedance in the range of 0 to 5 KΩ shunted by capacitances of 0.1 μf or more, are subject to a worst case error of ±20 mv (specification limit) excluding ground processing errors.

10.7.3 Discrete Instrumentation Error

The parameters which affect the end-to-end telemetry accuracy of the digital data are the same as those for analog data with the exception of the conversion errors (both A/D and D/A) and the digitizing error. The remaining parameters are:

(1) DC offset
(2) Sampling transient
(3) Bit error
(4) Display equipment error

However, since a voltage level of -4 to +1 volt is detected and encoded as a digital 0, and a voltage of +3 to +33 volts is detected and encoded as a digital 1, the errors associated with dc offset, sampling transients, and display equipment error have negligible effect on the data. Thus, the accuracy of encoded discrete telemetry data is affected only by the bit-error rates of the equipment involved. The error rates are the same as those for encoded analog data and are considered negligible.

10.8 Instrumentation Summary

Table 3.10-10 summarizes those instrumentation points directly associated with the instrumentation and telemetry subsystem. Points processed in the IP that do not affect performance of the overall subsystem are not listed, but can be found on the IP schematics presented in Figures 3.10-7 through 3.10-17.

10.9 Command Summary

10.9.1 10V WORD Command (Bits 29 and 30)

TABLE 3.10-10

INSTRUMENTATION AND TELEMETRY SUBSYSTEM INSTRUMENTATION SUMMARY

IMP	TITLE	DESCRIPTION	POWER
5032	PCM 1 ON/OFF, PCM 2 ON/OFF, FDS bits 9, 10	Latching relays tracking the command input relays of the command processor monitor the receipt of commands from the satellite control section and feed either 0.0v or 5.0v to a 4-bit integrated circuit D/A converter. Output occurs in 12 discrete steps ranging from 0.25v to 4.75v in 0.3v increments excluding the following voltage levels: 1.15v; 2.35v; 3.55v; 4.75v. Bit 1 (LSB)* = PCM 1 ON/OFF Bit 2 = PCM 2 ON/OFF Bit 3 = FDS bit 9 Bit 4 (MSB)** = FDS bit 10(LSB)	+5/±15 vdc
5589	DTU 1 ON/OFF	A voltage divider network connected across the switched main power feed to DTU 1 produces a voltage proportional to the main power voltage. The output is converted in the DTU to yield a binary signal (On/Off): "0" = Off "1" = On	Self
5590	DTU 2 ON/OFF	Similar to IMP 5589; monitors the switched power feed to DTU 2.	Self

*LSB = Least Significant Bit
**MSB = Most Significant Bit

TABLE 3.10-10 (CONT'D)

IMP	TITLE	DESCRIPTION	POWER
5196	+15 vdc supply	A divider circuit in the instrumentation processor produces a voltage proportional to the voltage level of the +15 vdc regulated supply. The output is linear from 0.0v (0.0v supply level) to 4.0v (15.0v supply level).	+15 vdc
5198	+5 vdc supply	A divider network in the instrumentation processor produces a voltage proportional to the voltage level of the +5v regulated supply. The output varies linearly from 0.0v (0.0v supply level) to 4.0v (5.0v supply level).	+5 vdc
5200	-15 vdc supply	A divider network, which uses the +5 vdc supply as a bias source, produces an output proportional to the voltage level of the -15 vdc supply. The output is linear from 4.0v (0.0v supply level) to 1.0v (-15.0v supply level).	+5/-15 vdc
5330	Temperature telemetry unit Section 1	The temperature inside DTU 1 is monitored by a thermistor located on the power supply circuit board. The output is nonlinear from -20F (5.05v) to +155F (0.7v).	+15 vdc
5331	Temperature telemetry unit Section 2	Similar to IMP 5330, monitors the temperature inside DTU 2.	+15 vdc

(10V06XYZ, bits 29, 30)

Function: This command controls the DTU states and determines the power state of the ±15-volt and +5-volt instrumentation power supplies.

Bit No.	Function
29-1	DTU 1 ON
29-0	DTU 1 OFF
30-1	DTU 2 ON
30-0	DTU 2 OFF

Interlocks: DTU 1 and 2 are logically interlocked to preclude simultaneous operation. Commanding DTU 1 ON while DTU 2 is already operating will remove power from both sides of the DTU. One side must be in the OFF state to permit the other to receive power.

10.9.2 M6V WORD (Bits 33 and 34)

(M6V002YZ, bits 33 and 34)

Function: This command controls the DTU states, the environmental power circuits, and the 5 parking brake power. The pressure transducer and the ±15-volt and the +5-volt instrumentation power supplies are also switched by the DTU commands.

Bit No.	Function
Implicit	Spare
33-1	DTU 1 ON
33-0	DTU 1 OFF
34-1	DTU 2 ON
34-0	DTU 2 OFF
35-1	Heater branches 1, 2, 4, 5, and 6, and 5 parking brake ON
35-0	Heater branches 1, 2, 4, 5, and 6, and 5 parking brake OFF
36-1	EPSM 1 ON
36-0	EPSM 1 OFF
37-1	EPSM 2 ON
37-0	EPSM 2 OFF
38-1 and 0	Spares

Interlocks:

(1) DTU 1 and 2 are logically interlocked to preclude simultaneous operation. Commanding DTU 1 ON while DTU 2 is already operating will remove power from both sides of the DTU. One side must be in the OFF state to permit the other to receive power.

(2) Commanding 5 OP ON or 9/5 RUNOUT ON will disable the 5 parking brake circuit. The circuit will not be re-enabled until both 5 OP and 5 parking brake power are off.

10.9.3 DTU ON Commands (MR)

DTU 1 ON (MR 21)
DTU 2 ON (MR 22)

Function: These commands control power to the indicated DTU side. They also control power to the pressure transducer and the ±15-volt and +5-volt instrumentation power supplies.

Interlocks: DTU 1 and DTU 2 are electrically interlocked to prevent power application to both at the same time. Commanding DTU 1 ON while DTU 2 is operating will remove power from both sides of the DTU. One side must be in the OFF state to permit the other to receive power.

10.9.4 DTU OFF Command (Umbilical)

Function: This is a vehicle umbilical command (BIL 8005) which removes power from both sides of the DTU.